

RAD-TOLERANT CLASS V, DUAL DIFFERENTIAL LINE RECEIVER

FEATURES

- Single 5-V Supply
- Differential Line Operation
- Dual Channels
- TTL Compatibility
- ± 15 -V Common-Mode Input Voltage Range
- ± 15 -V Differential Input Voltage Range
- Individual Channel Strobes
- Built-In Optional Line-Termination Resistor
- Individual Frequency Response Controls
- Designed for Use With Dual Differential Drivers SN55183 and SN75183
- Designed to Be Interchangeable With National Semiconductor DS7820A and DS8820A
- Rad-Tolerant: >40 kRad (Si) ELDRS
- QML-V Qualified, SMD 5962-79008

DESCRIPTION/ORDERING INFORMATION

The SN55182 dual differential line receiver is designed to sense small differential signals in the presence of large common-mode noise. This device gives TTL-compatible output signals as a function of the polarity of the differential input voltage. The frequency response of each channel can be easily controlled by a single external capacitor to provide immunity to differential noise spikes. The output goes to a high level when the inputs are open circuited. A strobe input (STRB) is provided that, when in the low level, disables the receiver and forces the output to a high level.

The receiver is of monolithic single-chip construction, and both halves of the dual circuits use common power-supply and ground terminals.

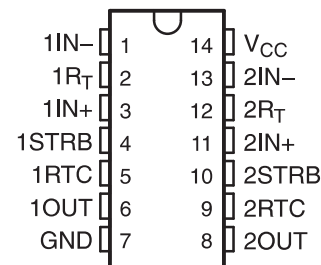
The SN55182 is characterized for operation over the full military temperature range of -55°C to 125°C .

PACKAGING/ORDERING INFORMATION⁽¹⁾

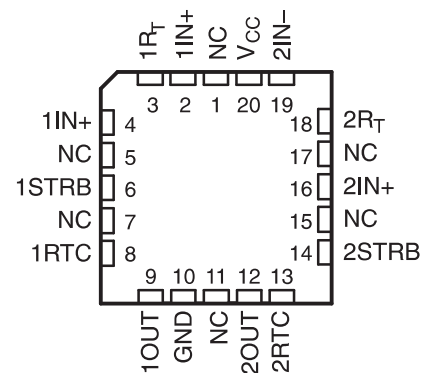
| TEMPERATURE | PACKAGED DEVICES | |
|--|---|-----------------|
| | CERAMIC FLATPACK W (14) ⁽²⁾ | SYMBOL |
| -55°C to 125°C | 5962-7900801VDA | 5962-7900801VDA |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

SN55182... J OR W PACKAGE
SN75182... N PACKAGE
(TOP VIEW)



SN55182... FK PACKAGE
(TOP VIEW)



NC – No internal connection



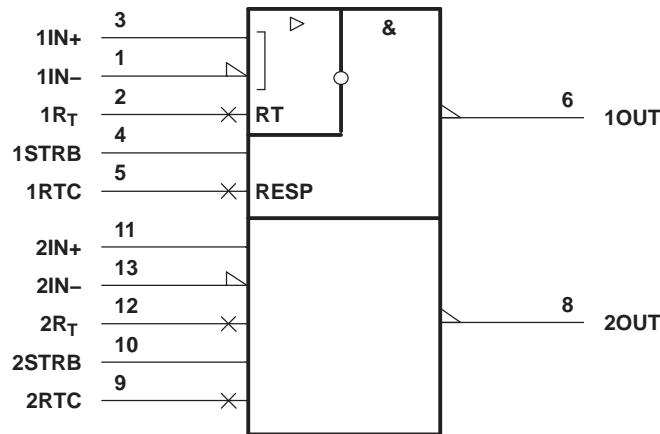
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTION TABLE⁽¹⁾

| INPUTS | | OUTPUT OUT |
|--------|-----------------|------------|
| STRB | V _{ID} | |
| L | X | H |
| H | H | H |
| H | L | L |

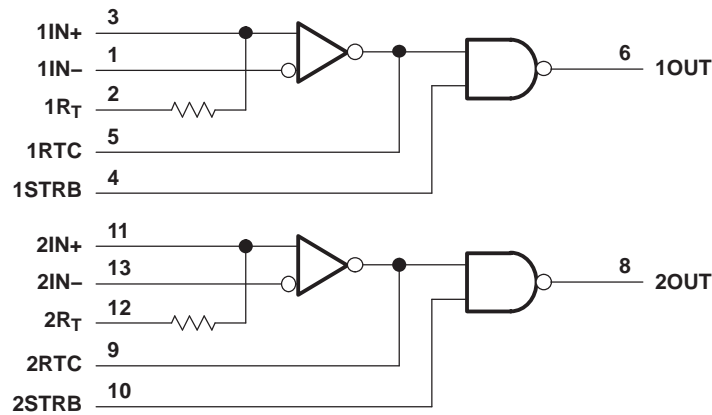
- (1) H = $V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max
 L = $V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max
 X = irrelevant

LOGIC SYMBOL



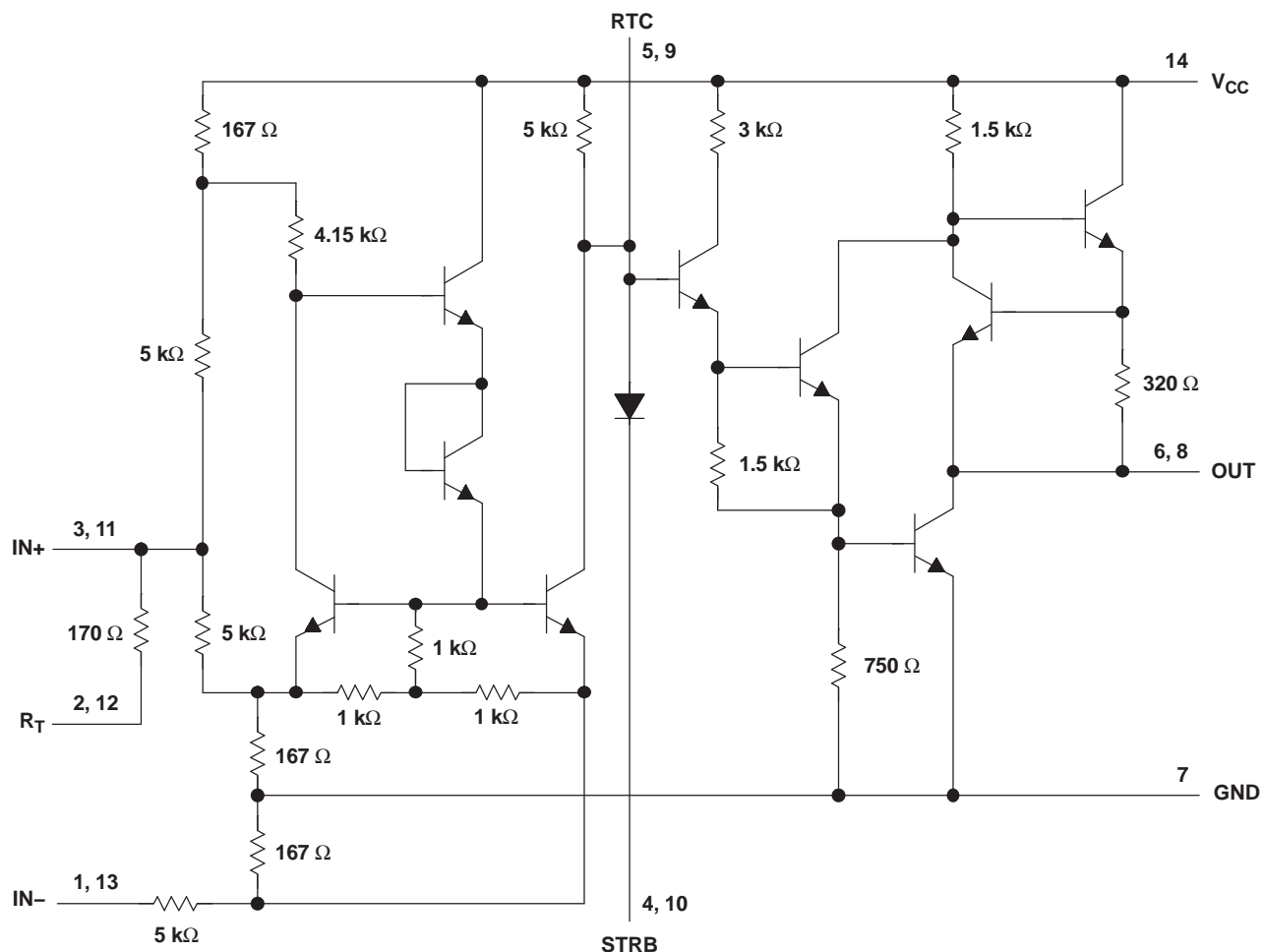
This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the J, N, and W packages.

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the J, N, and W packages.

SCHEMATIC (EACH RECEIVER)



Resistor values shown are nominal.
Pin numbers shown are for the J, N, and W packages.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | UNIT |
|----------------------|--|------------------------------|
| V _{CC} | Supply voltage ⁽²⁾ | 8 V |
| V _{IC} | Common-mode input voltage | ±20 V |
| V _{ID} | Differential input voltage ⁽³⁾ | ±20 V |
| V _{I(STRB)} | Strobe input voltage | 8 V |
| I _O | Output sink current | 50 mA |
| | Continuous total power dissipation | See Dissipation Rating Table |
| T _{stg} | Storage temperature range | –65°C to 150°C |
| | Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package | 300°C |

- (1) The absolute maximum ratings under any condition are limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) All voltage values, except differential voltages, are with respect to network ground terminal.
- (3) Differential voltage values are at the noninverting terminal with respect to the inverting terminal.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$ POWER RATING | $T_A = 125^\circ\text{C}$ POWER RATING |
|------------------|---|---|--|---|
| W ⁽¹⁾ | 1000 mW | 8.0 mW/°C | 640 mW | 200 mW |

(1) In the FK, J, and W packages, SN55182 chips are alloy mounted.

RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|-----------------------|---------------------------------|-----|-----|------|------|
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V_{IC} | Common-mode input voltage | | | ±15 | V |
| $V_{IH(\text{STRB})}$ | High-level strobe input voltage | 2.1 | | 5.5 | V |
| $V_{IL(\text{STRB})}$ | Low-level strobe input voltage | 0 | | 0.9 | V |
| I_{OH} | High-level output current | | | –400 | μA |
| I_{OL} | Low-level output current | | | 16 | mA |
| T_A | Operating free-air temperature | –55 | | 125 | °C |

ELECTRICAL CHARACTERISTICS

over recommended ranges of V_{CC} , V_{IC} , and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | | MIN | TYP ⁽²⁾ | MAX | UNIT | |
|----------------|--|--|--|--------------------------|--------------------|------|---------------|----|
| V_{IT+} | Positive-going input threshold voltage | $V_O = 2.5\text{ V}$, $I_{OH} = -400\ \mu\text{A}$ | $V_{IC} = -3\text{ V to }3\text{ V}$ | | | 0.5 | V | |
| | | | $V_{IC} = -15\text{ V to }15\text{ V}$ | | | 1 | | |
| V_{IT-} | Negative-going input threshold voltage | $V_O = 0.4\text{ V}$, $I_{OL} = 16\text{ mA}$ | $V_{IC} = -3\text{ V to }3\text{ V}$ | | | -0.5 | V | |
| | | | $V_{IC} = -15\text{ V to }15\text{ V}$ | | | -1 | | |
| V_{OH} | High-level output voltage | $V_{ID} = 1\text{ V}$, $V_{(STRB)} = 2.1\text{ V}$, $I_{OH} = -400\ \mu\text{A}$ | | 2.5 | 4.2 | 5.5 | V | |
| | | | $V_{ID} = 1\text{ V}$, $V_{(STRB)} = 0.4\text{ V}$, $I_{OH} = -400\ \mu\text{A}$ | 2.5 | 4.2 | 5.5 | | |
| V_{OL} | Low-level output voltage | $V_{ID} = -1\text{ V}$, $V_{(STRB)} = 2.1\text{ V}$, $I_{OL} = 16\text{ mA}$ | | 0.25 | | 0.4 | V | |
| I_I | Input current | | Inverting input | $V_{IC} = 15\text{ V}$ | | 3 | 4.2 | mA |
| | | | | $V_{IC} = 0$ | | 0 | -0.5 | |
| | | | | $V_{IC} = -15\text{ V}$ | | -3 | -4.2 | |
| | | | Noninverting input | $V_{IC} = 15\text{ V}$ | | 5 | 7 | |
| | | | | $V_{IC} = 0$ | | -1 | -1.4 | |
| | | | | $V_{IC} = -15\text{ V}$ | | -7 | -9.8 | |
| $I_{IH(STRB)}$ | High-level strobe input current | $V_{(STRB)} = 5.5\text{ V}$ | | | | 5 | μA | |
| $I_{IL(STRB)}$ | Low-level strobe input current | $V_{(STRB)} = 0$ | | | | -1 | -1.4 | mA |
| r_i | Input resistance | | Inverting input | | 3.6 | 5 | k Ω | |
| | | | Noninverting input | | 1.8 | 2.5 | | |
| | Line-terminating resistance | $T_A = 25^\circ\text{C}$ | | 120 | 170 | 250 | Ω | |
| I_{OS} | Short-circuit output current | $V_{CC} = 5.5\text{ V}$, | $V_O = 0$ | -2.8 | -4.5 | -6.7 | mA | |
| I_{CC} | Supply current (average per receiver) | | $V_{IC} = 15\text{ V}$, | $V_{ID} = -1\text{ V}$ | | 4.2 | 6 | mA |
| | | | $V_{IC} = 0$, | $V_{ID} = -0.5\text{ V}$ | | 6.8 | 10.2 | |
| | | | $V_{IC} = -15\text{ V}$, | $V_{ID} = -1\text{ V}$ | | 9.4 | 14 | |

(1) Unless otherwise noted, $V_{(STRB)} \geq 2.1\text{ V}$ or open.

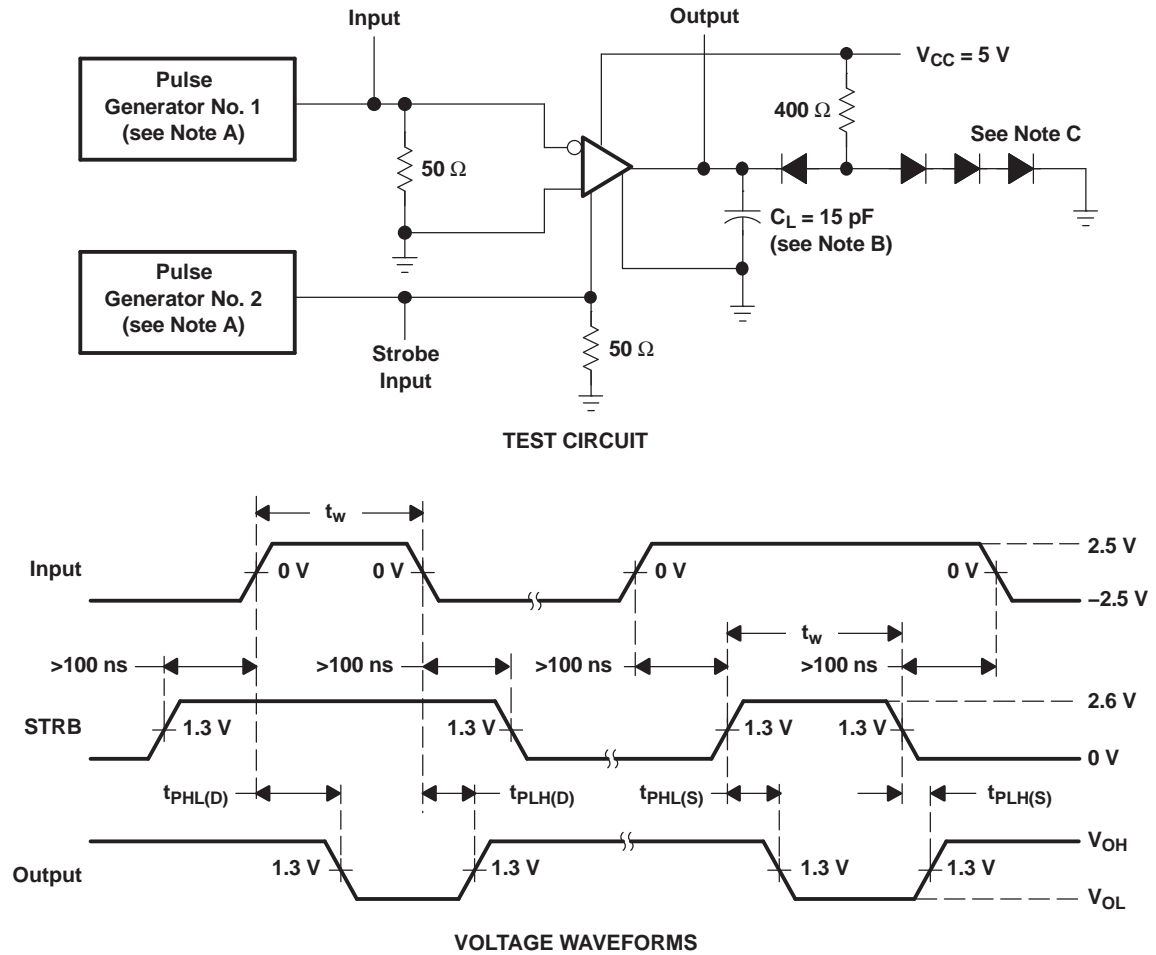
(2) All typical values are at $V_{CC} = 5\text{ V}$, $V_{IC} = 0$, and $T_A = 25^\circ\text{C}$.

SWITCHING CHARACTERISTICS

 $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--------------|---|-----------------------|---|-----|-----|-----|------|
| $t_{PLH(D)}$ | Propagation delay time, low- to high-level output from differential input | $R_L = 400\ \Omega$, | $C_L = 15\text{ pF}$, See Figure 1 | | 18 | 40 | ns |
| $t_{PHL(D)}$ | Propagation delay time, high- to low-level output from differential input | $R_L = 400\ \Omega$, | $C_L = 15\text{ pF}$, See Figure 1 | | 31 | 45 | ns |
| $t_{PLH(S)}$ | Propagation delay time, low- to high-level output from STRB input | $R_L = 400\ \Omega$, | $C_L = 15\text{ pF}$, See Figure 1 | | 9 | 30 | ns |
| $t_{PHL(S)}$ | Propagation delay time, high- to low-level output from STRB input | $R_L = 400\ \Omega$, | $C_L = 15\text{ pF}$, See Figure 1 | | 15 | 25 | ns |

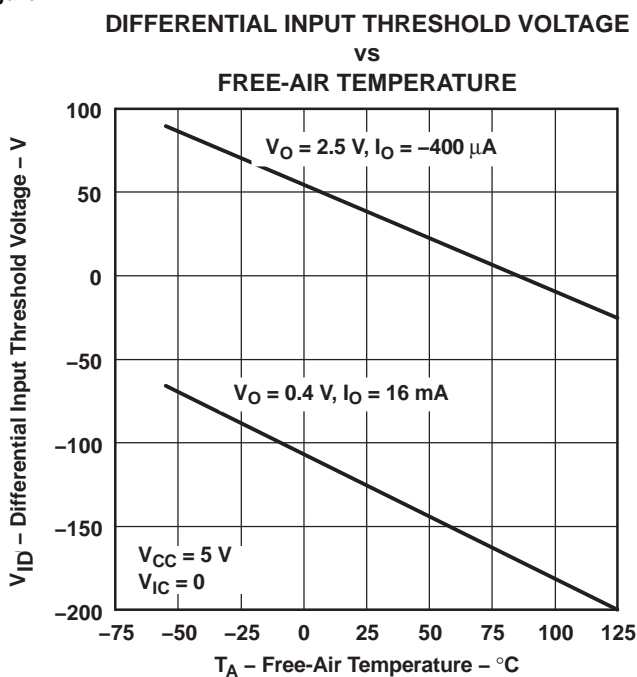
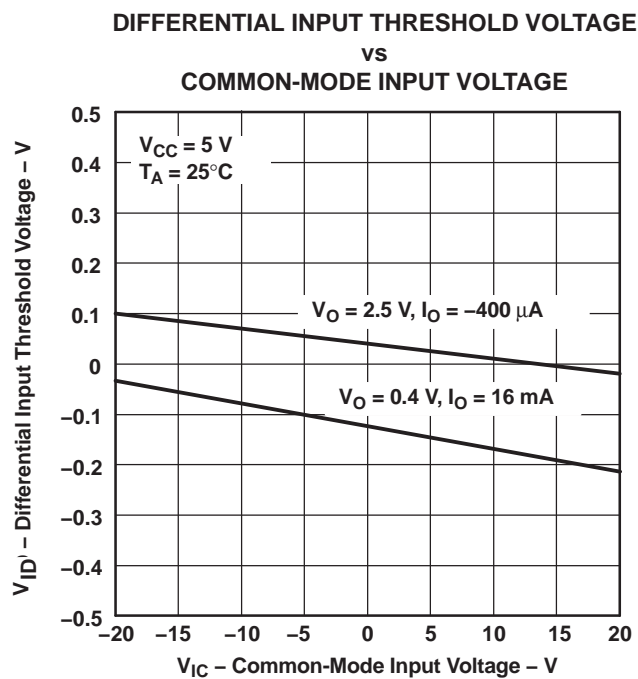
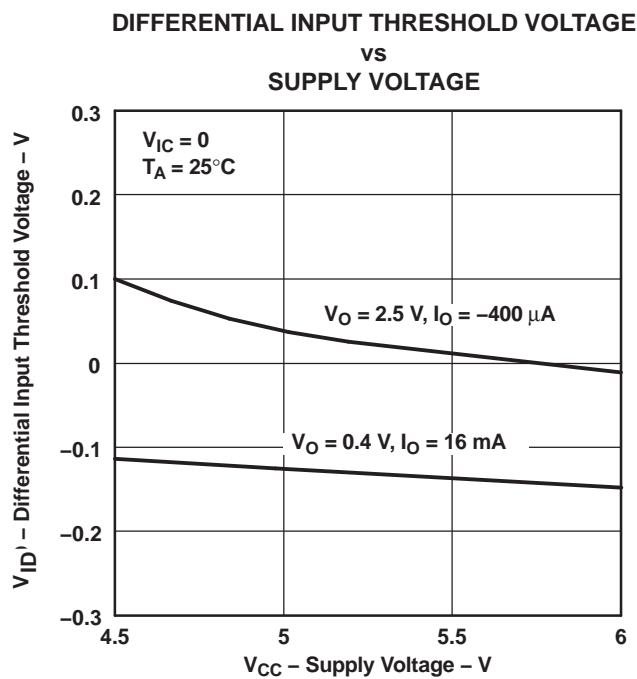
PARAMETER MEASUREMENT INFORMATION



- A. The pulse generators have the following characteristics: $Z_O = 50 \Omega$, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$, $t_w = 0.5 \pm 0.1 \mu\text{s}$, $\text{PRR} \leq 1 \text{ MHz}$.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS⁽¹⁾



(1) Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

TYPICAL CHARACTERISTICS⁽¹⁾

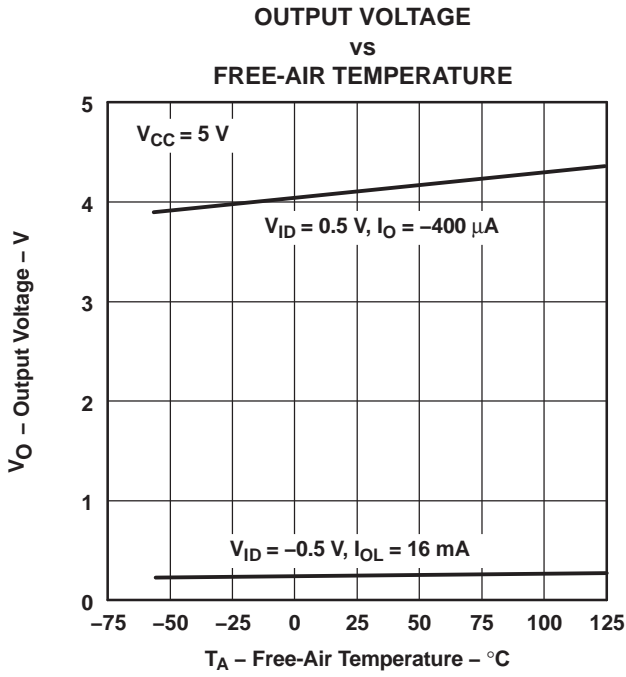


Figure 5.

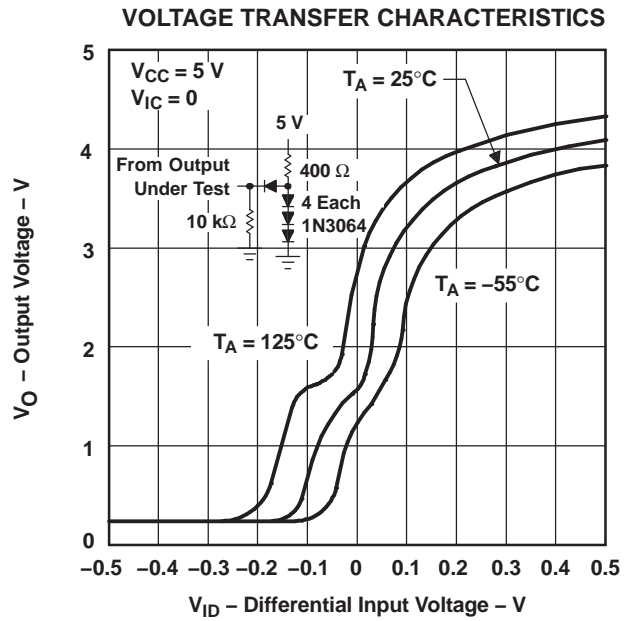


Figure 6.

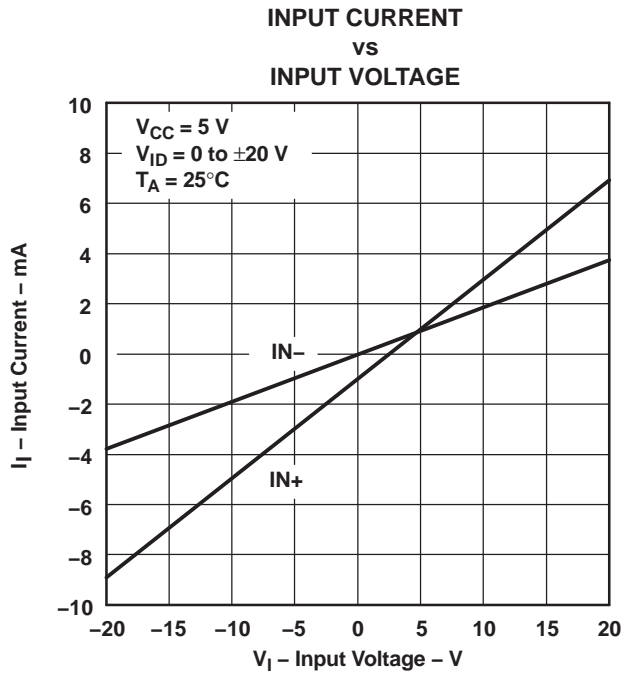


Figure 7.

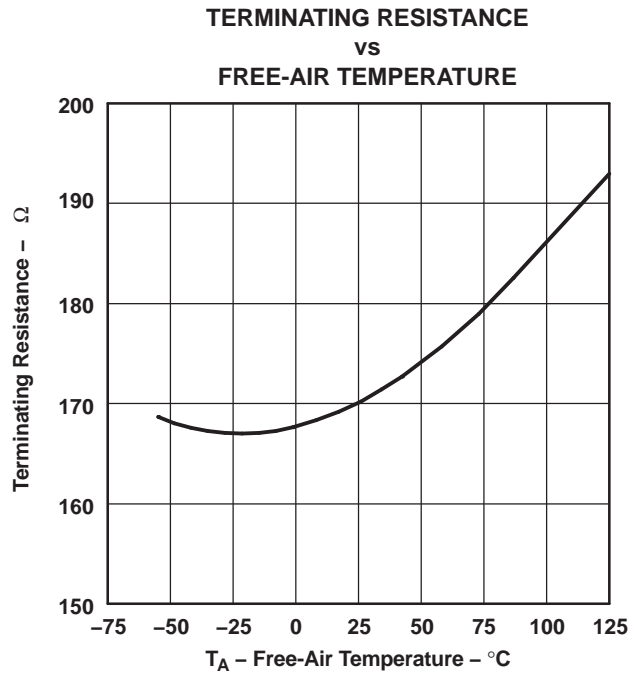
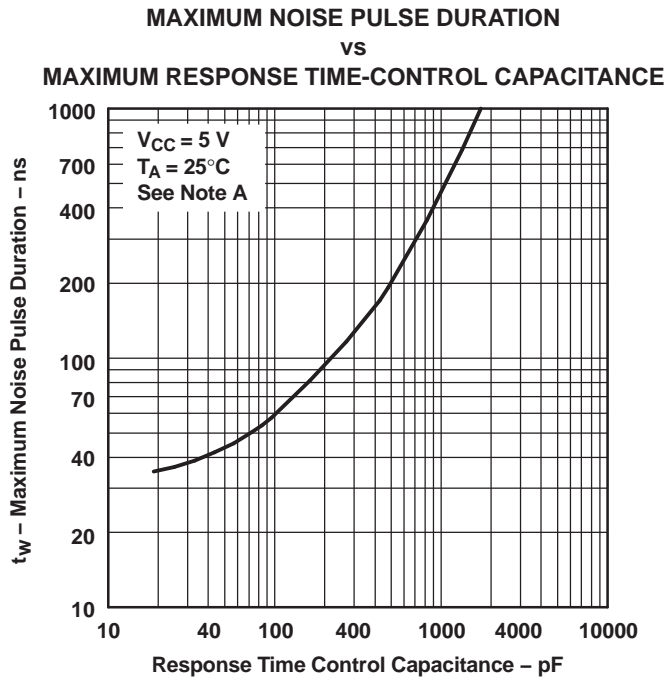
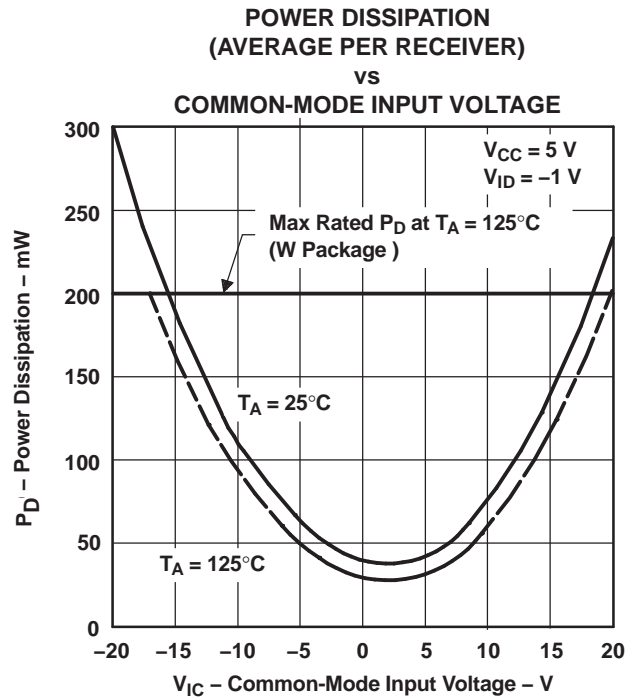
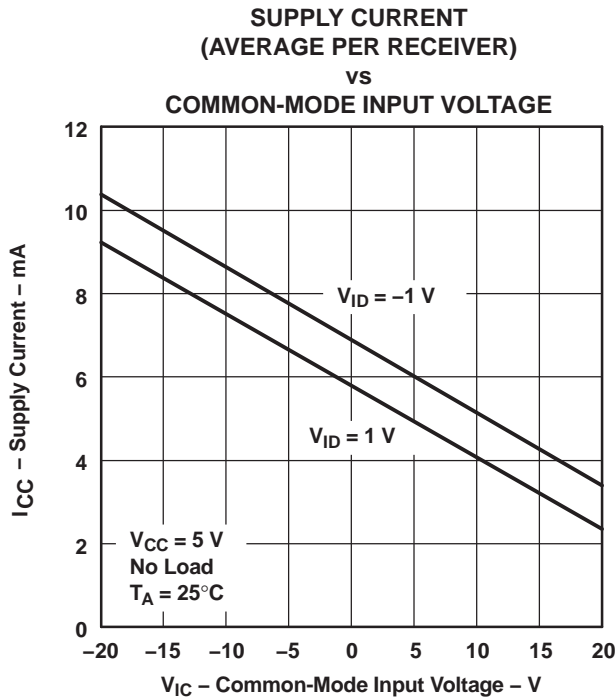


Figure 8.

(1) Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

TYPICAL CHARACTERISTICS⁽¹⁾



A. Figure 11 shows the maximum duration of the illustrated pulse that can be applied differently without the output changing from the low to high level.

Figure 11.

(1) Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

TYPICAL CHARACTERISTICS⁽¹⁾

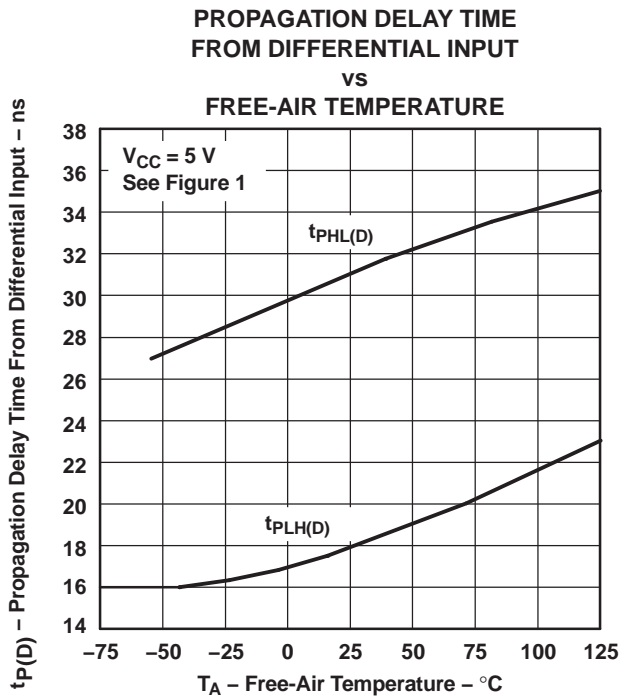


Figure 12.

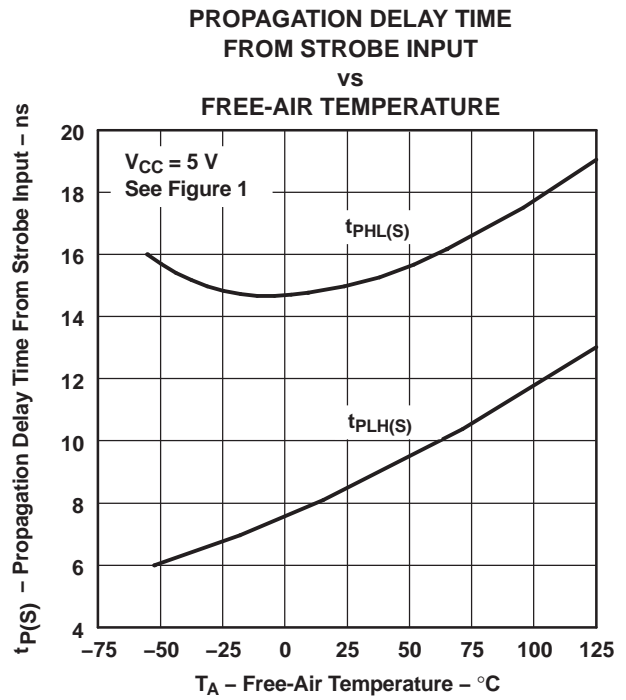
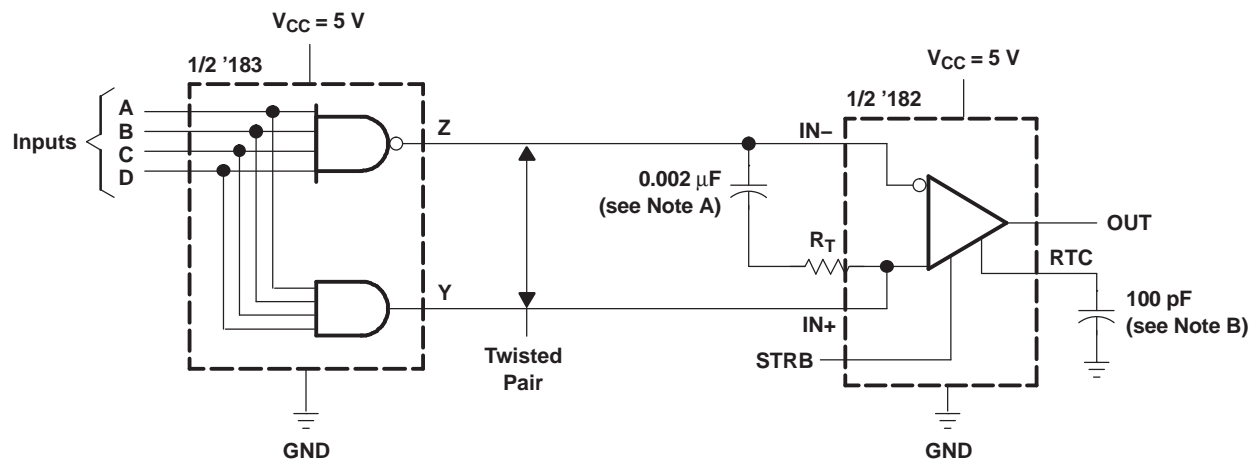


Figure 13.

(1) Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

APPLICATION INFORMATION



NOTES: A. When the inputs are open circuited, the output is high. A capacitor may be used for dc isolation of the line-terminating resistor. At the frequency of operation, the impedance of the capacitor should be relatively small.

Example: let $f = 5 \text{ MHz}$
 $C = 0.002 \mu\text{F}$

$$Z_{(C)} = \frac{1}{2\pi f C} = \frac{1}{2\pi(5 \times 10^6)(0.002 \times 10^{-6})}$$

$$Z_{(C)} \approx 16\Omega$$

B. Use of a capacitor to control response time is optional.

Figure 14. Transmission of Digital Data Over Twisted-Pair Line

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-7900801VCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| 5962-7900801VDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN55182-SP :

- Catalog: [SN55182](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

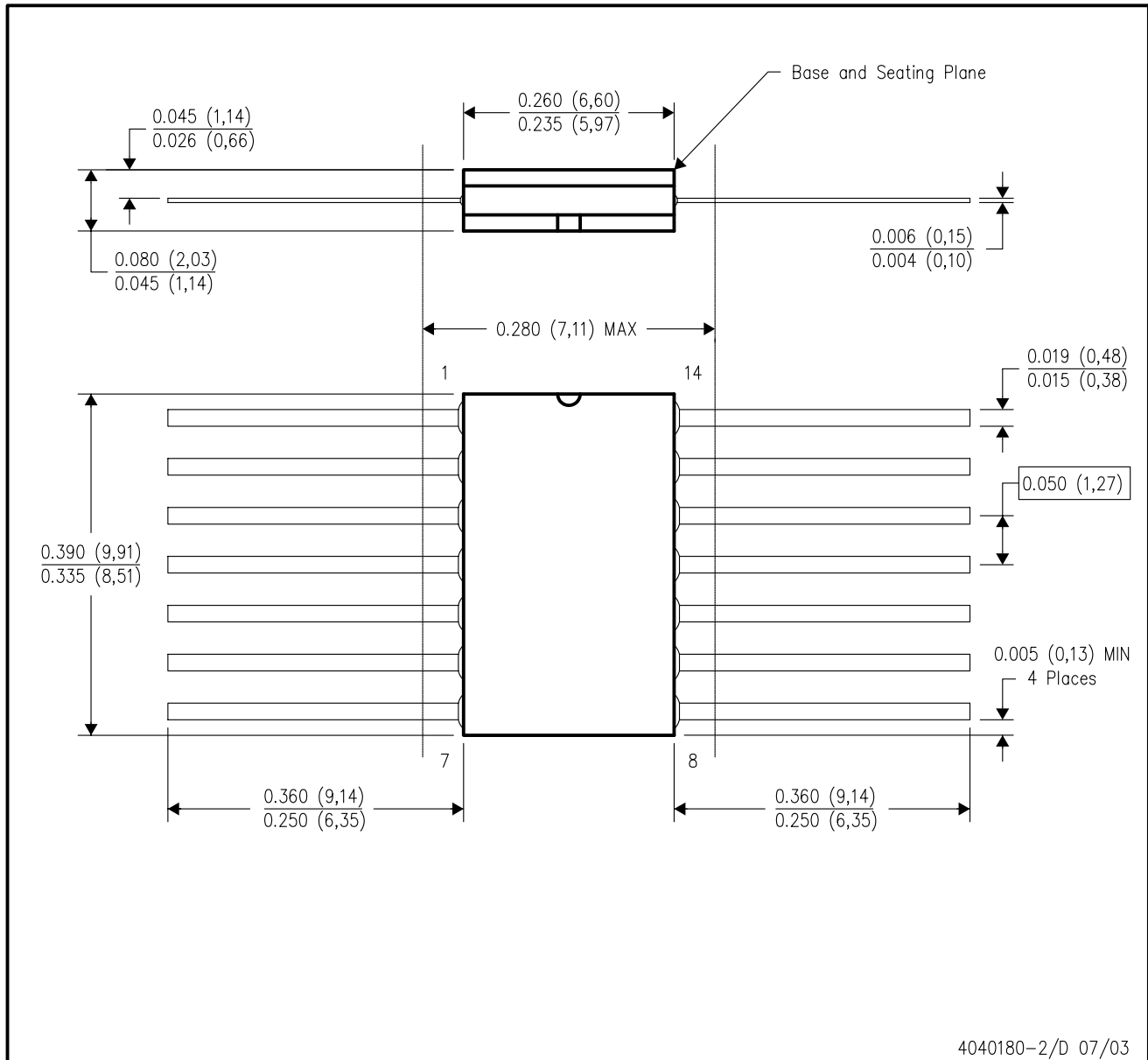


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

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