10-MHz To 66-MHz, 10:1 LVDS SERIALIZER/DESERIALIZER

Check for Samples: SN65LV1023A SN65LV1224B

FEATURES

- **100-Mbps to 660-Mbps Serial LVDS Data Payload Bandwidth at 10-MHz to 66-MHz System Clock**
- **Pin-Compatible Superset of DS92LV1023/DS92LV1224**
- **Chipset (Serializer/Deserializer) Power Consumption <450 mW (Typ) at 66 MHz**
- **Synchronization Mode for Faster Lock**
- **Lock Indicator**
- **No External Components Required for PLL**
- **28-Pin SSOP and Space Saving 5 × 5 mm QFN Packages Available**
- **Industrial Temperature Qualified, T_A = −40°C to 85°C**
- **Programmable Edge Trigger on Clock**
- **Flow-Through Pinout for Easy PCB Layout**

APPLICATIONS

- **Wireless Base Station**
- **Backplane Interconnect**
- **DSLAM**

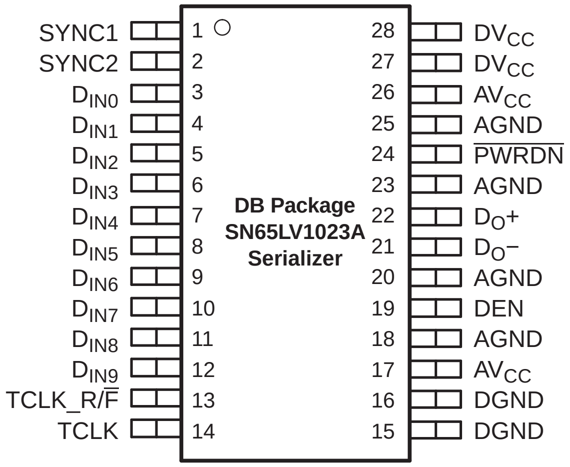
DESCRIPTION

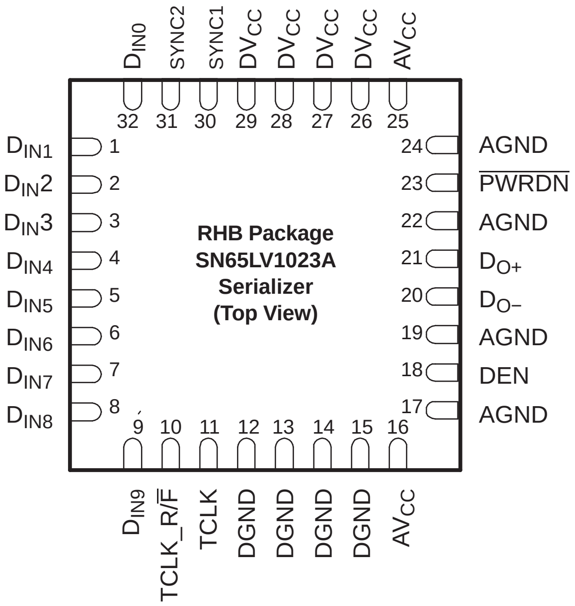
The SN65LV1023A serializer and SN65LV1224B deserializer comprise a 10-bit serdes chipset designed to transmit and receive serial data over LVDS differential backplanes at equivalent parallel word rates from 10 MHz to 66 MHz. Including overhead, this translates into a serial data rate between 120-Mbps and 792-Mbps payload encoded throughput.

Upon power up, the chipset link can be initialized via a synchronization mode with internally generated SYNC patterns or the deserializer can be allowed to synchronize to random data. By using the synchronization mode, the deserializer establishes lock within specified, shorter time parameters.

The device can be entered into a power-down state when no data transfer is required. Alternatively, a mode is available to place the output pins in the high-impedance state without losing PLL lock.

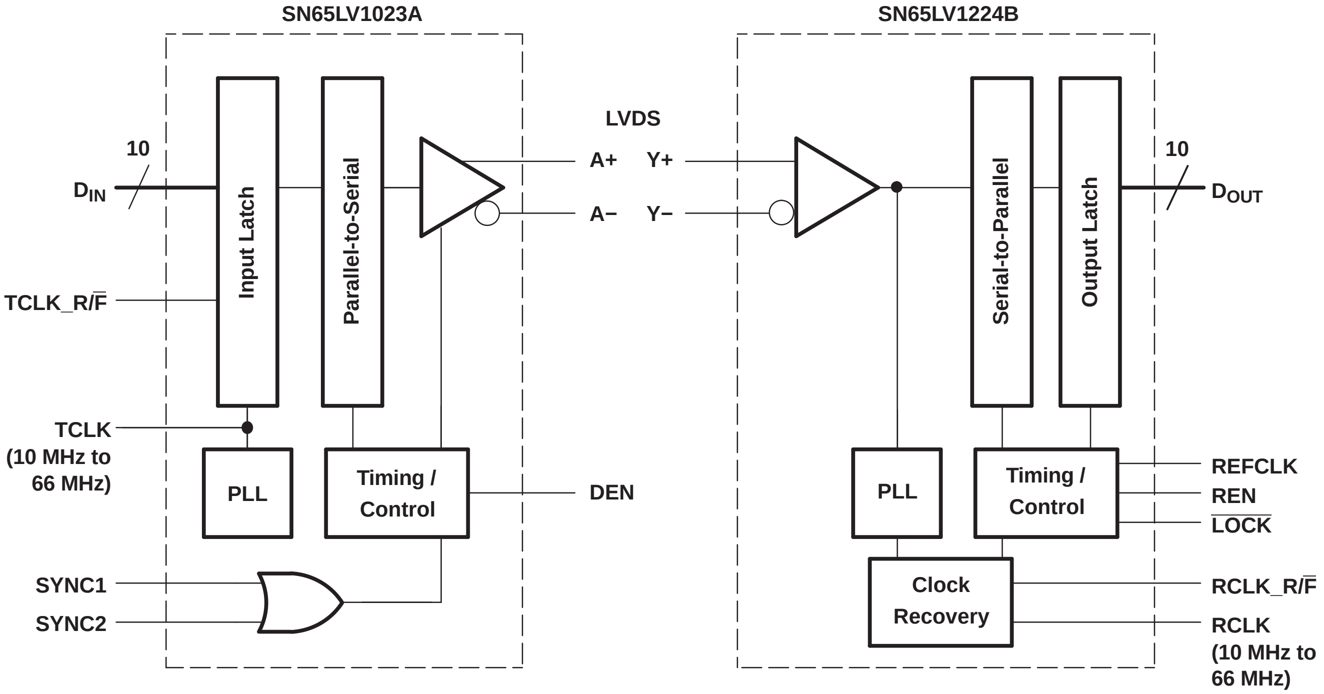
The SN65LV1023A and SN65LV1224B are characterized for operation over ambient air temperature of –40°C to 85°C.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

BLOCK DIAGRAMS



FUNCTIONAL DESCRIPTION

The SN65LV1023A and SN65LV1224B are a 10-bit serializer/deserializer chipset designed to transmit data over differential backplanes or unshielded twisted pair (UTP) at clock speeds from 10 MHz to 66 MHz. The chipset has five states of operation: initialization mode, synchronization mode, data transmission mode, power-down mode, and high-impedance mode. The following sections describe each state of operation.

INITIALIZATION MODE

Initialization of both devices must occur before data transmission can commence. Initialization refers to synchronization of the serializer and deserializer PLLs to local clocks.

When V_{CC} is applied to the serializer and/or deserializer, the respective outputs enter the high-impedance state, while on-chip power-on circuitry disables internal circuitry. When V_{CC} reaches 2.45 V, the PLL in each device begins locking to a local clock. For the serializer, the local clock is the transmit clock (TCLK) provided by an external source. For the deserializer, a local clock must be applied to the REFCLK pin. The serializer outputs remain in the high-impedance state, while the PLL locks to the TCLK.

SYNCHRONIZATION MODE

The deserializer PLL must synchronize to the serializer in order to receive valid data. Synchronization can be accomplished in one of two ways:

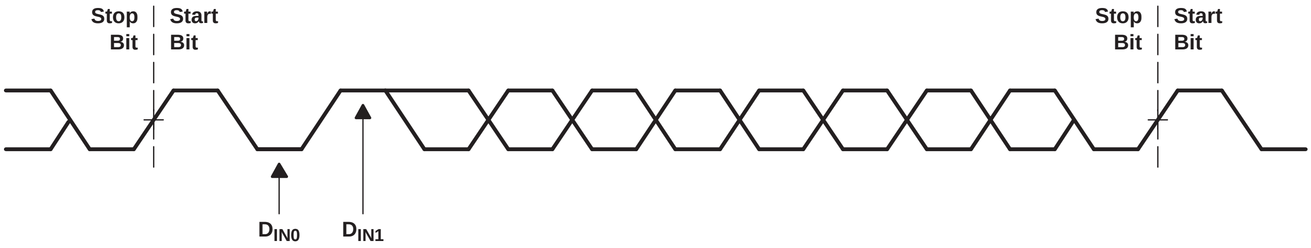
- **Rapid Synchronization:** The serializer has the capability to send specific SYNC patterns consisting of six ones and six zeros switching at the input clock rate. The transmission of SYNC patterns enables the deserializer to lock to the serializer signal within a deterministic time frame. This transmission of SYNC patterns is selected via the SYNC1 and SYNC2 inputs on the serializer. Upon receiving valid SYNC1 or SYNC2 pulse (wider than 6 clock cycles), 1026 cycles of SYNC pattern are sent.

  When the deserializer detects *edge* transitions at the LVDS input, it attempts to lock to the embedded clock information. The deserializer LOCK output remains high while its PLL locks to the incoming data or SYNC patterns present on the serial input. When the deserializer locks to the LVDS data, the LOCK output goes low. When LOCK is low, the deserializer outputs represent incoming LVDS data. One approach is to tie the deserializer LOCK output directly to SYNC1 or SYNC2.
- **Random-Lock Synchronization:** The deserializer can attain lock to a data stream without requiring the serializer to send special SYNC patterns. This allows the SN65LV1224B to operate in open-loop applications. Equally important is the deserializer's ability to support hot insertion into a running backplane. In the open-loop or hot-insertion case, it is assumed the data stream is essentially random. Therefore, because lock time varies due to data stream characteristics, the exact lock time cannot be predicted. The primary constraint on the random lock time is the initial phase relation between the incoming data and the REFCLK when the deserializer powers up.

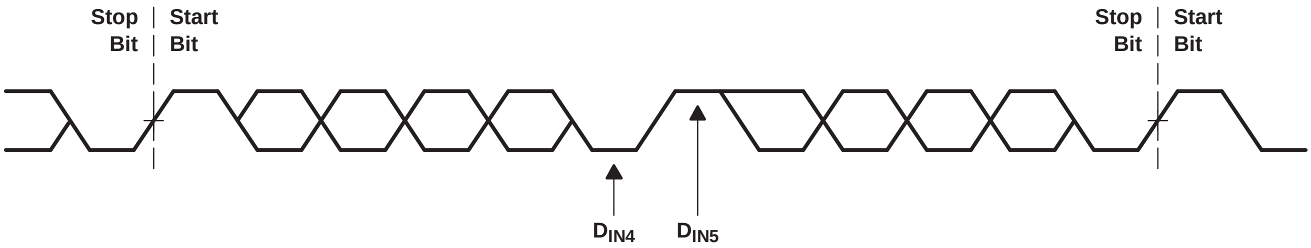
The data contained in the data stream can also affect lock time. If a specific pattern is repetitive, the deserializer could enter false lock—falsely recognizing the data pattern as the start/stop bits. This is referred to as repetitive multitransition (RMT); see Figure 1 for RMT examples. This occurs when more than one low-high transition takes place per clock cycle over multiple cycles. In the worst case, the deserializer could become locked to the data pattern rather than the clock. Circuitry within the deserializer can detect that the possibility of false lock exists. Upon detection, the circuitry prevents the LOCK output from becoming active until the potential false lock pattern changes. Notice that the RMT pattern only affects the deserializer lock time, and once the deserializer is in lock, the RMT pattern does not affect the deserializer state as long as the same data boundary happens each cycle. The deserializer does not go into lock until it finds a unique four consecutive cycles of data boundary (stop/start bits) at the same position.

The deserializer stays in lock until it cannot detect the same data boundary (stop/start bits) for four consecutive cycles. Then the deserializer goes out of lock and hunts for the new data boundary (stop/start bits). In the event of loss of synchronization, the LOCK pin output goes high and the outputs (including RCLK) enter a high-impedance state. The user's system should monitor the LOCK pin in order to detect a loss of synchronization. Upon detection of loss of lock, sending sync patterns for resynchronization is desirable if reestablishing lock within a specific time is critical. However, the deserializer can lock to random data as previously noted.

D_{IN0} Held Low and D_{IN1} Held High



D_{IN4} Held Low and D_{IN5} Held High



D_{IN8} Held Low and D_{IN9} Held High

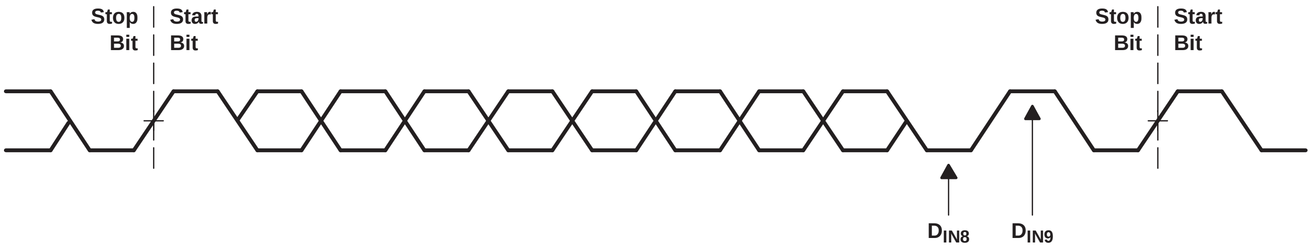


Figure 1. RMT Pattern Examples

DATA TRANSMISSION MODE

After initialization and synchronization, the serializer accepts parallel data from inputs D_{IN0}–D_{IN9}. The serializer uses the TCLK input to latch the incoming data. The TCLK_R/$\overline{\text{F}}$ pin selects which edge the serializer uses to strobe incoming data. If either of the SYNC inputs is high for six TCLK cycles, the data at D_{IN0}−D_{IN9} is ignored regardless of the clock edge selected and 1026 cycles of SYNC pattern are sent.

After determining which clock edge to use, a start and stop bit, appended internally, frames the data bits in the register. The start bit is always high and the stop bit is always low. The start and stop bits function as the embedded clock bits in the serial stream.

The serializer transmits serialized data and appended clock bits (10+2 bits) from the serial data output (DO±) at 12 times the TCLK frequency. For example, if TCLK is 66 MHz, the serial rate is 66 × 12 = 792 Mbps. Because only 10 bits are input data, the useful data rate is 10 times the TCLK frequency. For instance, if TCLK = 66 MHz, the useful data rate is 66 × 10 = 660 Mbps. The data source, which provides TCLK, must be in the range of 10 MHz to 66 MHz.

The serializer outputs (DO±) can drive point-to-point connections or limited multipoint or multidrop backplanes. The outputs transmit data when the enable pin (DEN) is high, $\overline{\text{PWRDN}}$ = high, and SYNC1 and SYNC2 are low. When DEN is driven low, the serializer output pins enter the high-impedance state.

Once the deserializer has synchronized to the serializer, the $\overline{\text{LOCK}}$ pin transitions low. The deserializer locks to the embedded clock and uses it to recover the serialized data. ROUT data is valid when $\overline{\text{LOCK}}$ is low, otherwise R_{OUT0}–R_{OUT9} is invalid. The R_{OUT0}–R_{OUT9} data is strobed out by RCLK. The specific RCLK edge polarity to be used is selected by the RCLK_R/F input. The R_{OUT0}–R_{OUT9}, $\overline{\text{LOCK}}$ and RCLK outputs can drive a maximum of three CMOS input gates (15-pF load. total for all three) with a 66-MHz clock.

POWER DOWN

When no data transfer is required, the power-down mode can be used. The serializer and deserializer use the power-down state, a low-power sleep mode, to reduce power consumption. The deserializer enters power down when you drive $\overline{\text{PWRDN}}$ and REN low. The serializer enters power down when you drive $\overline{\text{PWRDN}}$ low. In power down, the PLL stops and the outputs enter a high-impedance state, which disables load current and reduces supply current to the milliampere range. To exit power down, you must drive the $\overline{\text{PWRDN}}$ pin high.

Before valid data exchanges between the serializer and deserializer can resume, you must reinitialize and resynchronize the devices to each other. Initialization of the serializer takes 1026 TCLK cycles. The deserializer initialize and drives $\overline{\text{LOCK}}$ high until lock to the LVDS clock occurs.

HIGH-IMPEDANCE MODE

The serializer enters the high-impedance mode when the DEN pin is driven low. This puts both driver output pins (DO+ and DO−) into a high-impedance state. When you drive DEN high, the serializer returns to the previous state, as long as all other control pins remain static (SYNC1, SYNC2, $\overline{\text{PWRDN}}$, TCLK_R/$\overline{\text{F}}$). When the REN pin is driven low, the deserializer enters high-impedance mode. Consequently, the receiver output pins (R_{OUT0}–R_{OUT9}) and RCLK are placed into the high-impedance state. The $\overline{\text{LOCK}}$ output remains active, reflecting the state of the PLL.

Table 1. Deserializer Truth Table

INPUTS		OUTPUTS		
$\overline{\text{PWRDN}}$	**REB**	**ROUT(0:9)**(1)	**$\overline{\text{LOCK}}$** (2)	**RCLK**(3) (1)
H	H	Z	H	Z
H	H	Active	L	Active
L	X	Z	Z	Z
H	L	Z	Active	Z

(1) ROUT and RCLK are 3-stated when $\overline{\text{LOCK}}$ is asserted high.
(2) $\overline{\text{LOCK}}$ output reflects the state of the deserializer with regard to the selected data stream.
(3) RCLK active indicates the RCLK is running if the deserializer is locked. The timing of RCLK with respect to ROUT is determined by RCLK_R/$\overline{\text{F}}$.

FAILSAFE BIASING FOR THE SN65LV1224B

The SN65LV1224B has an input threshold sensitivity of ±50 mV. This allows for greater differential noise margin in the SN65LV1224B. However, in cases where the receiver input is not being actively driven, the increased sensitivity of the SN65LV1224B can pickup noise as a signal and cause unintentional locking. This may occur when the input cable is disconnected. The SN65LV1224B has an on-chip fail-safe circuit that drives the serial input and $\overline{\text{LOCK}}$ signal high. The response time of the fail-safe circuit depends on interconnect characteristics.

PIN FUNCTIONS

PIN		I/O	DESCRIPTION
DB PACKAGE	RHB PACKAGE		
SERIALIZER			
18, 20, 23, 25	17, 19, 22, 24	AGND	Analog circuit ground (PLL and analog circuits)
17, 26	16, 25	AV_{CC}	Analog circuit power supply (PLL and analog circuits)
19	18	DEN	LVTTL logic input. Low puts the LVDS serial output into the high-impedance state. High enables serial data output.
15, 16	12, 13, 14, 15	DGND	Digital circuit ground
3−12	32, 1−9	D_{IN0} − D_{IN9}	Parallel LVTTL data inputs
21	20	D_O−	Inverting LVDS differential output
22	21	D_O+	Noninverting LVDS differential output
27, 28	26, 27, 28, 29	DV_{CC}	Digital circuit power supply
24	23	$\overline{\text{PWRDN}}$	LVTTL logic input. Asserting this pin low turns off the PLL and places the outputs into the high-impedance state, putting the device into a low-power mode.
1, 2	30, 31	SYNC1, SYNC2	LVTTL logic inputs SYNC1 and SYNC2 are ORed together. When at least one of the two pins is asserted high for 6 cycles of TCLK, the serializer initiates transmission of a minimum 1026 SYNC patterns. If after completion of the transmission of 1026 patterns SYNC continues to be asserted, then the transmission continues until SYNC is driven low and if the time SYNC holds > 6 cycles, another 1026 SYNC pattern transmission initiates.
13	10	TCLK_R/$\overline{\text{F}}$	LVTTL logic input. Low selects a TCLK falling-edge data strobe; high selects a TCLK rising-edge data strobe.
14	11	TCLK	LVTTL-level reference clock input. The SN65LV1023A accepts a 10-MHz to 66-MHz clock. TCLK strobes parallel data into the input latch and provides a reference frequency to the PLL.
DESERIALIZER			
1, 12, 13	10, 11, 28, 29, 30	AGND	Analog circuit ground (PLL and analog circuits)
4, 11	1, 8, 9	AV_{CC}	Analog circuit power supply (PLL and analog circuits)
14, 20, 22	12, 13, 19, 21	DGND	Digital circuit ground
21, 23	20, 22	DV_{CC}	Digital circuit power supply
10	7	$\overline{\text{LOCK}}$	LVTTL level output. $\overline{\text{LOCK}}$ goes low when the deserializer PLL locks onto the embedded clock edge.
7	4	$\overline{\text{PWRDN}}$	LVTTL logic input. Asserting this pin low turns off the PLL and places outputs into a high-impedance state, putting the device into a low-power mode. To initiate power down, this pin is held low for a minimum of 16 ns. As long as $\overline{\text{PWRDN}}$ is held low, the device is in the power down state.
2	31	RCLK_R/$\overline{\text{F}}$	LVTTL logic input. Low selects an RCLK falling-edge data strobe; high selects an RCLK rising-edge data strobe.
9	6	RCLK	LVTTL level output recovered clock. Use RCLK to strobe ROUTx.
3	32	REFCLK	LVTTL logic input. Use this pin to supply a REFCLK signal for the internal PLL frequency.
8	5	REN	LVTTL logic input. Low places R_{OUT0}−R_{OUT9} and RCLK in the high-impedance state.
5	2	R_I+	Serial data input. Noninverting LVDS differential input
6	3	R_I–	Serial data input. Inverting LVDS differential input
28−24, 19−15	27−23, 18−14	R_{OUT0}−R_{OUT9}	Parallel LVTTL data outputs

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
V_{CC} to GND		−0.3 V to 4 V
LVTTL input voltage		−0.3 V to (V_{CC} + 0.3 V)
LVTTL output voltage		−0.3 V to (V_{CC} + 0.3 V)
LVDS receiver input voltage		−0.3 V to 3.9 V
LVDS driver output voltage		−0.3 V to 3.9 V
LVDS output short circuit duration		10 ms
Electrostatic discharge:	HBM	up to 6 kV
	MM	up to 200 V
Junction temperature		150°C
Storage temperature		−65°C to 150°C
DB package maximum package power dissipation	T_A = 25°C	1.27 W
RHB package maximum package power dissipation	T_A = 25°C	2.85 W
DB package derating		10.3 mW/°C above 25°C
RHB package derating		23.6 mW/°C above 25°C

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(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC} (1)	Supply voltage	3	3.3	3.6	V
	Receiver input voltage range	0		2.4	V
V_{CM}	Receiver input common mode range	$\frac{V_{ID}}{2}$		$2.4 - \left(\frac{V_{ID}}{2}\right)$	V
	Supply noise voltage			100	mV_{PP}
T_A	Operating free-air temperature	–40	25		°C

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(1) By design, DVCC and AVCC are separated internally and does not matter what the difference is for |DVCC−AVCC|, as long as both are within 3 V to 3.6 V.

ELECTRICAL CHARACTERISTICS

over recommended operating supply and temperature ranges (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SERIALIZER LVCMOS/LVTTL DC SPECIFICATIONS[1]							
V_{IH}	High-level input voltage			2		V_{CC}	V
V_{IL}	Low-level input voltage			GND		0.8	V
V_{CL}	Input clamp voltage	I_{CL} = −18 mA			-0.86	–1.5	V
I_{IN}	Input current, [2]	V_{IN} = 0 V or 3.6 V		–200	±100	200	µA
DESERIALIZER LVCMOS/LVTTL DC SPECIFICATIONS[3]							
V_{IH}	High-level input voltage			2		V_{CC}	V
V_{IL}	Low-level input voltage			GND		0.8	V
V_{CL}	Input clamp voltage	I_{CL} = −18 mA			-0.62	–1.5	V
I_{IN}	Input current (pull-up and pull-down resistors on inputs)	V_{IN} = 0 V or 3.6 V		–200		200	µA
V_{OH}	High-level output voltage	I_{OH} = −5 mA		2.2	3	V_{CC}	V
V_{OL}	Low-level output voltage	I_{OL} = 5 mA		GND	0.25	0.5	V
I_{OS}	Output short-circuit current	V_{OUT} = 0 V		–15	–47	–85	mA
I_{OZ}	High-impedance output current	$\overline{\text{PWRDN}}$ or REN = 0.8 V, V_{OUT} = 0 V or V_{CC}		–10	±1	10	µA
SERIALIZER LVDS DC SPECIFICATIONS (Apply to Pins DO+ and DO−)							
V_{OD}	Output differential voltage (DO+)–(DO−)	R_L = 27 Ω, See Figure 2		350	450		mV
ΔV_{OD}	Output differential voltage unbalance					35	mV
V_{OS}	Offset voltage			1.1	1.2	1.3	V
ΔV_{OS}	Offset voltage unbalance				4.8	35	mV
I_{OS}	Output short circuit current	D0 = 0 V, D_{INx} = high, $\overline{\text{PWRDN}}$ and DEN = 2.4 V			-10	-90	mA
I_{OZ}	High-impedance output current	$\overline{\text{PWRDN}}$ or DEN = 0.8 V, DO = 0 V or V_{CC}		–10	±1	10	µA
I_{OX}	Power-off output current	V_{CC} = 0 V, DO = 0 V or 3.6 V		-20	±1	25	µA
C_O	Output single-ended capacitance					1±20%	pF
DESERIALIZER LVDS DC SPECIFICATIONS (Apply to Pins RI+ and RI−)							
V_{TH}	Differential threshold high voltage	V_{CM} = 1.1 V				50	mV
V_{TL}	Differential threshold low voltage			–50			mV
I_{IN}	Input current	V_{IN} = 2.4 V, V_{CC} = 3.6 V or 0 V		–10	±1	15	µA
		V_{IN} = 0 V, V_{CC} = 3.6 V or 0 V		–10	±0.05	10	
C_I	Input single-ended capacitance					0.5±20%	pF
SERIALIZER SUPPLY CURRENT (Applies to Pins DVCC and AVCC)							
I_{CCD}	Serializer supply current worst case	R_L = 27 Ω, See Figure 5	f = 10 MHz		20	25	mA
			f = 66 MHz		55	70	
I_{CCXD}	Serializer supply current	$\overline{\text{PWRDN}}$ = 0.8 V			200	500	µA
DESERIALIZER SUPPLY CURRENT (applies to pins DVCC and AVCC)							
I_{CCR}	Deserializer supply current, worst case	C_L = 15 pF, See Figure 5	f = 10 MHz		15	35	mA
			f = 66 MHz		80	95	
I_{CCXR}	Deserializer supply current, power down	$\overline{\text{PWRDN}}$ = 0.8 V, REN = 0.8 V			0.36	1	mA

(1) Apply to D_{IN0}–D_{IN9}, TCLK, $\overline{\text{PWRDN}}$, TCLK_R/$\overline{\text{F}}$, SYNC1, SYNC2, and DEN
(2) High I_{IN} values are due to pullup and pulldown resistors on the inputs.
(3) Apply to pins $\overline{\text{PWRDN}}$, RCLK_R/$\overline{\text{F}}$, REN, and REFCLK = inputs; apply to pins R_{OUTx}, RCLK, and $\overline{\text{LOCK}}$ = outputs

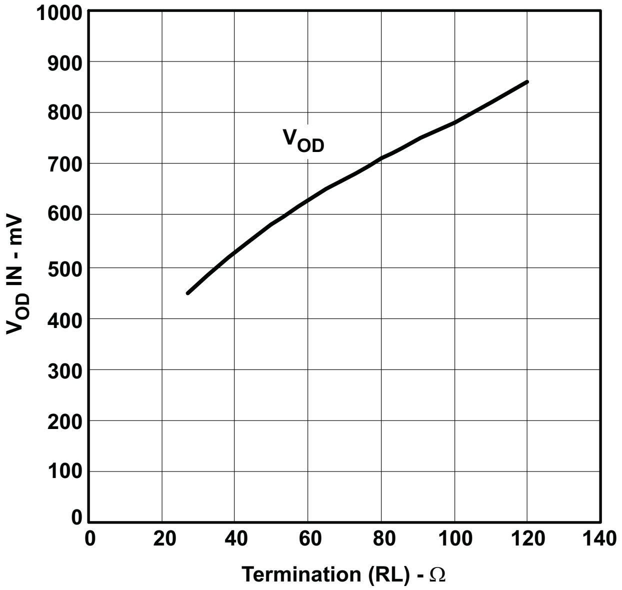


Figure 2. Typical V_{OD} Curve

SERIALIZER TIMING REQUIREMENTS FOR TCLK

over recommended operating supply and temperature ranges (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{TCP}	Transmit clock period		15.15	T	100	ns
t_{TCIH}	Transmit clock high time		0.4T	0.5T	0.6T	ns
t_{TCIL}	Transmit clock low time		0.4T	0.5T	0.6T	ns
$t_{t(CLK)}$	TCLK input transition time			3	6	ns
t_{JIT}	TCLK input jitter	See Figure 19			150	ps (RMS)
	Frequency tolerance		-100		+100	ppm

SERIALIZER SWITCHING CHARACTERISTICS

over recommended operating supply and temperature ranges (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{TLH(L)}$	LVDS low-to-high transition time	R_L = 27 Ω, C_L = 10 pF to GND, See Figure 6		0.2	0.4	ns
$t_{LTHL(L)}$	LVDS high-to-low transition time			0.25	0.4	ns
$t_{su(DI)}$	DIN0−DIN9 setup to TCLK	See Figure 9	0.5			ns
$t_{su(DI)}$	DIN0−DIN9 hold from TCLK		4			ns
$t_{d(HZ)}$	DO± high-to-high impedance state delay	R_L = 27 Ω, C_L = 10 pF to GND, See Figure 10		2.5	5	ns
$t_{d(LZ)}$	DO± low-to-high impedance state delay			2.5	5	
$t_{d(ZH)}$	DO± high-to-high impedance state-to-high delay			5	10	
$t_{d(ZL)}$	DO± high-to-high impedance state-to-low delay			6.5	10	
$t_{w(SPW)}$	SYNC pulse duration	See Figure 12	6×t_{TCP}			ns
$t_{(PLD)}$	Serializer PLL lock time		1026×t_{TCP}			ns
$t_{d(S)}$	Serializer delay	See Figure 13	t_{TCP}+1	t_{TCP}+2	t_{TCP}+3	ns
t_{DJIT}	Deterministic jitter	RL = 27 Ω, C_L = 10 pF to GND			230	ps
					150	
t_{RJIT}	Random jitter	RL = 27 Ω, C_L = 10 pF to GND		10	19	ps (RMS)

DESERIALIZER TIMING REQUIREMENTS FOR REFCLK

over recommended operating supply and temperature ranges (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RFCP}	REFCLK period		15.15	T	100	ns
t_{RFDC}	REFCLK duty cycle		30%	50%	70%	
$t_{t(RF)}$	REFCLK transition time			3	6	ns
	Frequency tolerance		-100		+100	ppm

DESERIALIZER SWITCHING CHARACTERISTICS

over recommended operating supply and temperature ranges (unless otherwise specified)

PARAMETER		TEST CONDITIONS	PIN/FREQ	MIN	TYP	MAX	UNIT
$t_{(RCP)}$	Receiver out clock period	$t_{(RCP)} = t_{(TCP)}$, See Figure 13	RCLK	15.15		100	ns
$t_{TLH(C)}$	CMOS/TTL low-to-high transition time	C_L = 15 pF, CL = 15 pF, See Figure 7	ROUT0−ROUT9 $\overline{\text{LOCK}}$, RCLK		1.2	2.5	ns
$t_{THL(C)}$	CMOS/TTL high-to-low transition time				1.1	2.5	
$t_{d(D)}$	Deserializer delay, See Figure 14	Room temperature, 3.3 V	10 MHz	1.75×$t_{(RCP)}$ +4.2		1.75×$t_{(RCP)}$ +12.6	ns
			66 MHz	1.75×$t_{(RCP)}$ +7.4		1.75×$t_{(RCP)}$ +9.7	ns
$t_{(ROS)}$	R_{OUTx} data valid before RCLK	See Figure 15	RCLK 10 MHz	0.4×$t_{(RCP)}$	0.5×$t_{(RCP)}$		ns
			RCLK 66 MHz	0.4×$t_{(RCP)}$	0.5×$t_{(RCP)}$		
$t_{(ROH)}$	R_{OUTx} data valid after RCLK		10 MHz	−0.4×$t_{(RCP)}$	−0.5×$t_{(RCP)}$		
			66 MHz	−0.4×$t_{(RCP)}$	−0.5×$t_{(RCP)}$		
$t_{(RDC)}$	RCLK duty cycle			40%	50%	60%	ns
$t_{d(HZ)}$	High-to-high impedance state delay	See Figure 16	R_{OUT0}−R_{OUT9}		6.5	8	ns
$t_{d(LZ)}$	Low-to-high impedance state delay				4.7	8	ns
$t_{d(HR)}$	High-impedance state to high delay				5.3	8	ns
$t_{d(ZL)}$	High-impedance state to low delay				4.7	8	ns
$t_{(DSR1)}$	Deserializer PLL lock time from $\overline{\text{PWRDN}}$ (with SYNCPAT)	See Figure 17, Figure 18, and (1)	10 MHz			850 x t_{RFCP}	µs
			66 MHz			850 x t_{RFCP}	
			10 MHz			2	
$t_{(DSR2)}$	Deserializer PLL lock time from SYNCPAT		66 MHz			0.303	
$t_{d(ZHLK)}$	High-impedance state to high delay (power up)		$\overline{\text{LOCK}}$			3	ns
t_{RNM}	Deserializer noise margin	See Figure 19 and (2)	10 MHz		3680		ps
			66 MHz		540		

(1) $t_{(DSR1)}$ represents the time required for the deserializer to register that a lock has occurred upon powerup or when leaving the powerdown mode. $t_{(DSR2)}$ represents the time required to register that a lock has occurred for the powered up and enabled deserializer when the input (RI±) conditions change from not receiving data to receiving synchronization patterns (SYNCPATs). In order to specify deserializer PLL performance, t_{DSR1} and t_{DSR2} are specified with REFCLK active and stable and specific conditions of SYNCPATs.

(2) t_{RNM} represents the phase noise or jitter that the deserializer can withstand in the incoming data stream before bit errors occur.

TIMING DIAGRAMS AND TEST CIRCUITS

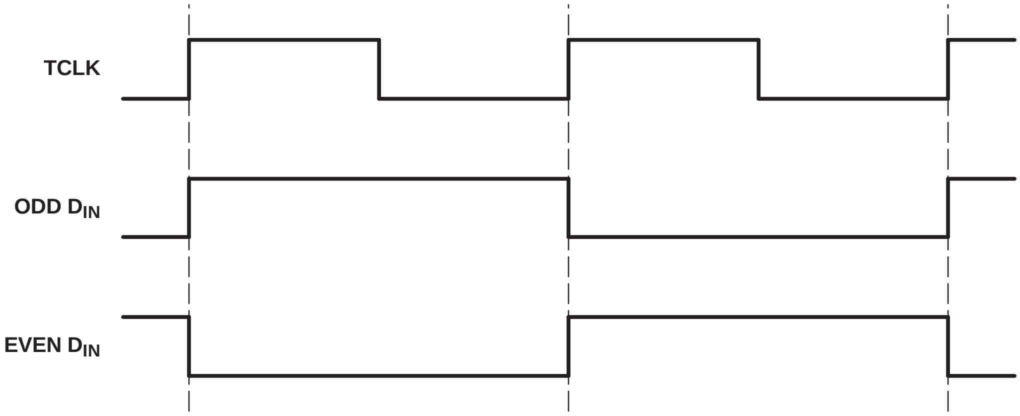


Figure 3. Worst-Case Serializer I_{CC} Test Pattern

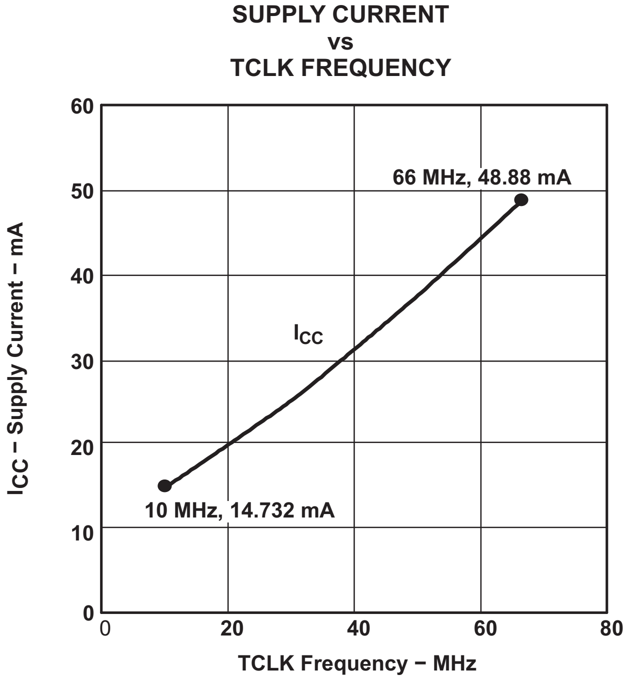


Figure 4.

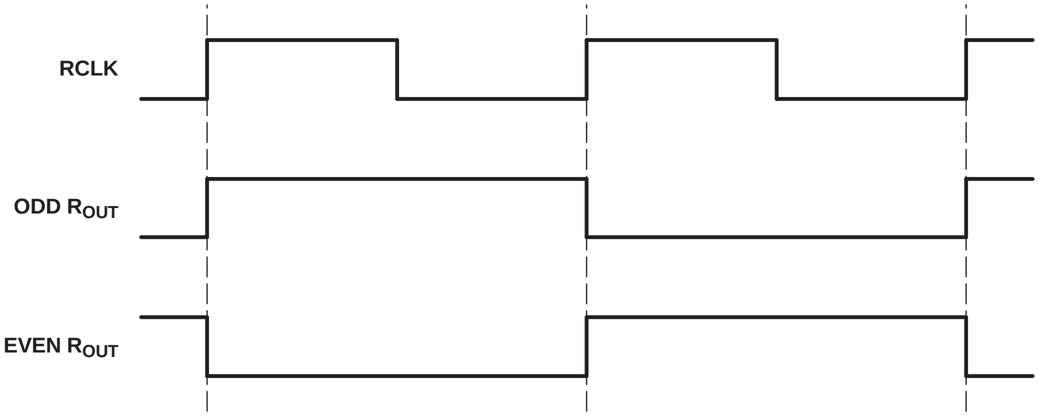


Figure 5. Worst-Case Deserializer I_{CC} Test Pattern

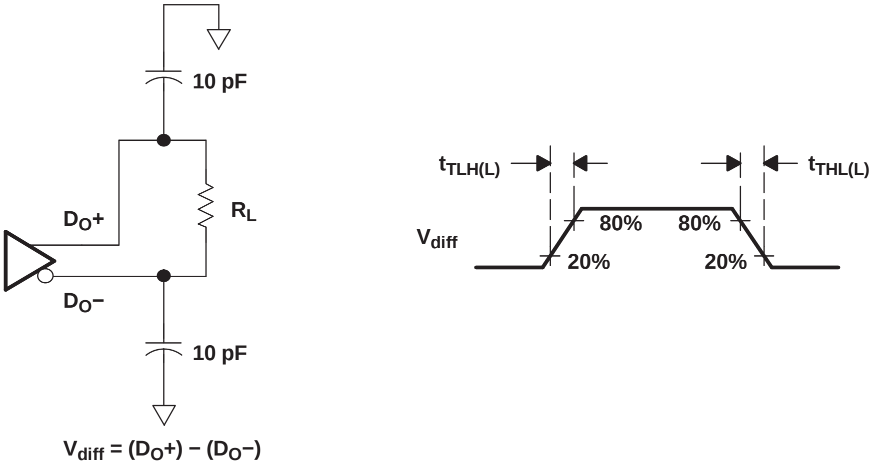


Figure 6. Serializer LVDS Output Load and Transition Times

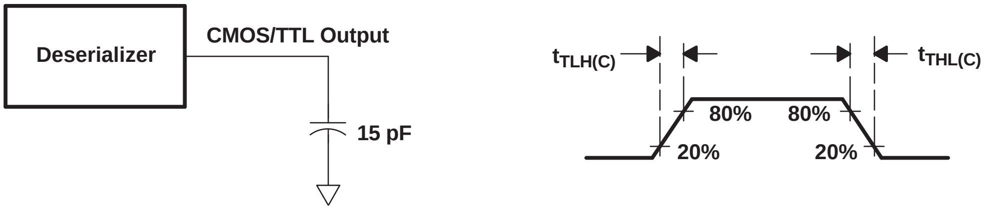


Figure 7. Deserializer CMOS/TTL Output Load and Transition Times

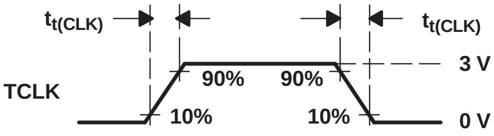


Figure 8. Serializer Input Clock Transition Time

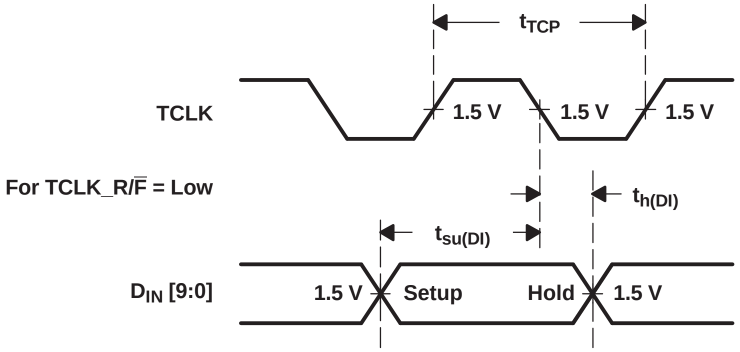


Figure 9. Serializer Setup/Hold Times

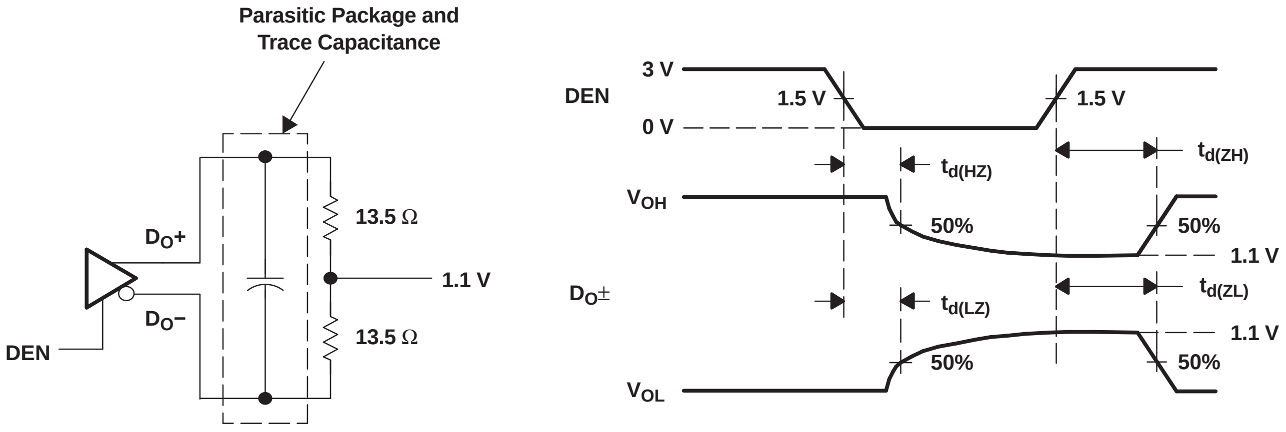


Figure 10. Serializer High-Impedance State Test Circuit and Timing

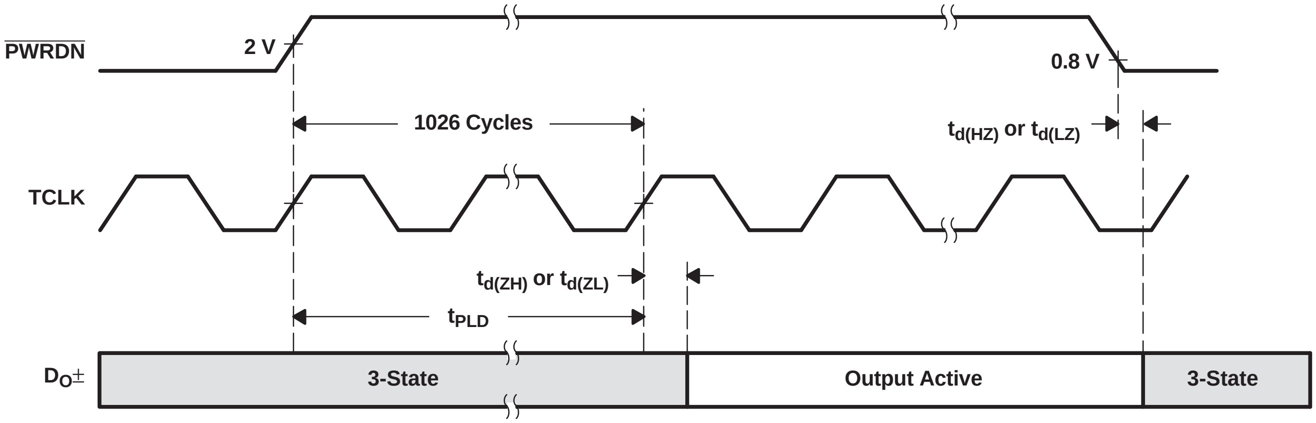


Figure 11. Serializer PLL Lock Time and $\overline{\text{PWRDN}}$ High-Impedance State Delays

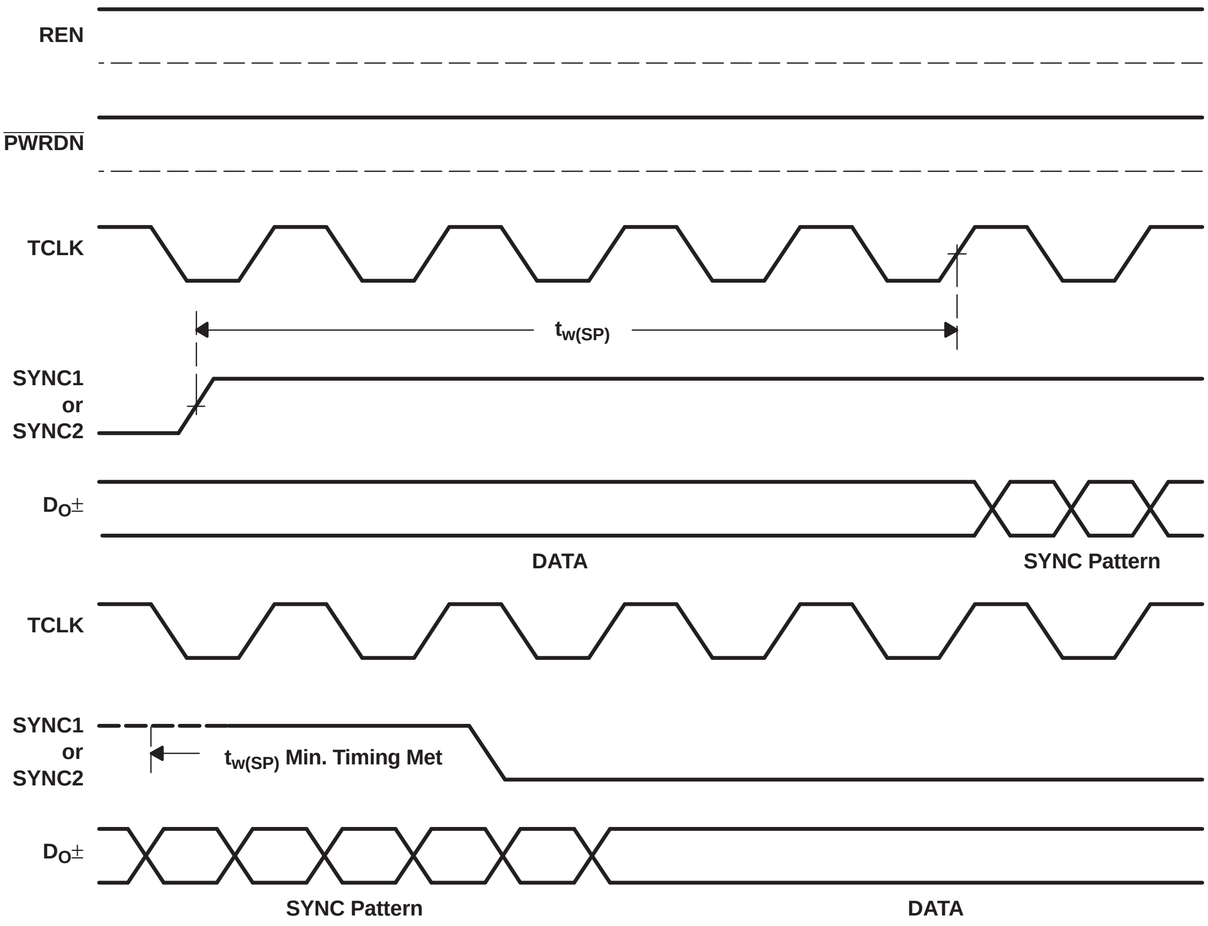


Figure 12. SYNC Timing Delays

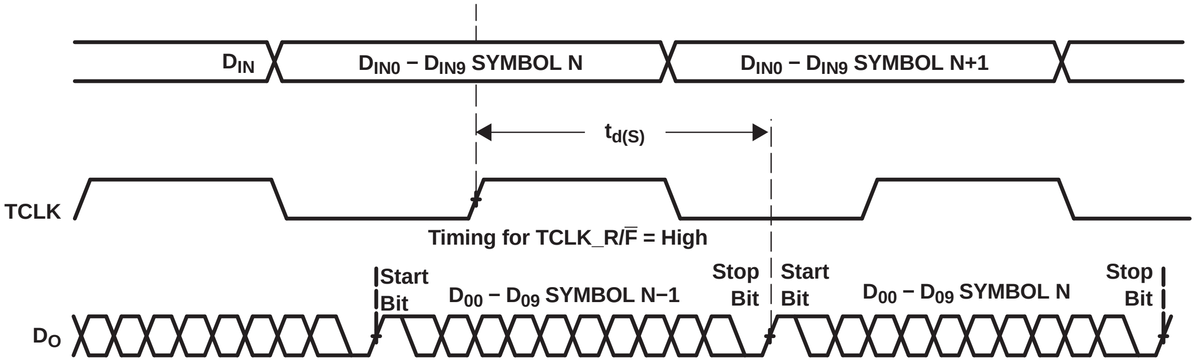


Figure 13. Serializer Delay

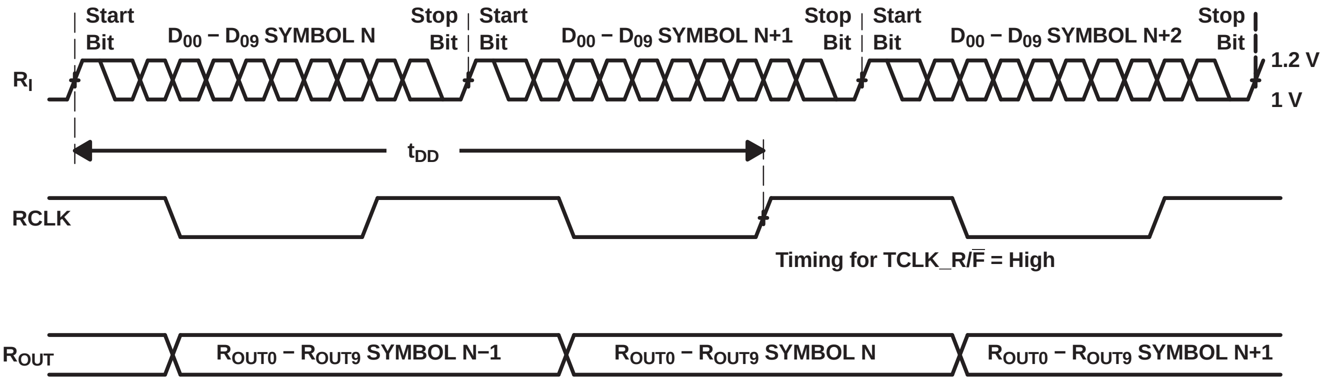


Figure 14. Deserializer Delay

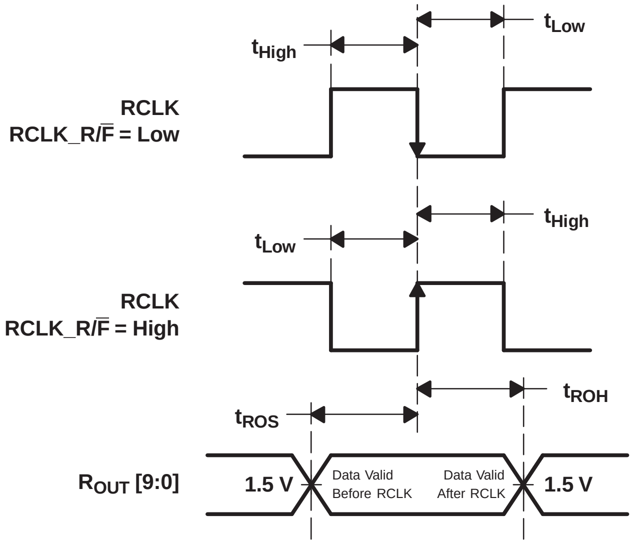


Figure 15. Deserializer Data Valid Out Times

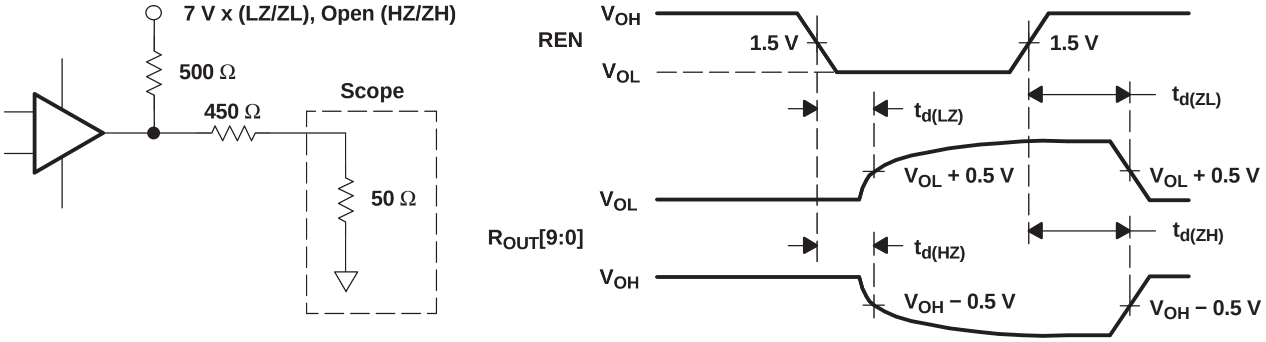


Figure 16. Deserializer High-Impedance State Test Circuit and Timing

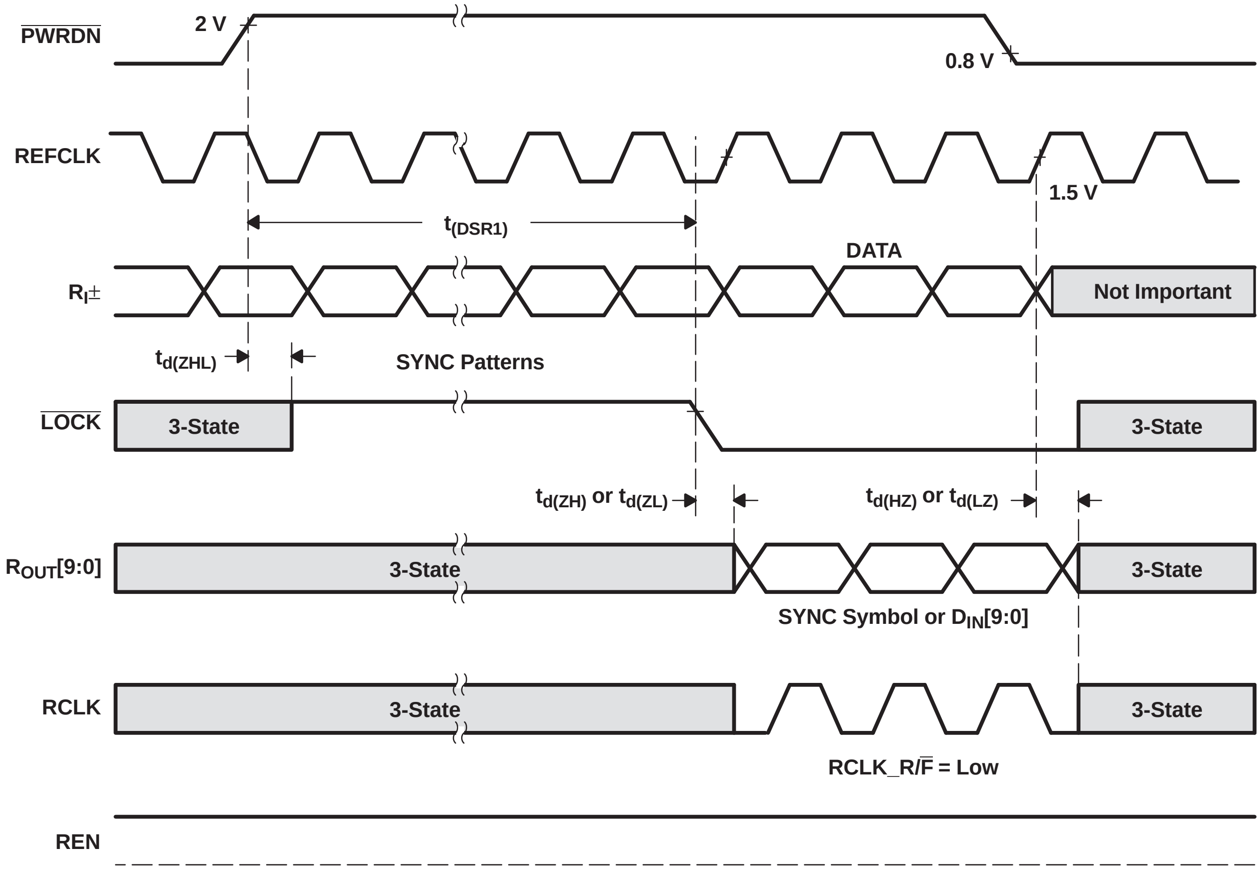


Figure 17. Deserializer PLL Lock Times and PWRDN 3-State Delays

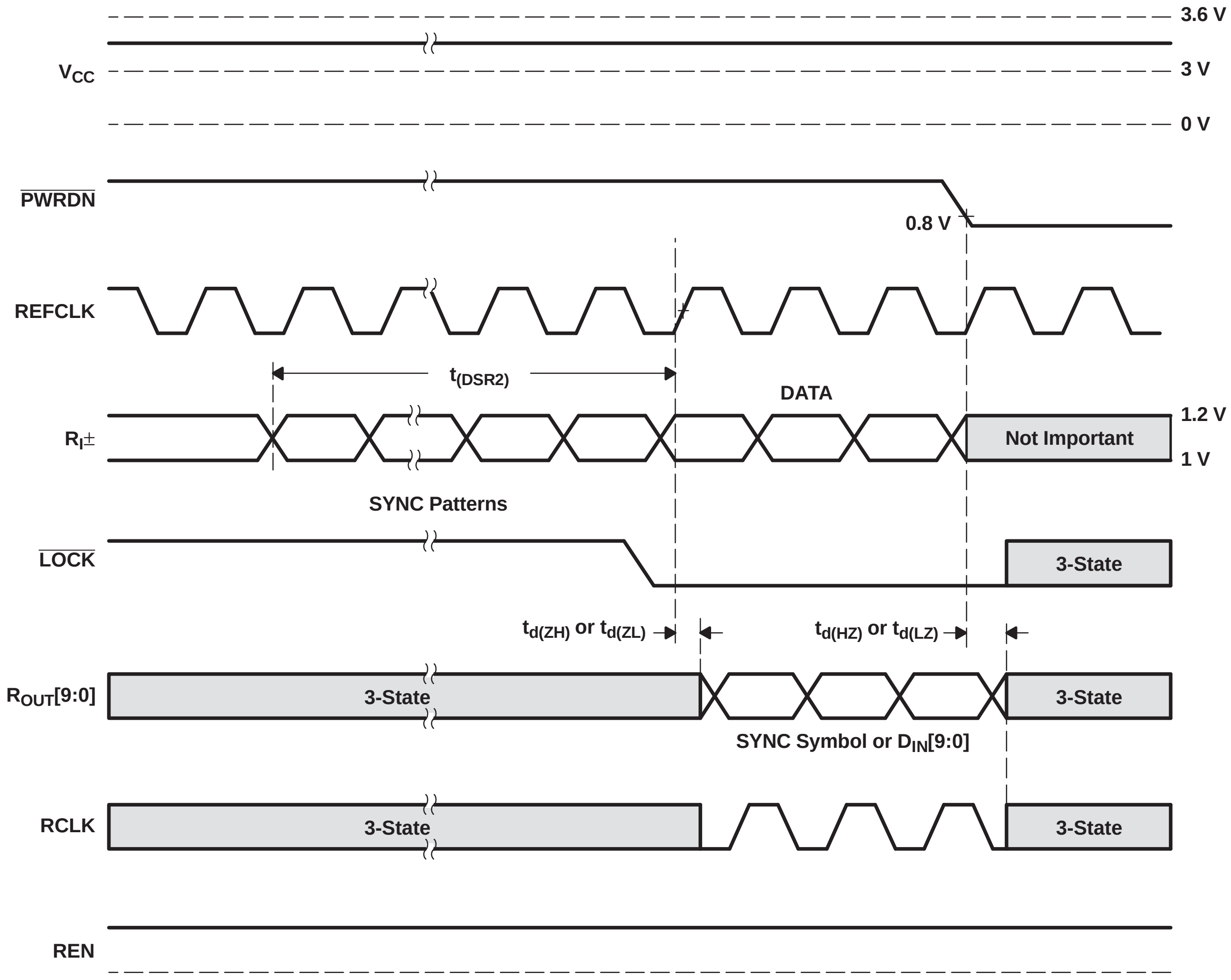
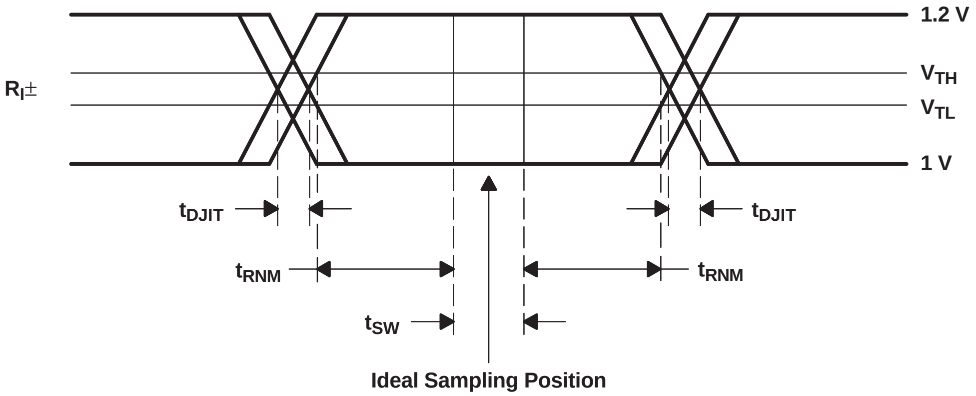
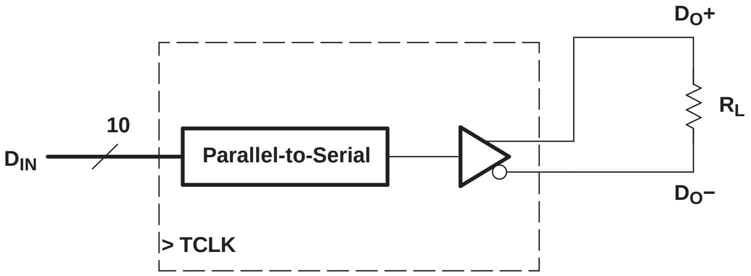


Figure 18. Deserializer PLL Lock Time From SyncPAT



t_{SW}: Setup and Hold Time (Internal Data Sampling Window)
t_{DJIT}: Serializer Output Bit Position Jitter That Results From Jitter on TCLK
t_{RNM}: Receiver Noise Margin Time

Figure 19. Receiver LVDS Input Skew Margin



$V_{OD} = (D_O+) - (D_O-)$
Differential Output Signal Is Shown as $(D_O+) - (D_O-)$

Figure 20. V_{OD} Diagram

DEVICE STARTUP PROCEDURE

It is recommended that the PWRDNB pin on both the SN65LV1023A and the SN65LV1224B device be held to a logic LOW level until after the power supplies have powered up to at least 3 V as shown in Figure 21.

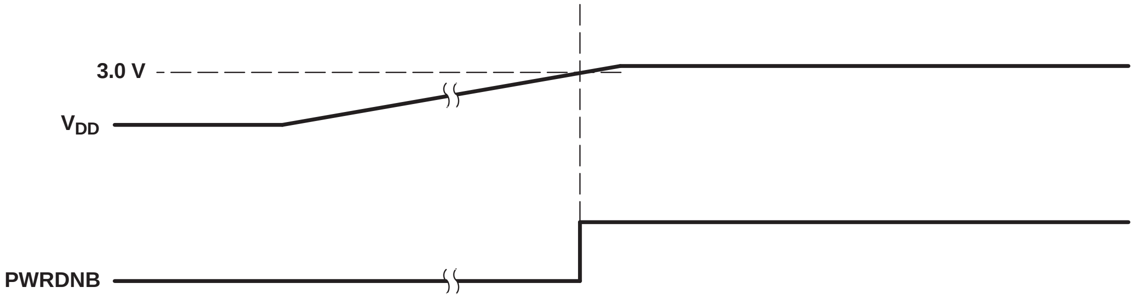


Figure 21. Device Startup

APPLICATION INFORMATION

DIFFERENTIAL TRACES AND TERMINATION

The performance of the SN65LV1023A/SN65LV1224B is affected by the characteristics of the transmission medium. Use controlled-impedance media and termination at the receiving end of the transmission line with the media's characteristics impedance.

Use balanced cables such as twisted pair or differential traces that are ran close together. A balanced cable picks up noise together and appears to the receiver as common mode. Differential receivers reject common-mode noise. Keep cables or traces matched in length to help reduce skew.

Running the differential traces close together helps cancel the external magnetic field, as well as maintain a constant impedance. Avoiding sharp turns and reducing the number of vias also helps.

TOPOLOGIES

There are several topologies that the serializers can operate. Three common examples are shown below.

Figure 22 shows an example of a single-terminated point-to-point connection. Here a single termination resistor is located at the deserializer end. The resistor value should match that of the characteristic impedance of the cable or PC board traces. The total load seen by the serializer is 100 Ω. Double termination can be used and typically reduces reflections compared with single termination. However, it also reduces the differential output voltage swing.

AC-coupling is only recommended if the parallel TX data stream is encoded to achieve a dc-balanced data stream. Otherwise the ac-capacitors can induce common mode voltage drift due to the dc-unbalanced data stream.

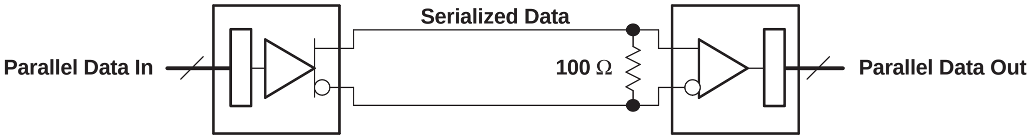


Figure 22. Single-Terminated Point-to-Point Connection

Figure 23 shows an example of a multidrop configuration. Here there is one transmitter broadcasting data to multiple receivers. A 50-kΩ resistor at the far end terminates the bus.

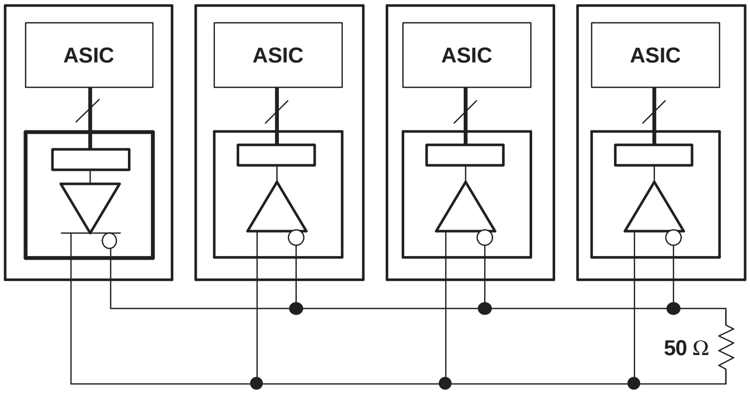


Figure 23. Multidrop Configuration

Figure 24 shows an example of multiple serializers and deserializers on the same differential bus, such as in a backplane. This is a multipoint configuration. In this situation, the characteristic impedance of the bus can be significantly less due to loading. Termination resistors that match the loaded characteristic impedance are required at each end of the bus. The total load seen by the serializer in this example is 27 Ω.

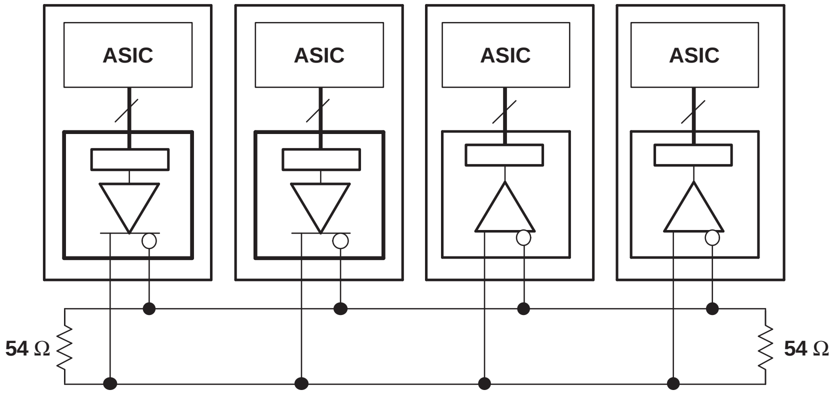


Figure 24. Multiple Serializers and Deserializers on the Same Differential Bus

REVISION HISTORY

Changes from Original (September 2004) to Revision A	Page
• Changed Figure 17	17
• Changed Figure 18	18

Changes from Revision A (January 2005) to Revision B	Page
• Added RHB package information	1

Changes from Revision B (July 2005) to Revision C	Page
• Changed Package description in the Features list.	1

Changes from Revision C (February 2006) to Revision D	Page
• Added the Applications List	1
• Deleted the DB and RHB packages for Deserializer	1
• Added Figure 2	9
• Changed Figure 4 Supply Current vs TCLK Frequency	12

Changes from Revision D (February 2009) to Revision E	Page
• Deleted footnote - "The deserializer delay time for all frequencies does not exceed two serial bit times" From $t_{d(D)}$	11

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN65LV1023ADB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LV1023ADBG4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LV1023ADBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LV1023ADBRG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LV1023ARHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LV1023ARHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LV1023ARHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LV1224BDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LV1224BDBG4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LV1224BDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LV1224BDBRG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LV1224BRHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LV1224BRHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LV1224BRHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LV1224BRHBTG4	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SNLV1023ARHBTG4	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

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[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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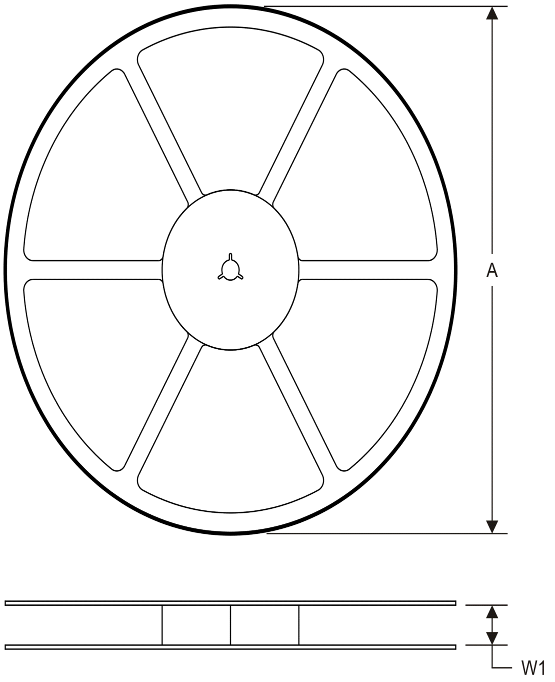
OTHER QUALIFIED VERSIONS OF SN65LV1023A, SN65LV1224B :
- Enhanced Product: SN65LV1023A-EP, SN65LV1224B-EP

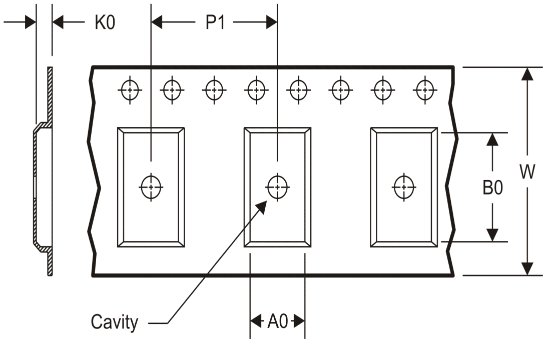
NOTE: Qualified Version Definitions:
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



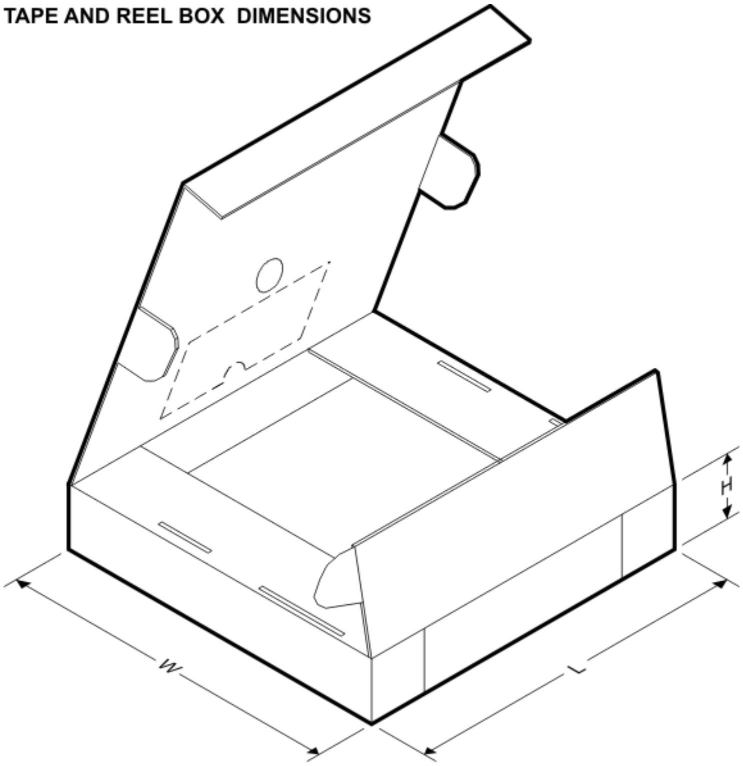
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LV1023ADBR	SSOP	DB	28	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN65LV1023ARHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
SN65LV1023ARHBT	QFN	RHB	32	250	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
SN65LV1224BDBR	SSOP	DB	28	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN65LV1224BRHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
SN65LV1224BRHBT	QFN	RHB	32	250	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

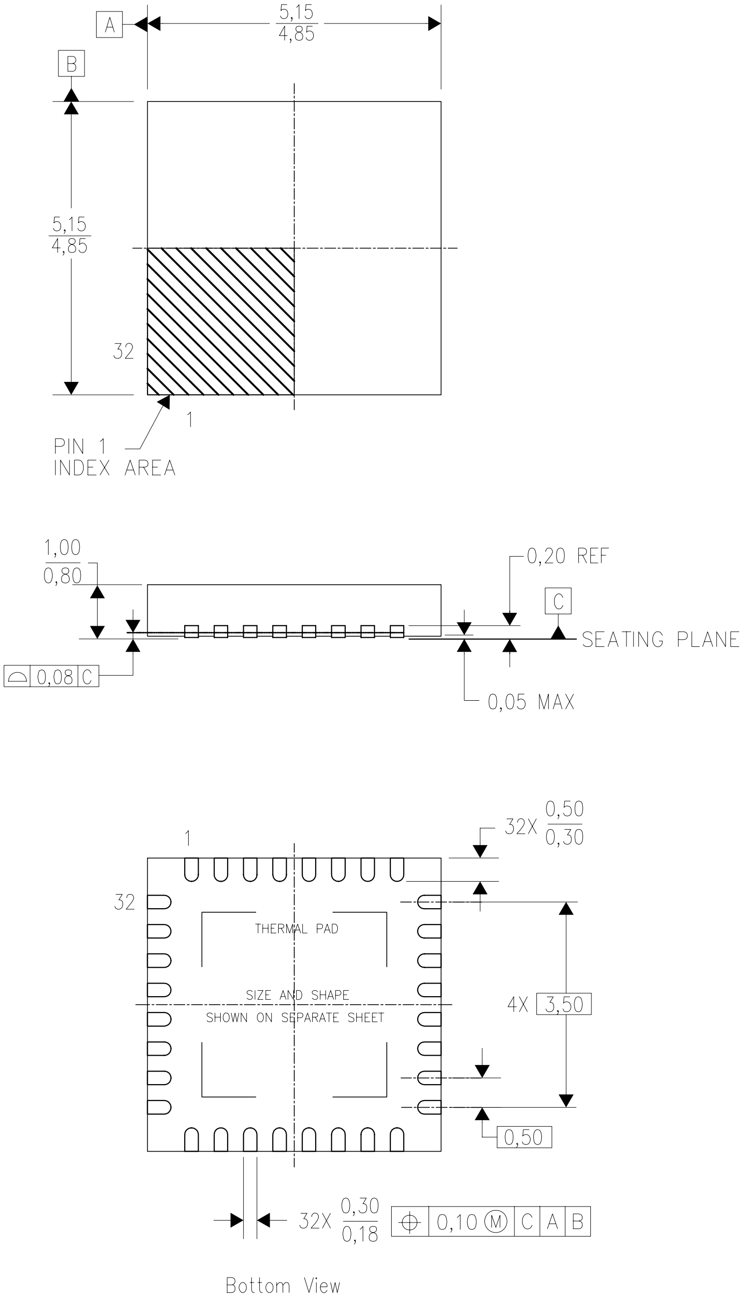
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LV1023ADBR	SSOP	DB	28	2000	367.0	367.0	38.0
SN65LV1023ARHBR	QFN	RHB	32	3000	338.1	338.1	20.6
SN65LV1023ARHBT	QFN	RHB	32	250	338.1	338.1	20.6
SN65LV1224BDBR	SSOP	DB	28	2000	367.0	367.0	38.0
SN65LV1224BRHBR	QFN	RHB	32	3000	338.1	338.1	20.6
SN65LV1224BRHBT	QFN	RHB	32	250	338.1	338.1	20.6

RHB (S-PVQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO-220.

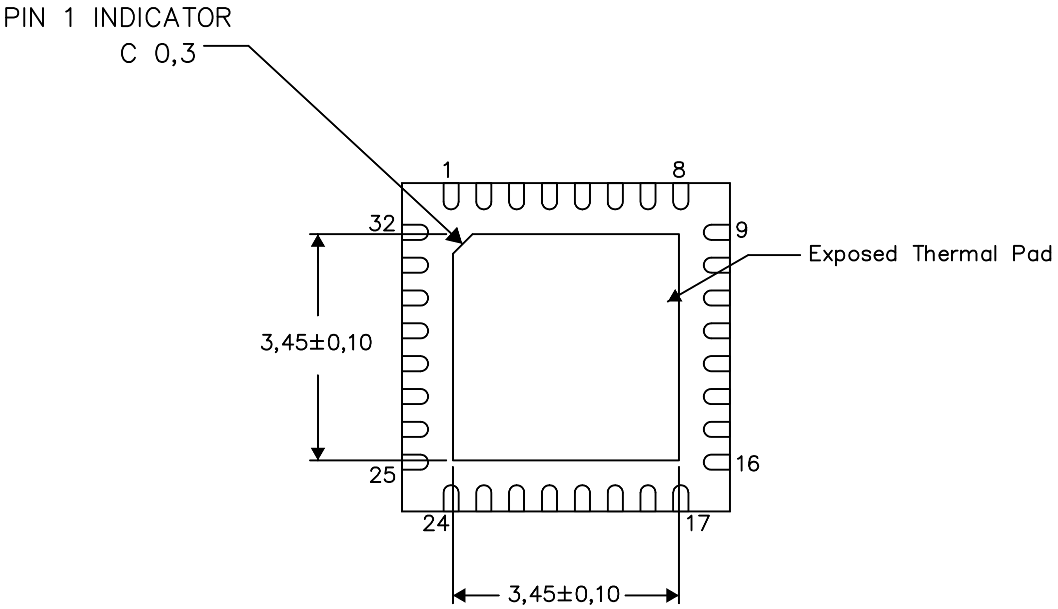
RHB (S-PVQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



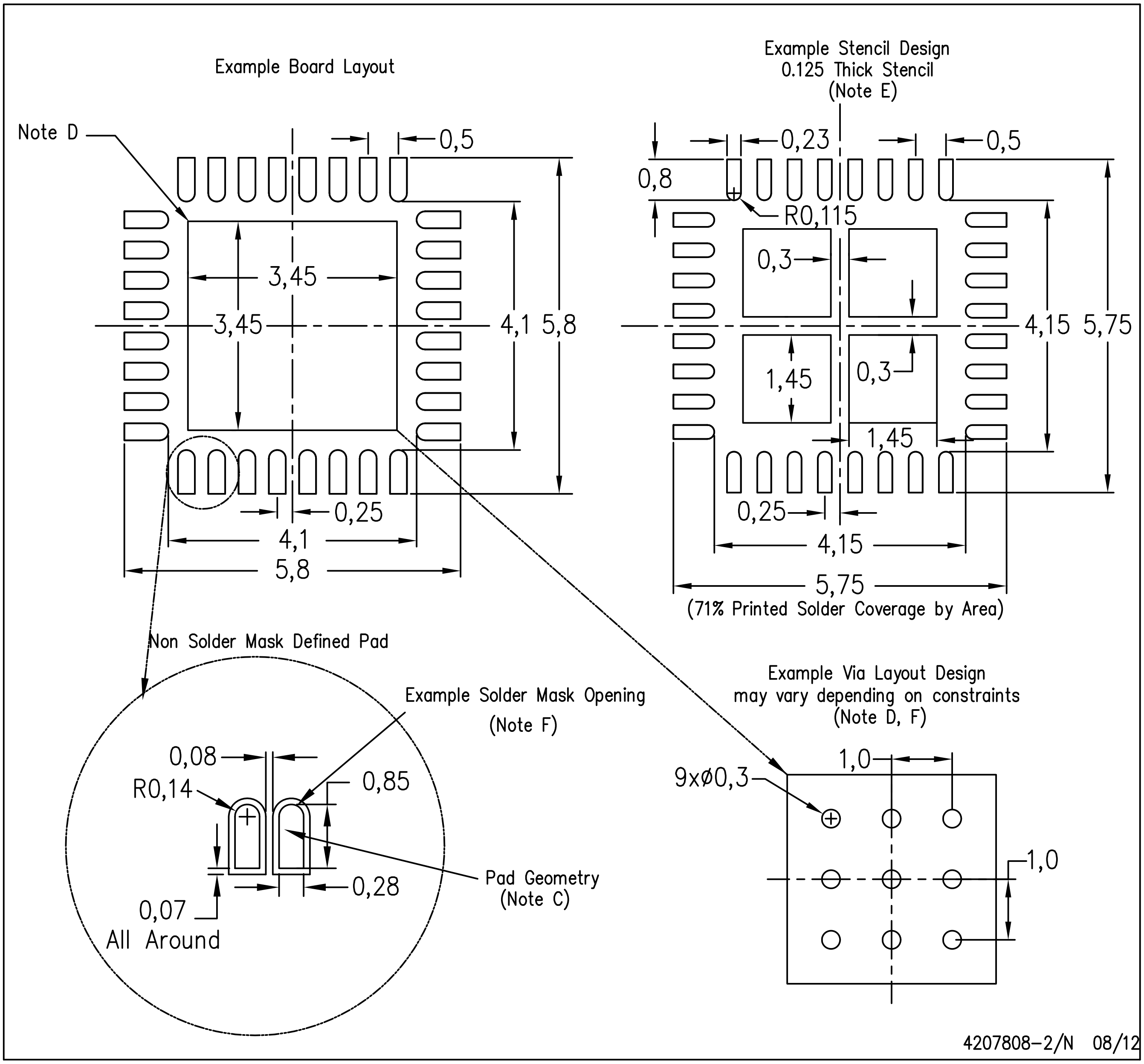
Bottom View

Exposed Thermal Pad Dimensions

4206356-2/W 09/12

NOTE: A. All linear dimensions are in millimeters

RHB (S-PVQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD

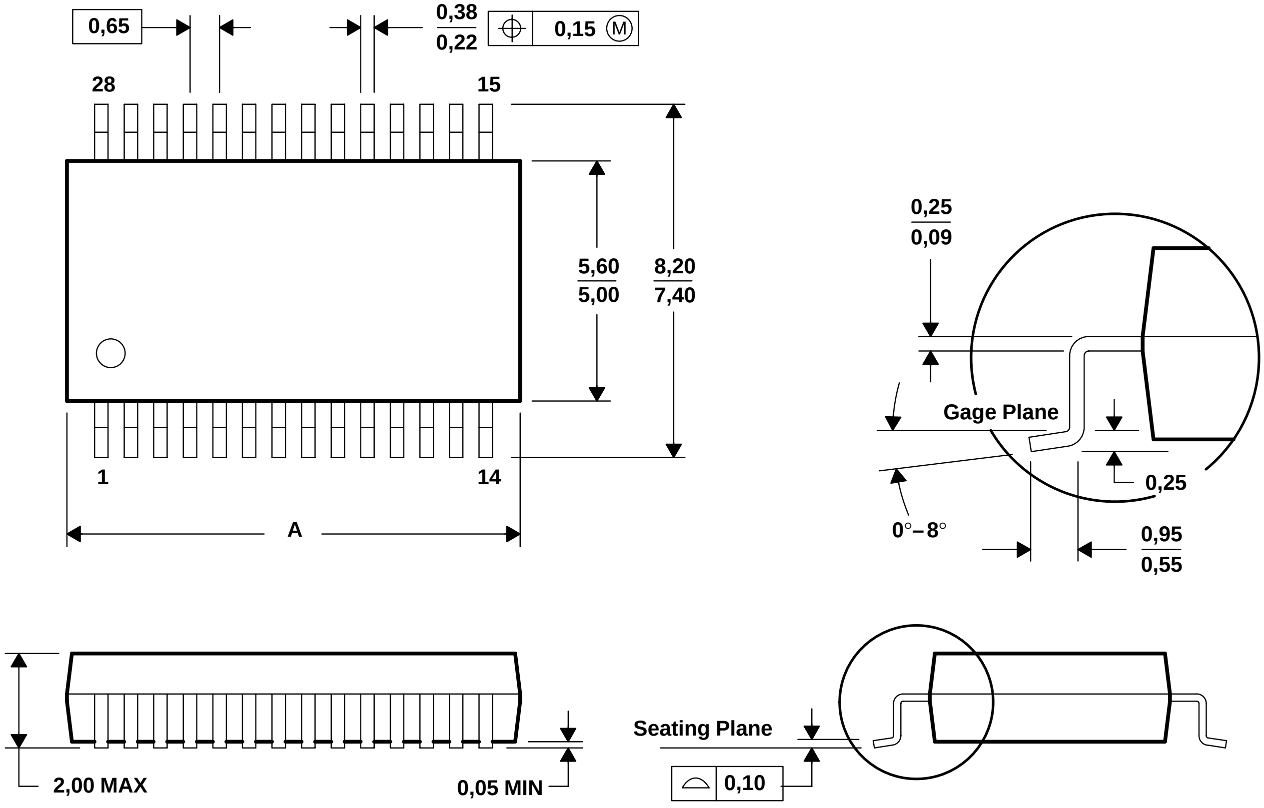


4207808-2/N 08/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

DB (R-PDSO-G**) PLASTIC SMALL-OUTLINE

28 PINS SHOWN



PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150

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