

SN74ALVC162601

18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS376 – MARCH 1994

- Member of the Texas Instruments *Widebus™* Family
- *UBT™* (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors on All I/O Pins
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit universal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC162601 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}), latch-enable (\overline{LEAB} and \overline{LEBA}), and clock (\overline{CLKAB} and \overline{CLKBA}) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when \overline{LEAB} is high. When \overline{LEAB} is low, the A data is latched if \overline{CLKAB} is held at a high or low logic level. If \overline{LEAB} is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of \overline{CLKAB} . Output enable \overline{OEAB} is active low. When \overline{OEAB} is low, the outputs are active. When \overline{OEAB} is high, the outputs are in the high-impedance state.

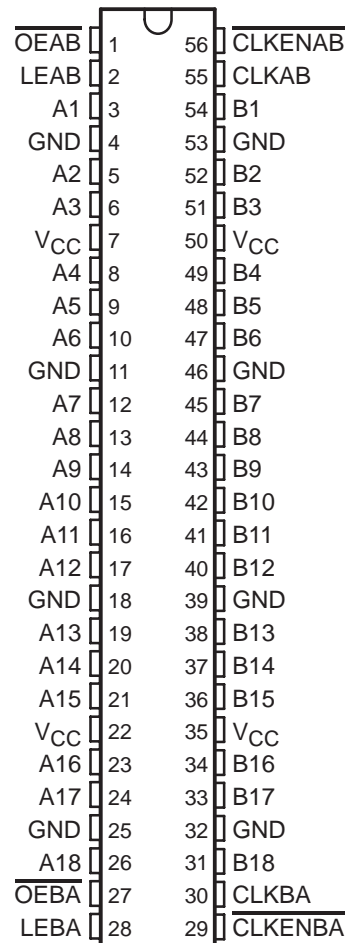
Data flow for B to A is similar to that of A to B but uses \overline{OEBA} , \overline{LEBA} , \overline{CLKBA} , and $\overline{CLKENBA}$.

The B-port outputs, include 25- Ω series resistors to reduce overshoot and undershoot.

The SN74ALVC162601 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC162601 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

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FUNCTION TABLE†

INPUTS					OUTPUT
CLKENAB	OEAB	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B ₀ ‡
H	L	L	X	X	B ₀ ‡
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B ₀ ‡
L	L	L	H	X	B ₀ §

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

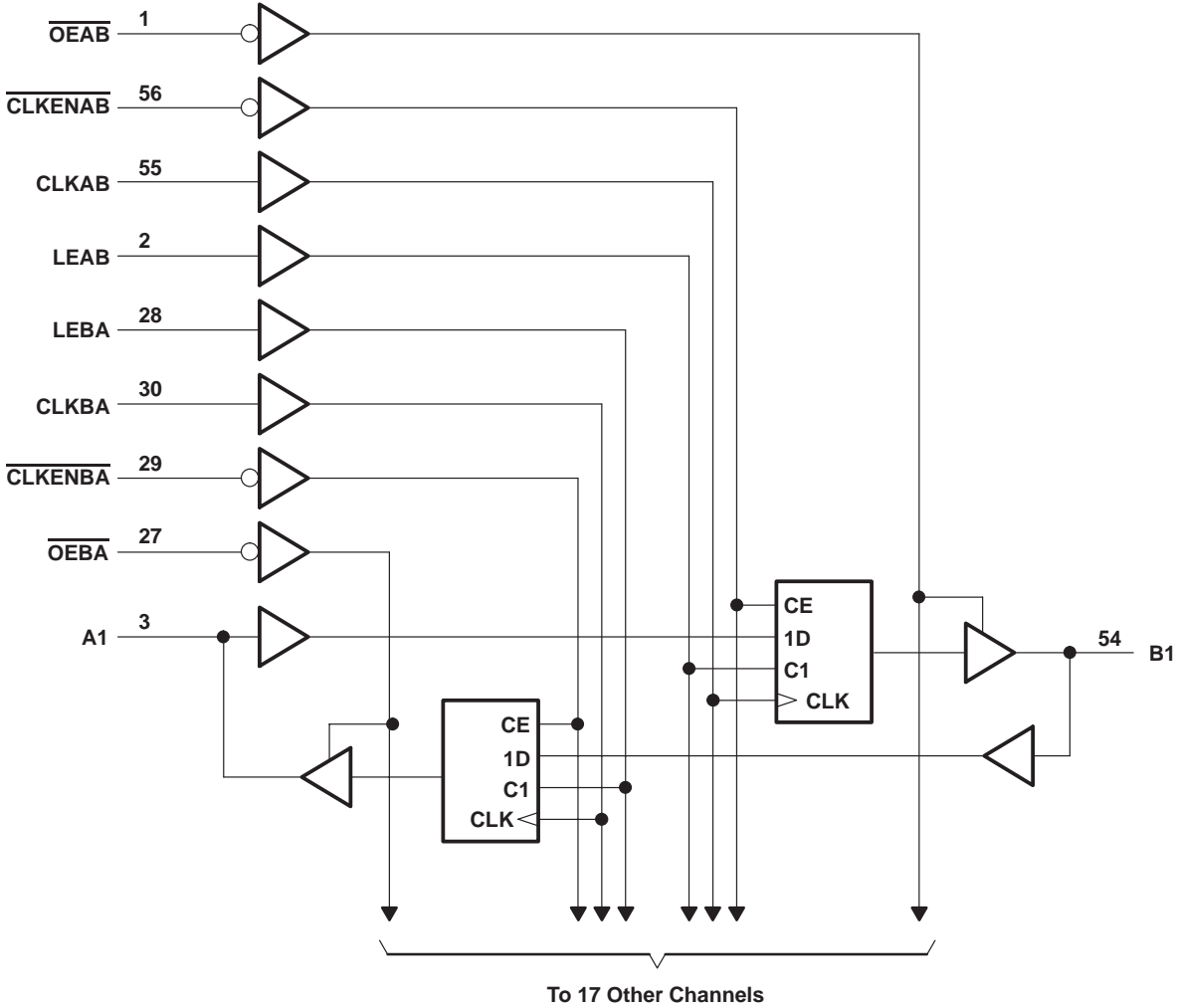
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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		mA
		$V_{CC} = 3$ V		
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		mA
		$V_{CC} = 3$ V		
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	–40	85	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC} [†]	MIN	MAX	UNIT
V _{OH}		I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2		V
		I _{OH} = -4 mA	2.7 V	2.4		
		I _{OH} = -6 mA	3 V	2.4		
		I _{OH} = TBD		2		
V _{OL}		I _{OL} = 100 μA	MIN to MAX	0.2		V
		I _{OL} = 4 mA	2.7 V	0.4		
		I _{OL} = 6 mA	3 V	0.4		
		I _{OH} = TBD		0.8		
I _I		V _I = V _{CC} or GND	3.6 V	±5		μA
I _I (hold)		V _I = 0.8 V	3 V	75		μA
		V _I = 2 V		-75		
I _{OZ} [‡]		V _O = V _{CC} or GND	3.6 V	±10		μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	3.6 V	40		μA
ΔI _{CC}		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND		750		μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V			pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74ALVC162601DL	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
SN74ALVC162601DLR	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

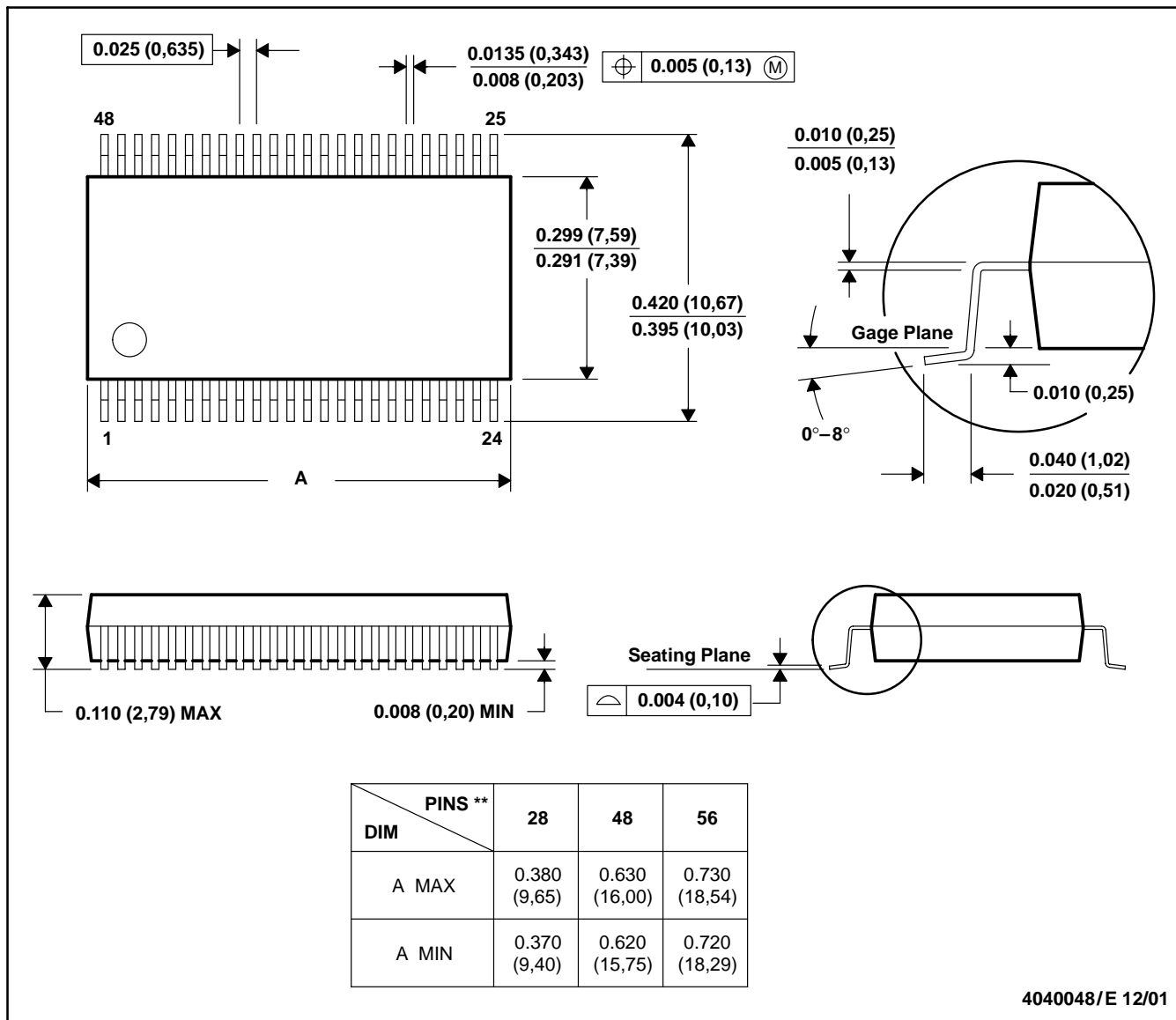
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DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

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