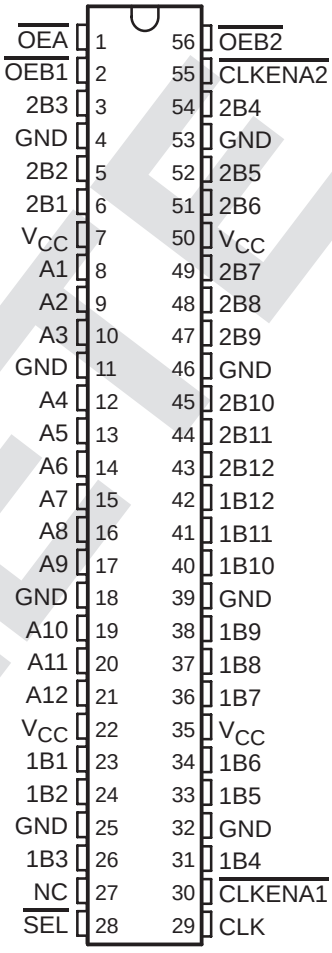
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Member of the Texas Instruments *Widebus*™ Family**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



NC − No internal connection

description

The SN74ALVC16269 is a 12-bit to 24-bit registered bus transceiver, which is intended for applications where two separate ports must be multiplexed onto, or demultiplexed from, a single port. The device is particularly suitable as an interface between synchronous DRAMs and high-speed microprocessors. The SN74ALVC16269 is designed specifically for low-voltage (3.3-V) V_{CC} operation; it is tested at 2.5-V, 2.7-V, and 3.3-V V_{CC}.

Data is stored in the internal B-port registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable ($\overline{\text{CLKENA}}$) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port. For data transfer in the B-to-A direction, a single storage register is provided. The select ($\overline{\text{SEL}}$) line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, thus extending the period that the data is valid on the bus. The control terminals are registered so that all transactions are synchronous with CLK. Data flow is controlled by the active-low output enables ($\overline{\text{OEA}}$, $\overline{\text{OEB1}}$, $\overline{\text{OEB2}}$).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16269 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16269 is characterized for operation from −40°C to 85°C.

Function Tables

OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	$\overline{OEA}$	$\overline{OEB}$	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A-TO-B STORAGE ($\overline{OEB}$ = L)

INPUTS				OUTPUTS	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B	2B
H	H	X	X	$1B_0$†	$2B_0$†
L	X	↑	L	L	X
L	X	↑	H	H	X
X	L	↑	L	X	L
X	L	↑	H	X	H

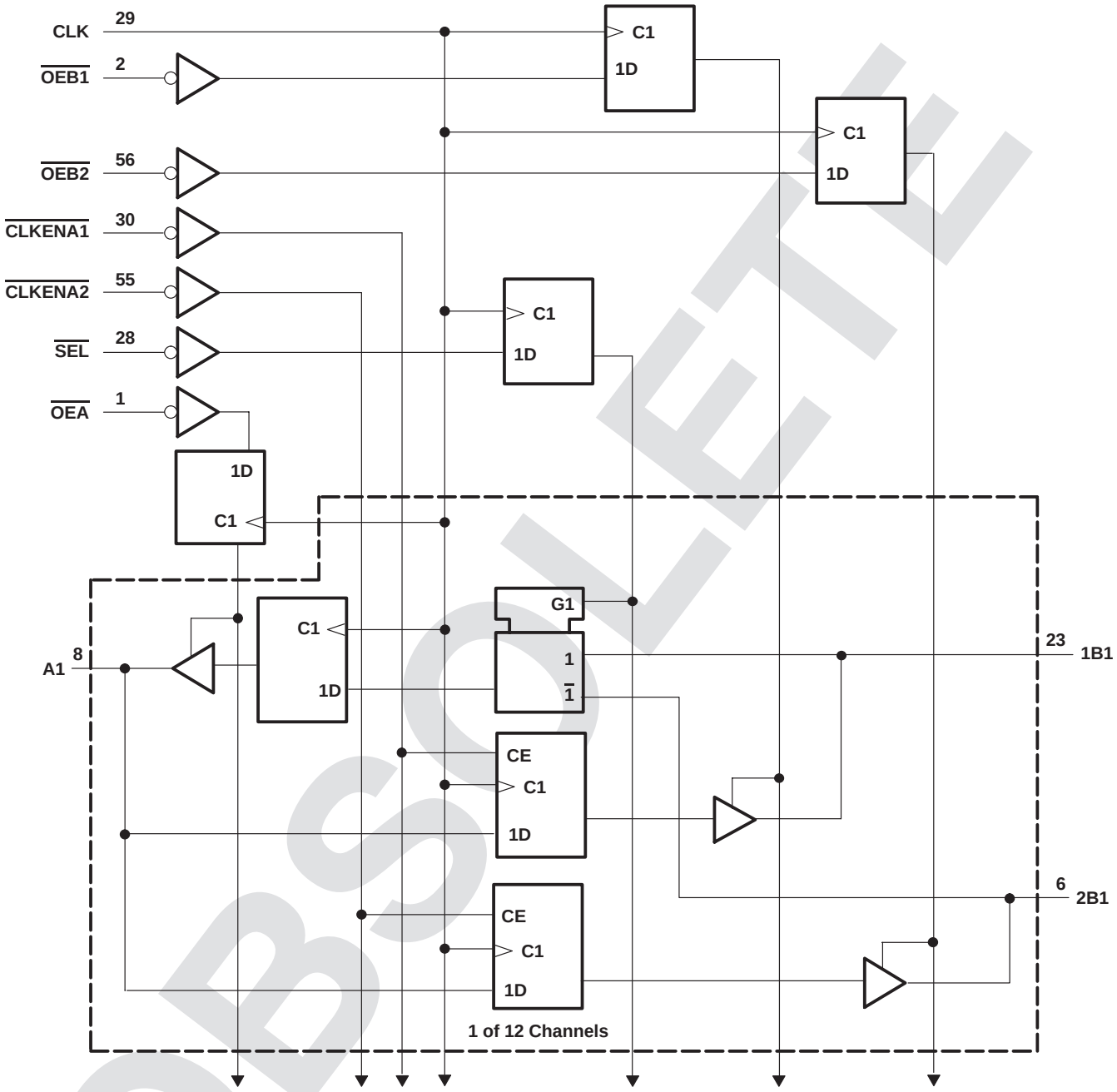
† Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{OEA}$ = L)

INPUTS				OUTPUT
CLK	$\overline{SEL}$	1B	2B	A
X	H	X	X	A_0†
X	L	X	X	A_0†
↑	H	L	X	L
↑	H	H	X	H
↑	L	X	L	L
↑	L	X	H	H

† Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 4.6 V
Input voltage range, V_I: Except I/O ports (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
I/O ports (see Notes 1 and 2) . . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . −50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package . . . . . 1 W
DL package . . . . . 1.4 W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		−12	mA
		V_{CC} = 2.7 V		−12	
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		12	mA
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = −40°C to 85°C			UNIT
				MIN	TYP‡	MAX	
V_{OH}	I_{OH} = −100 μA		MIN to MAX	V_{CC} − 0.2			V
	I_{OH} = −6 mA,	V_{IH} = 1.7 V	2.3 V	2			
	I_{OH} = −12 mA	V_{IH} = 1.7 V	2.3 V	1.7			
		V_{IH} = 2 V	2.7 V	2.2			
		V_{IH} = 2 V	3 V	2.4			
	I_{OH} = −24 mA,	V_{IH} = 2 V	3 V	2			
V_{OL}	I_{OL} = 100 μA		MIN to MAX			0.2	V
	I_{OL} = 6 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
	I_{OL} = 12 mA	V_{IL} = 0.7 V	2.3 V			0.7	
		V_{IL} = 0.8 V	2.7 V			0.4	
	I_{OL} = 24 mA,	V_{IL} = 0.8 V	3 V			0.55	
I_I	V_I = V_{CC} or GND		3.6 V			±5	μA
$I_{I(hold)}$	V_I = 0.7 V		2.3 V	45			μA
	V_I = 1.7 V			−45			
	V_I = 0.8 V		3 V	75			
	V_I = 2 V			−75			
	V_I = 0 to 3.6 V		3.6 V			±500	
I_{OZ}§	V_O = V_{CC} or GND		3.6 V			±10	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	μA
ΔI_{CC}	One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND		3 V to 3.6 V			750	μA
C_i	V_I = V_{CC} or GND		3.3 V		3.5		pF
C_{io}	V_O = V_{CC} or GND		3.3 V		9		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ All typical values are at V_{CC} = 3.3 V.
§ For I/O ports, the parameter I_{OZ} includes the input-leakage current.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency				135		135		135	MHz
t_w	Pulse duration, CLK high or low			3.3		3.3		3.3		ns
t_{su}	Setup time	A data before CLK↑	High or low	2		2		1.7		ns
		B data before CLK↑	High or low	2.2		2.1		1.8		
		$\overline{SEL}$ before CLK↑	High or low	1.6		1.6		1.3		
		$\overline{CLKENA1}$ or $\overline{CLKENA2}$ before CLK↑	High or low	1		1.2		0.9		
		$\overline{OE}$ before CLK↑	High or low	1.5		1.6		1.3		
t_h	Hold time	A data after CLK↑	High or low	0.7		0.6		0.6		ns
		B data after CLK↑	High or low	0.7		0.6		0.6		
		$\overline{SEL}$ after CLK↑	High or low	1.1		0.7		0.7		
		$\overline{CLKENA1}$ or $\overline{CLKENA2}$ after CLK↑	High or low	1		0.8		1.1		
		$\overline{OE}$ after CLK↑	High or low	0.8		0.8		0.8		

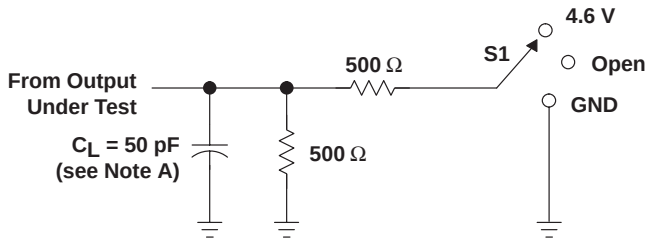
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			135		135		135		ns
t_{pd}	CLK	B	1	8.8		7.3	1	6.2	ns
		A	1	7		5.8	1	5	
t_{en}	CLK	B	1	8.4		6.7	1	6.1	ns
		A	1	8.1		6.2	1	5.9	
t_{dis}	CLK	B	1.4	8.3		6.9	1	6.1	ns
		A	1.5	7.7		6.8	1	5.6	

operating characteristics, T_A = 25°C

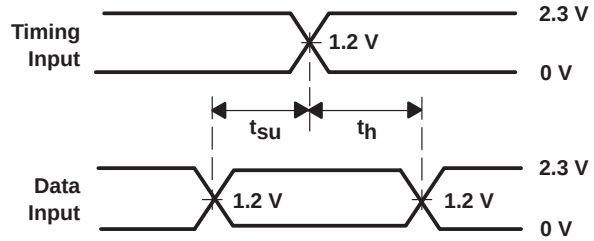
PARAMETER			TEST CONDITIONS	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 10 MHz	55	59	pF
		Outputs disabled		46	49	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

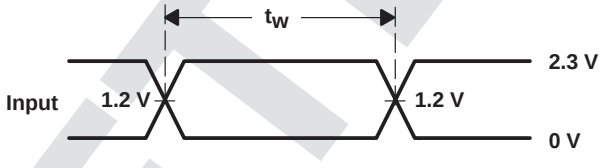


TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 4.6 V GND

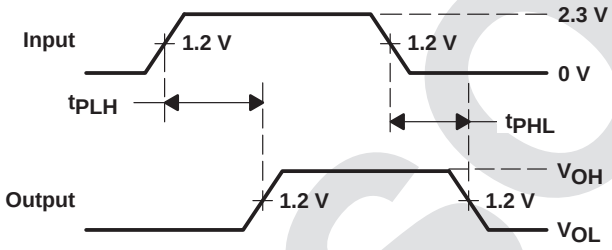
LOAD CIRCUIT



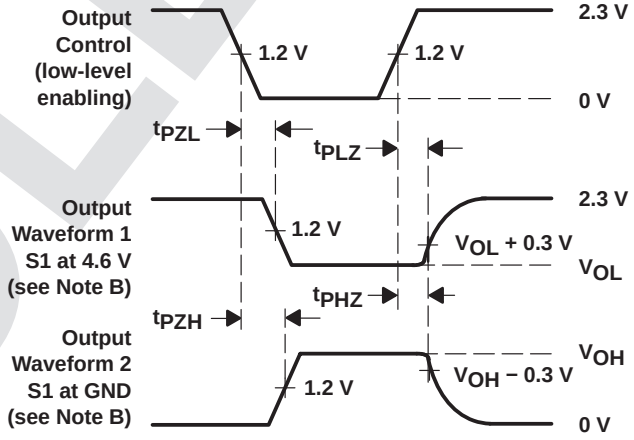
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

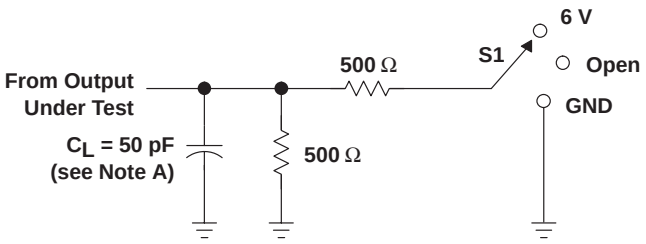


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

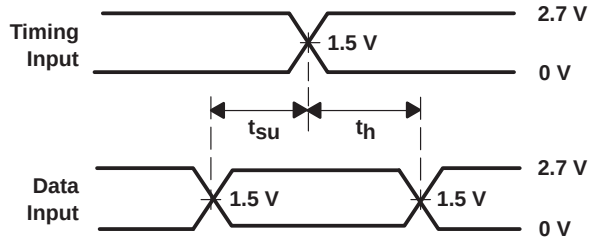
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

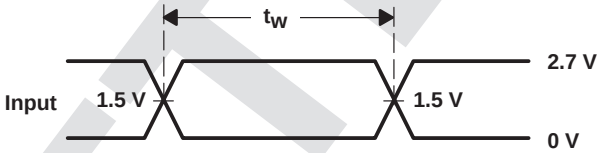


TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 6 V GND

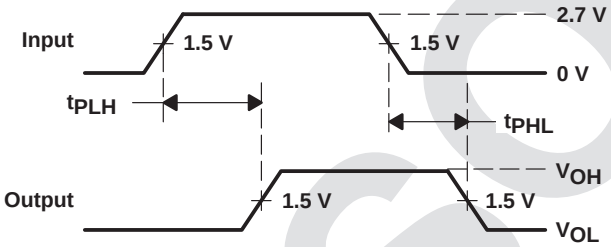
LOAD CIRCUIT



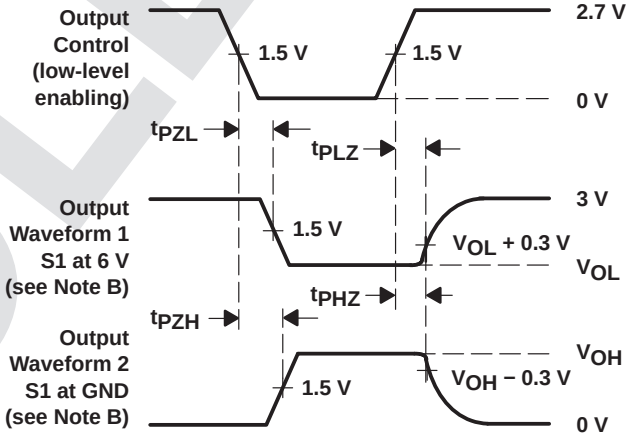
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265