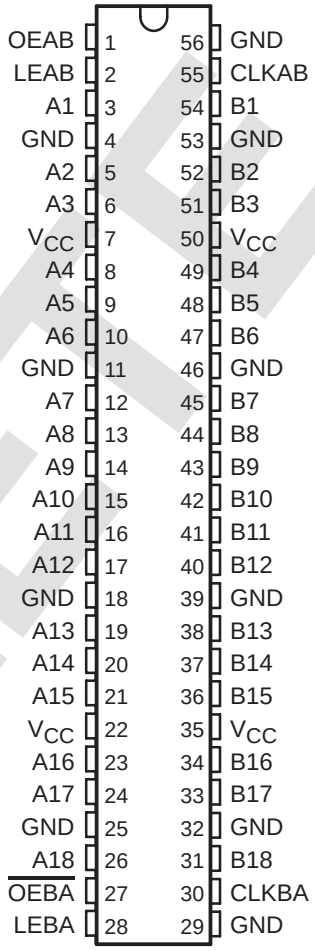
- ***EPIC*** ™ **(Enhanced-Performance Implanted CMOS) Submicron Process**
- **Member of the Texas Instruments *Widebus*™ Family**
- ***UBT*** ™ **(Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74ALVC16501 18-bit universal bus transceiver is designed for low-voltage (3.3-V) V_{CC} operation; it is tested at 2.5-V, 2.7-V, and 3.3-V V_{CC}.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and $\overline{\text{OEBA}}$ is active low).

The SN74ALVC16501 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

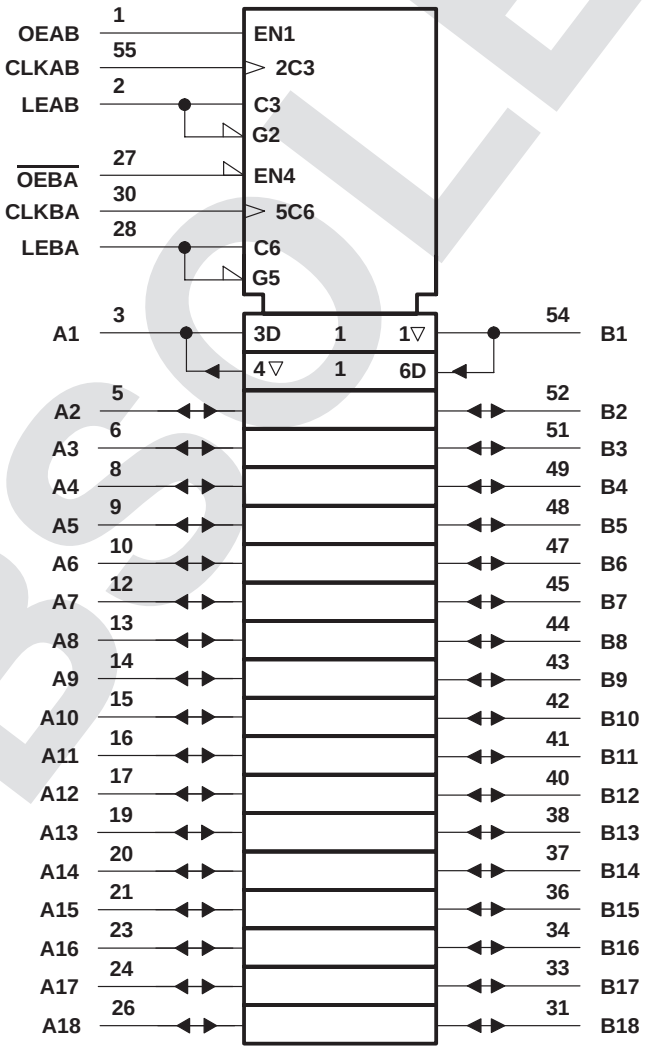
The SN74ALVC16501 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

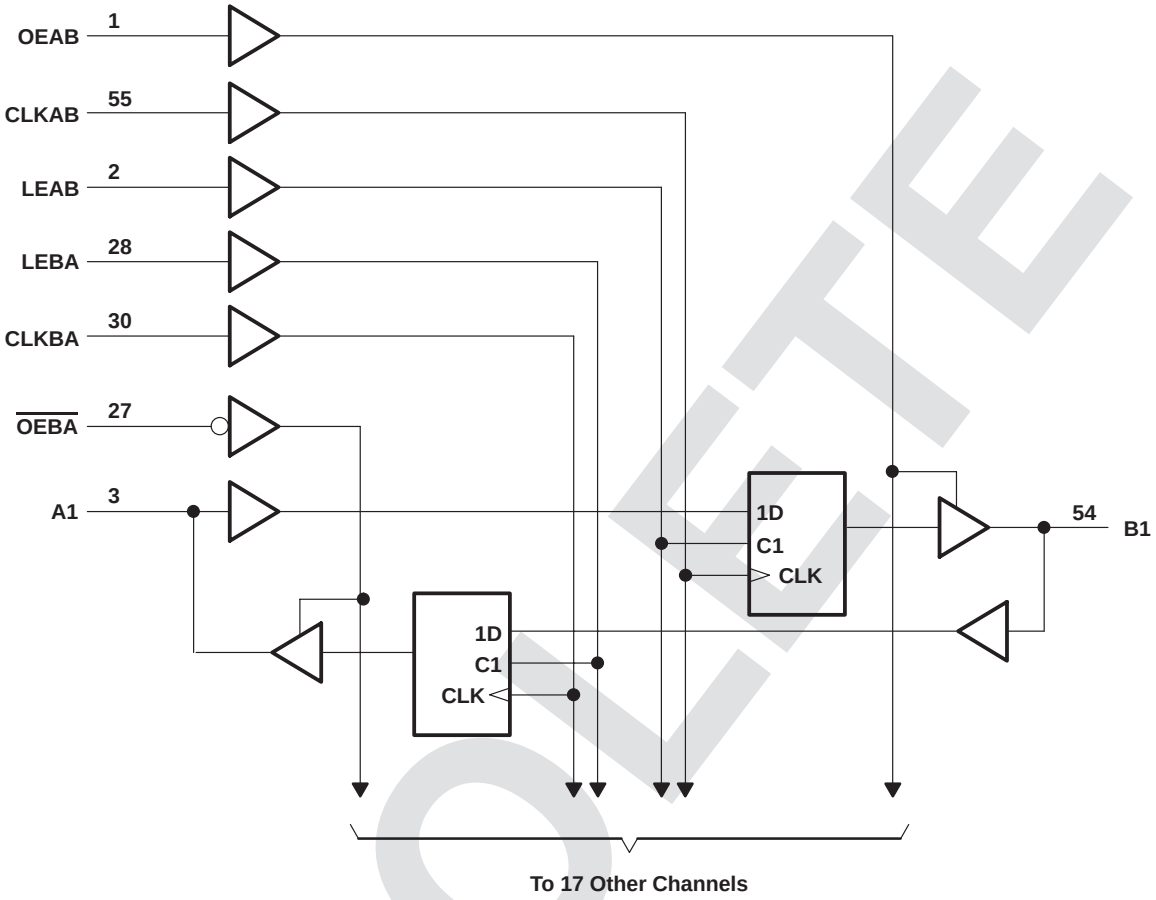
† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA.
‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB is high before LEAB goes low
§ Output level before the indicated steady-state input conditions were established

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	−0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0)	−50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		−12	mA
		V_{CC} = 2.7 V		−12	
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		12	mA
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}†	T_A = −40°C to 85°C			UNIT
					MIN	TYP‡	MAX	
V_{OH}		I_{OH} = −100 μA		MIN to MAX	V_{CC} −0.2			V
		I_{OH} = −6 mA	V_{IH} = 1.7 V	2.3 V	2			
		I_{OH} = −12 mA	V_{IH} = 1.7 V	2.3 V	1.7			
			V_{IH} = 2 V	2.7 V	2.2			
			V_{IH} = 2 V	3 V	2.4			
		I_{OH} = −24 mA	V_{IH} = 2 V	3 V	2			
V_{OL}		I_{OL} = 100 μA		MIN to MAX			0.2	V
		I_{OL} = 6 mA	V_{IL} = 0.7 V	2.3 V			0.4	
		I_{OL} = 12 mA	V_{IL} = 0.7 V	2.3 V			0.7	
			V_{IL} = 0.8 V	2.7 V			0.4	
		I_{OL} = 24 mA	V_{IL} = 0.8 V	3 V			0.55	
I_I		V_I = V_{CC} or GND		3.6 V				μA
I_{hold}		V_I = 0.7 V		2.3 V	45			μA
		V_I = 1.7 V			−45			
		V_I = 0.8 V		3 V	75			
		V_I = 2 V			−75			
		V_I = 0 to 3.6 V		3.6 V			±500	
I_{OZ}§		V_O = V_{CC} or GND		3.6 V			±10	μA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				750	μA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		4		pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V		8		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ All typical values are at V_{CC} = 3.3 V.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	MHz
t_w	Pulse duration	LE high	3.3		3.3		3.3		ns
		CLK high or low	3.3		3.3		3.3		
t_{su}	Setup time	Data before CLK↑	2.2		2.1		1.7		ns
		Data before LE↓, CLK high	1.9		1.6		1.5		
		Data before LE↓, CLK low	1.3		1.1		1		
t_h	Hold time	Data after CLK↑	0.6		0.6		0.7		ns
		Data after LE↓, CLK high or low	1.4		1.7		1.4		

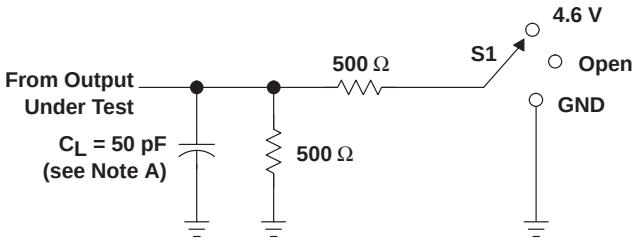
switching characteristics over recommended operating free-air temperature range, (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			150		150		150		ns
t_{pd}	$\overline{A}$ or B	B or A	1.2	5.4		4.5	1	3.9	ns
	LE	A or B	1.6	6.3		5.3	1.3	4.6	
	CLK	A or B	1.7	6.7		5.6	1.4	4.9	
t_{en}	$\overline{OEAB}$	B	1.1	6.3		5.3	1	4.6	ns
t_{dis}	$\overline{OEAB}$	B	2.2	6.4		5.7	1.4	5	ns
t_{en}	$\overline{OEBA}$	A	1.4	6.8		6	1.1	5	ns
t_{dis}	$\overline{OEBA}$	A	2	5.5		4.6	1.3	4.2	ns

operating characteristics, T_A = 25°C

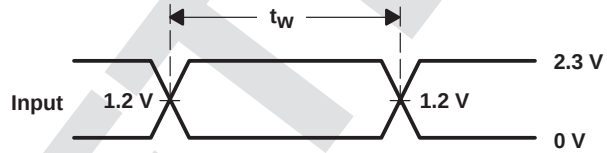
PARAMETER			TEST CONDITIONS	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 10 MHz	44	54	pF
		Outputs disabled		6	6	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

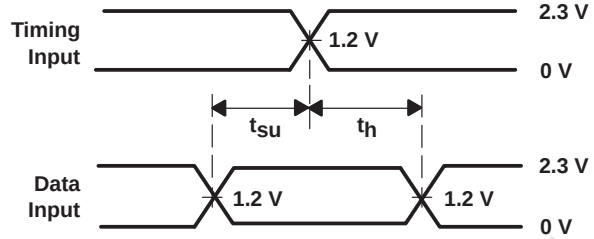


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND

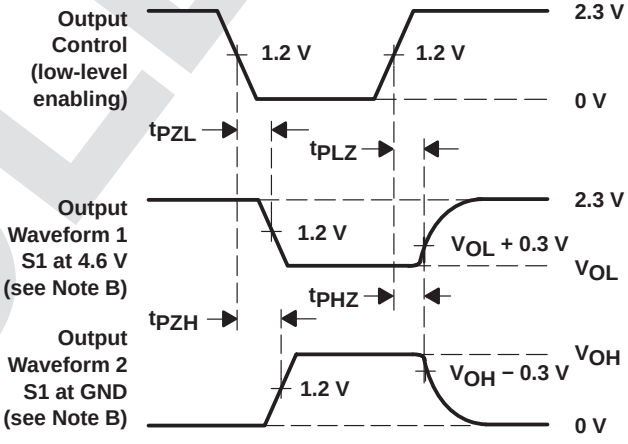
LOAD CIRCUIT



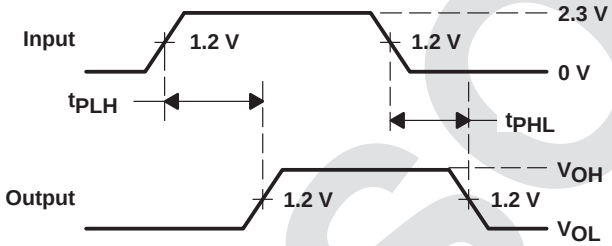
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

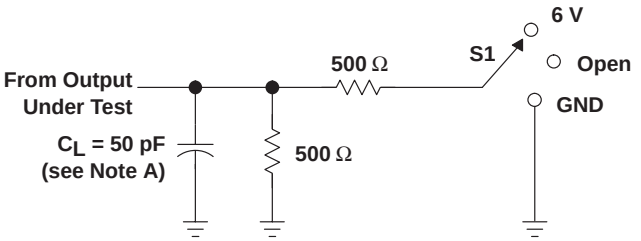


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

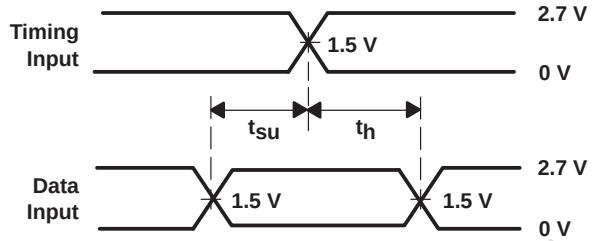
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

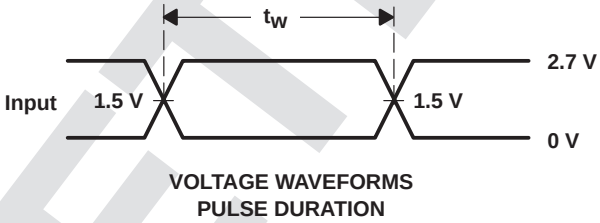


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

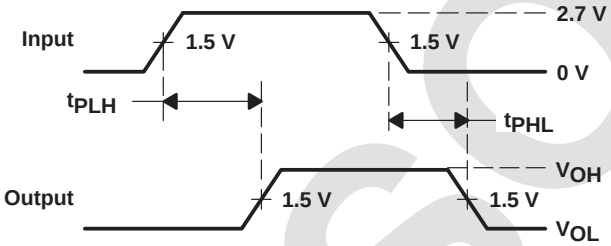
LOAD CIRCUIT



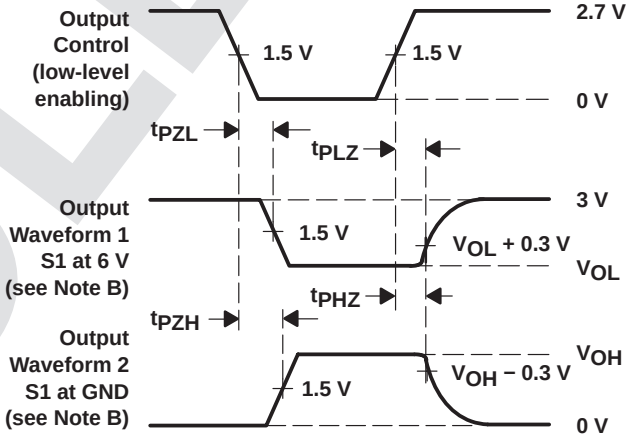
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74ALVC16501DL	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
SN74ALVC16501DLR	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI

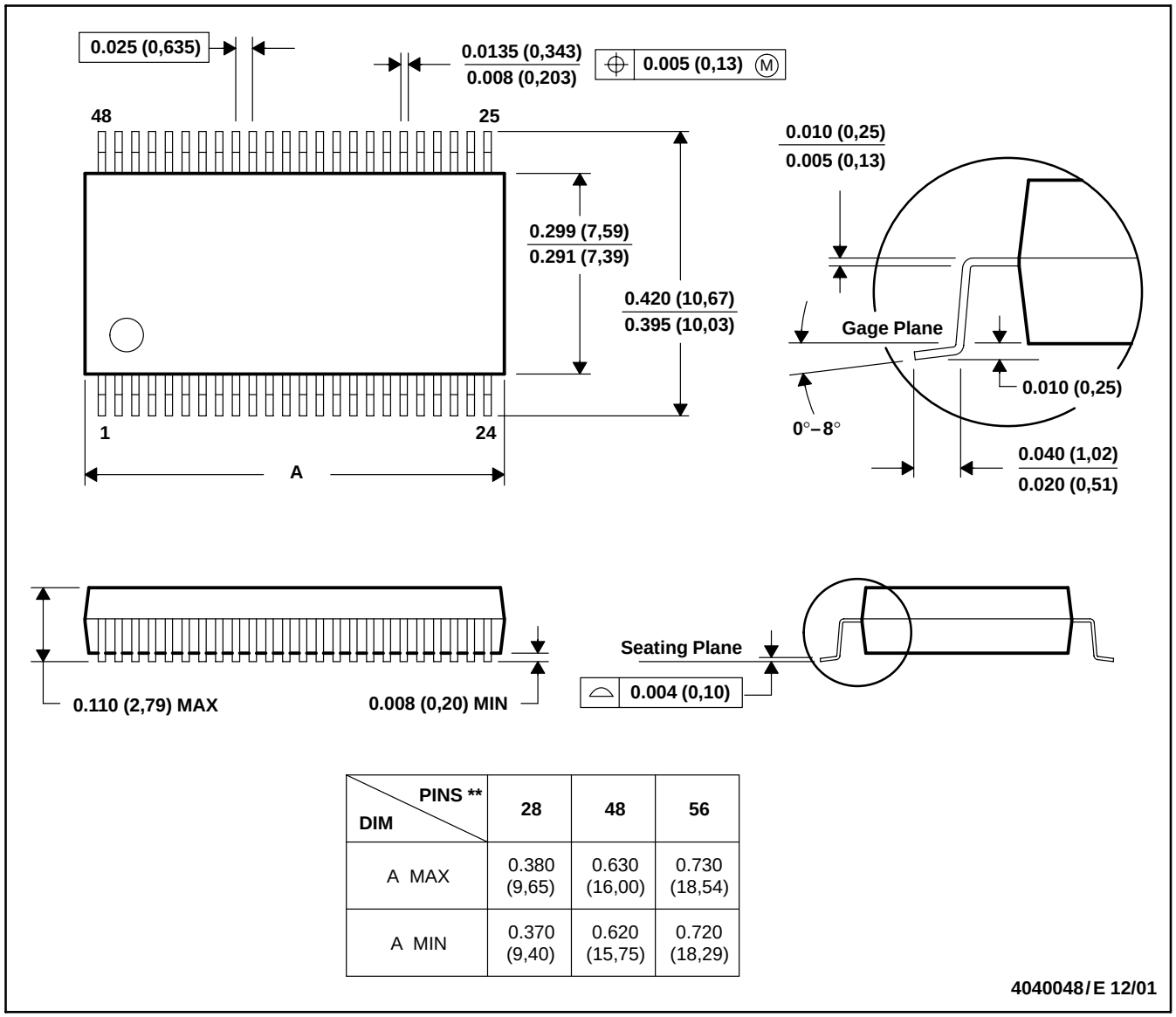
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048/E 12/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

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