

FEATURES

- Member of the Texas Instruments Widebus+™ Family
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- Max t_{pd} of 1.8 ns at 1.8 V
- Low Power Consumption, 40- μ A Max I_{CC}
- ± 8 -mA Output Drive at 1.8 V
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION/ORDERING INFORMATION

This 32-bit buffer/driver is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

The SN74AUCH32244 is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as eight 4-bit buffers, four 8-bit buffers, two 16-bit buffers, or one 32-bit buffer. It provides true outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------------------|---------------|-----------------------|------------------|
| -40°C to 85°C | LFBGA – GKE | Tape and reel | SN74AUCH32244GKER | MK244 |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



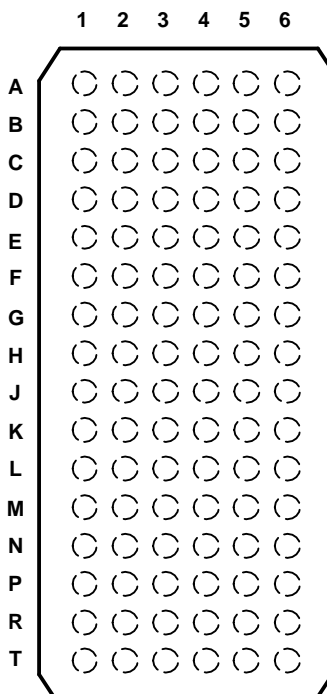
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SN74AUCH32244
32-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCES412B—SEPTEMBER 2002—REVISED JUNE 2005

GKE PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS

| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|-----|-----|-------------------|-------------------|-----|-----|
| A | 1Y2 | 1Y1 | 1 \overline{OE} | 2 \overline{OE} | 1A1 | 1A2 |
| B | 1Y4 | 1Y3 | GND | GND | 1A3 | 1A4 |
| C | 2Y2 | 2Y1 | V _{CC} | V _{CC} | 2A1 | 2A2 |
| D | 2Y4 | 2Y3 | GND | GND | 2A3 | 2A4 |
| E | 3Y2 | 3Y1 | GND | GND | 3A1 | 3A2 |
| F | 3Y4 | 3Y3 | V _{CC} | V _{CC} | 3A3 | 3A4 |
| G | 4Y2 | 4Y1 | GND | GND | 4A1 | 4A2 |
| H | 4Y3 | 4Y4 | 4 \overline{OE} | 3 \overline{OE} | 4A4 | 4A3 |
| J | 5Y2 | 5Y1 | 5 \overline{OE} | 6 \overline{OE} | 5A1 | 5A2 |
| K | 5Y4 | 5Y3 | GND | GND | 5A3 | 5A4 |
| L | 6Y2 | 6Y1 | V _{CC} | V _{CC} | 6A1 | 6A2 |
| M | 6Y4 | 6Y3 | GND | GND | 6A3 | 6A4 |
| N | 7Y2 | 7Y1 | GND | GND | 7A1 | 7A2 |
| P | 7Y4 | 7Y3 | V _{CC} | V _{CC} | 7A3 | 7A4 |
| R | 8Y2 | 8Y1 | GND | GND | 8A1 | 8A2 |
| T | 8Y3 | 8Y4 | 8 \overline{OE} | 7 \overline{OE} | 8A4 | 8A3 |

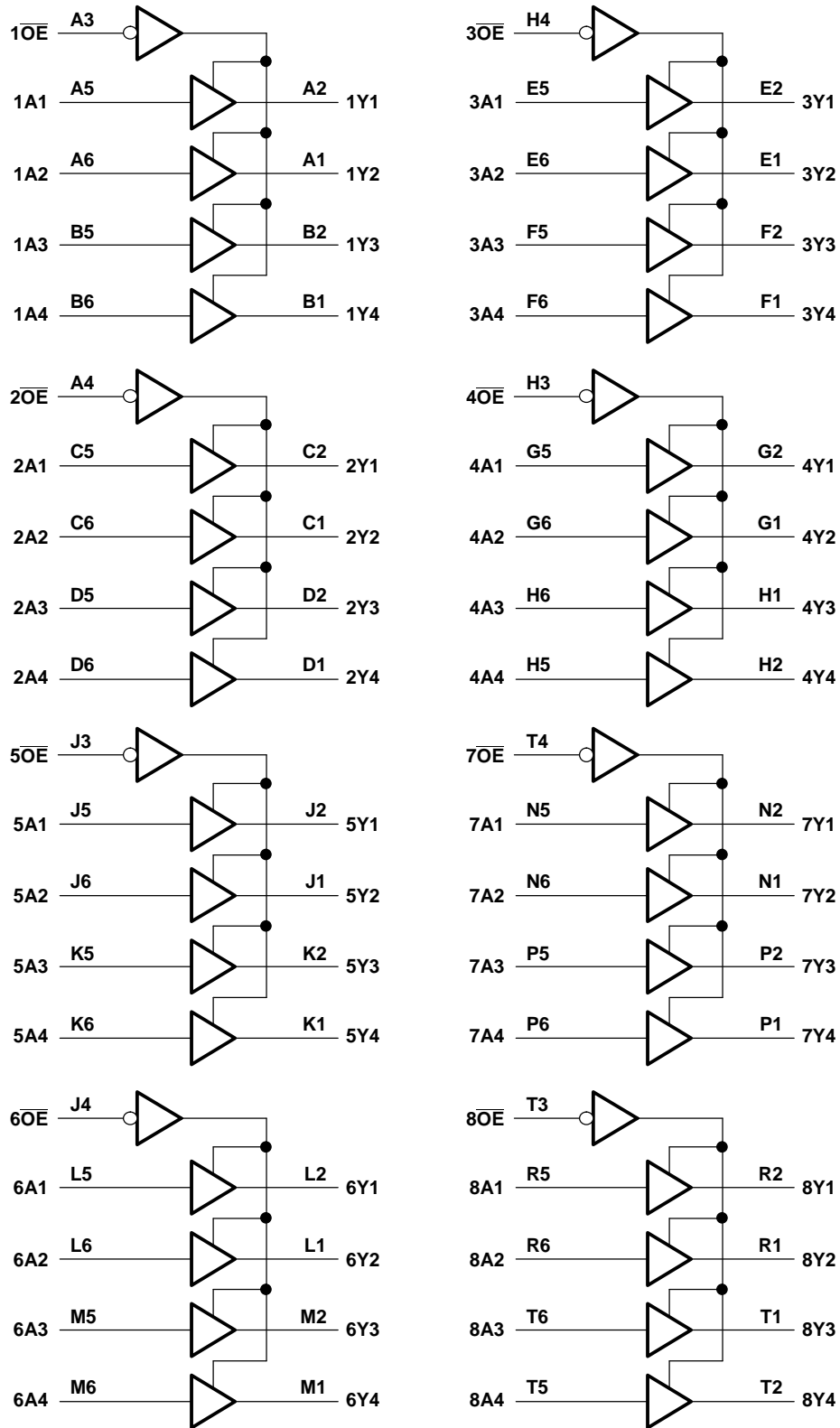
FUNCTION TABLE
(EACH 4-BIT BUFFER)

| INPUTS | | OUTPUT Y |
|-----------------|---|-------------|
| \overline{OE} | A | |
| L | H | H |
| L | L | L |

FUNCTION TABLE
(EACH 4-BIT BUFFER) (continued)

| INPUTS | | OUTPUT |
|-----------------|---|--------|
| \overline{OE} | A | Y |
| H | X | Z |

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---------------|---|-----------|------|----------------|------|
| V_{CC} | Supply voltage range | | -0.5 | 3.6 | V |
| V_I | Input voltage range ⁽²⁾ | | -0.5 | 3.6 | V |
| V_O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | | -0.5 | 3.6 | V |
| V_O | Output voltage range ⁽²⁾ | | -0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Input clamp current | $V_I < 0$ | | -50 | mA |
| I_{OK} | Output clamp current | $V_O < 0$ | | -50 | mA |
| I_O | Continuous output current | | | ± 20 | mA |
| | Continuous current through V_{CC} or GND | | | ± 100 | mA |
| θ_{JA} | Package thermal impedance ⁽³⁾ | | | 40 | °C/W |
| T_{stg} | Storage temperature range | | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

| | | | MIN | MAX | UNIT |
|---------------------|------------------------------------|-------------------------------------|-----|----------------------|------|
| V_{CC} | Supply voltage | | 0.8 | 2.7 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 0.8$ V | | V_{CC} | V |
| | | $V_{CC} = 1.1$ V to 1.95 V | | $0.65 \times V_{CC}$ | |
| | | $V_{CC} = 2.3$ V to 2.7 V | | 1.7 | |
| V_{IL} | Low-level input voltage | $V_{CC} = 0.8$ V | | 0 | V |
| | | $V_{CC} = 1.1$ V to 1.95 V | | $0.35 \times V_{CC}$ | |
| | | $V_{CC} = 2.3$ V to 2.7 V | | 0.7 | |
| V_I | Input voltage | | 0 | 3.6 | V |
| V_O | Output voltage | Active state | 0 | V_{CC} | V |
| | | 3-state | 0 | 3.6 | |
| I_{OH} | High-level output current | $V_{CC} = 0.8$ V | | -0.7 | mA |
| | | $V_{CC} = 1.1$ V | | -3 | |
| | | $V_{CC} = 1.4$ V | | -5 | |
| | | $V_{CC} = 1.65$ V | | -8 | |
| | | $V_{CC} = 2.3$ V | | -9 | |
| I_{OL} | Low-level output current | $V_{CC} = 0.8$ V | | 0.7 | mA |
| | | $V_{CC} = 1.1$ V | | 3 | |
| | | $V_{CC} = 1.4$ V | | 5 | |
| | | $V_{CC} = 1.65$ V | | 8 | |
| | | $V_{CC} = 2.3$ V | | 9 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC} = 0.8$ V | | 20 | ns/V |
| | | $V_{CC} = 1.3$ V | | 15 | |
| | | $V_{CC} = 1.6$ V, 1.95 V, and 2.7 V | | 10 | |
| T_A | Operating free-air temperature | | -40 | 85 | °C |

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74AUCH32244
32-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCES412B–SEPTEMBER 2002–REVISED JUNE 2005

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|----------------------------------|---------------------------------------|---|-----------------|-----------------------|--------------------|------|------|
| V _{OH} | | I _{OH} = –100 μA | 0.8 V to 2.7 V | V _{CC} – 0.1 | | | V |
| | | I _{OH} = –0.7 mA | 0.8 V | 0.55 | | | |
| | | I _{OH} = –3 mA | 1.1 V | 0.8 | | | |
| | | I _{OH} = –5 mA | 1.4 V | 1 | | | |
| | | I _{OH} = –8 mA | 1.65 V | 1.2 | | | |
| | | I _{OH} = –9 mA | 2.3 V | 1.8 | | | |
| V _{OL} | | I _{OL} = 100 μA | 0.8 V to 2.7 V | | | 0.2 | V |
| | | I _{OL} = 0.7 mA | 0.8 V | 0.25 | | | |
| | | I _{OL} = 3 mA | 1.1 V | | | 0.3 | |
| | | I _{OL} = 5 mA | 1.4 V | | | 0.4 | |
| | | I _{OL} = 8 mA | 1.65 V | | | 0.45 | |
| | | I _{OL} = 9 mA | 2.3 V | | | 0.6 | |
| I _I | A or \overline{OE} inputs | V _I = V _{CC} or GND | 0 to 2.7 V | | | ±5 | μA |
| I _{BHL} ⁽²⁾ | | V _I = 0.35 V | 1.1 V | 10 | | | μA |
| | | V _I = 0.47 V | 1.4 V | 15 | | | |
| | | V _I = 0.57 V | 1.65 V | 20 | | | |
| | | V _I = 0.7 V | 2.3 V | 40 | | | |
| I _{BHH} ⁽³⁾ | | V _I = 0.8 V | 1.1 V | –10 | | | μA |
| | | V _I = 0.9 V | 1.4 V | –15 | | | |
| | | V _I = 1.07 V | 1.65 V | –20 | | | |
| | | V _I = 1.7 V | 2.3 V | –40 | | | |
| I _{BHLO} ⁽⁴⁾ | V _I = 0 to V _{CC} | | 1.3 V | 75 | | | μA |
| | | | 1.6 V | 125 | | | |
| | | | 1.95 V | 175 | | | |
| | | | 2.7 V | 275 | | | |
| I _{BHHO} ⁽⁵⁾ | V _I = 0 to V _{CC} | | 1.3 V | –75 | | | μA |
| | | | 1.6 V | –125 | | | |
| | | | 1.95 V | –175 | | | |
| | | | 2.7 V | –275 | | | |
| I _{off} | | V _I or V _O = 2.7 V | 0 | | | ±10 | μA |
| I _{OZ} | | V _O = V _{CC} or GND | 2.7 V | | | ±10 | μA |
| I _{CC} | | V _I = V _{CC} or GND, I _O = 0 | 0.8 V to 2.7 V | | | 40 | μA |
| C _i | | V _I = V _{CC} or GND | 2.5 V | | 3 | 4.5 | pF |
| C _o | | V _O = V _{CC} or GND | 2.5 V | | 4 | 7 | pF |

- (1) All typical values are at T_A = 25°C.
- (2) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.
- (3) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.
- (4) An external driver must source at least I_{BHLO} to switch this node from low to high.
- (5) An external driver must sink at least I_{BHHO} to switch this node from high to low.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

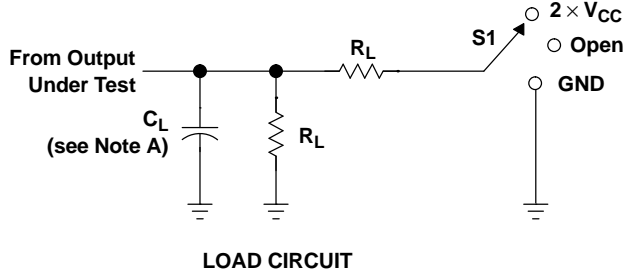
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 0.8 V | V _{CC} = 1.2 V ± 0.1 V | | V _{CC} = 1.5 V ± 0.1 V | | V _{CC} = 1.8 V ± 0.15 V | | | V _{CC} = 2.5 V ± 0.2 V | | UNIT |
|------------------|-----------------|----------------|-------------------------|------------------------------------|-----|------------------------------------|-----|-------------------------------------|-----|-----|------------------------------------|-----|------|
| | | | TYP | MIN | MAX | MIN | MAX | MIN | TYP | MAX | MIN | MAX | |
| t _{pd} | A | Y | 5.4 | 0.8 | 2.8 | 0.6 | 1.9 | 0.7 | 1.3 | 1.8 | 0.5 | 1.8 | ns |
| t _{en} | \overline{OE} | Y | 8 | 1 | 4.4 | 0.7 | 2.6 | 0.8 | 1.4 | 2.5 | 0.6 | 1.9 | ns |
| t _{dis} | \overline{OE} | Y | 12 | 1.9 | 4.9 | 1 | 4.6 | 1.5 | 2.6 | 4 | 0.5 | 2 | ns |

Operating Characteristics

T_A = 25°C

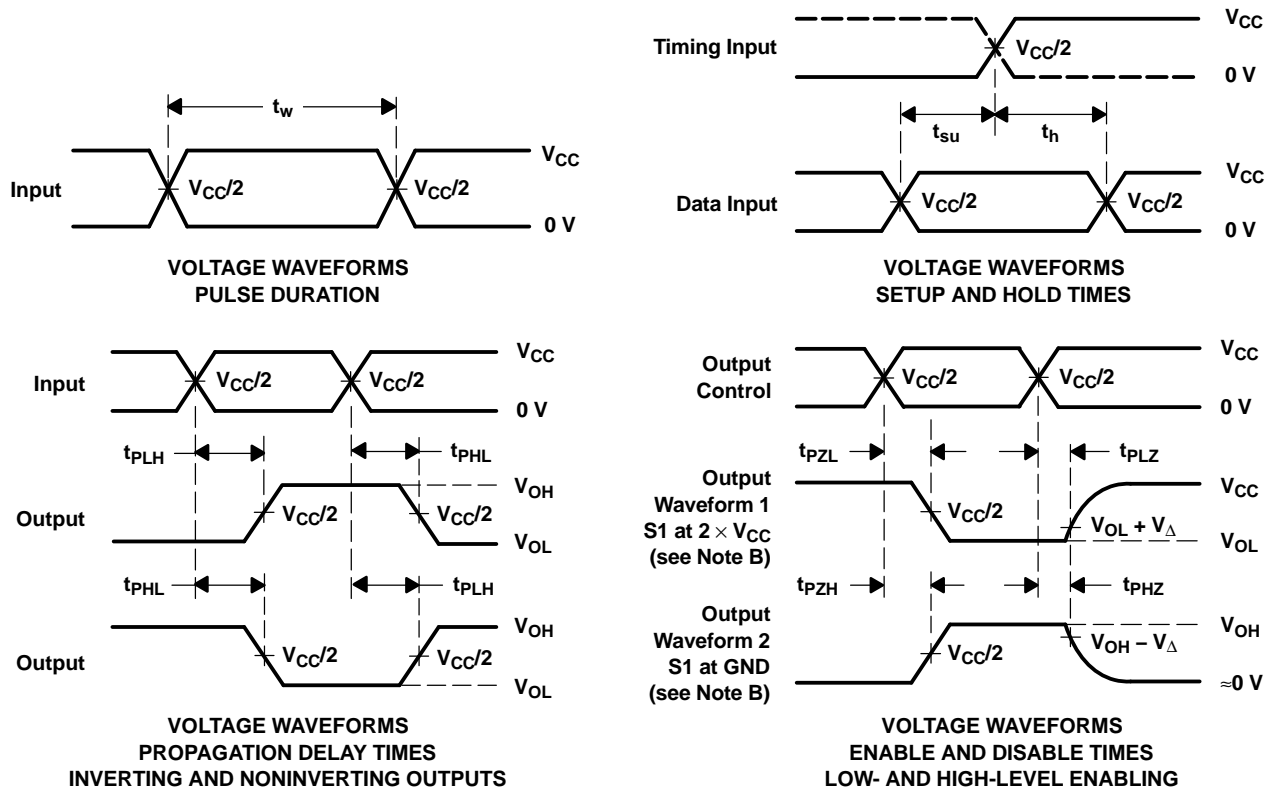
| PARAMETER | | TEST CONDITIONS | V _{CC} = 0.8 V | V _{CC} = 1.2 V | V _{CC} = 1.5 V | V _{CC} = 1.8 V | V _{CC} = 2.5 V | UNIT |
|-----------------|-------------------------------------|----------------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|------|
| | | | TYP | TYP | TYP | TYP | TYP | |
| C _{pd} | Power dissipation capacitance | Outputs enabled f = 10 MHz | 21 | 22 | 23 | 25 | 30 | pF |
| | Outputs disabled | | 1 | 1 | 1 | 1 | 1 | |

PARAMETER MEASUREMENT INFORMATION



| TEST | S1 |
|-------------------|-------------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | C_L | R_L | V_{Δ} |
|--------------------|-------|--------------|--------------|
| 0.8 V | 15 pF | 2 k Ω | 0.1 V |
| 1.2 V \pm 0.1 V | 15 pF | 2 k Ω | 0.1 V |
| 1.5 V \pm 0.1 V | 15 pF | 2 k Ω | 0.1 V |
| 1.8 V \pm 0.15 V | 30 pF | 1 k Ω | 0.15 V |
| 2.5 V \pm 0.2 V | 30 pF | 500 Ω | 0.15 V |



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, slew rate \geq 1 V/ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|-------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74AUCH32244GKER | NRND | LFBGA | GKE | 96 | 1000 | TBD | SNPB | Level-2-235C-1 YEAR |
| SN74AUCH32244ZKER | ACTIVE | LFBGA | ZKE | 96 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AUCH32244GKER | LFBGA | GKE | 96 | 1000 | 330.0 | 24.4 | 5.7 | 13.7 | 2.0 | 8.0 | 24.0 | Q1 |
| SN74AUCH32244ZKER | LFBGA | ZKE | 96 | 1000 | 330.0 | 24.4 | 5.7 | 13.7 | 2.0 | 8.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

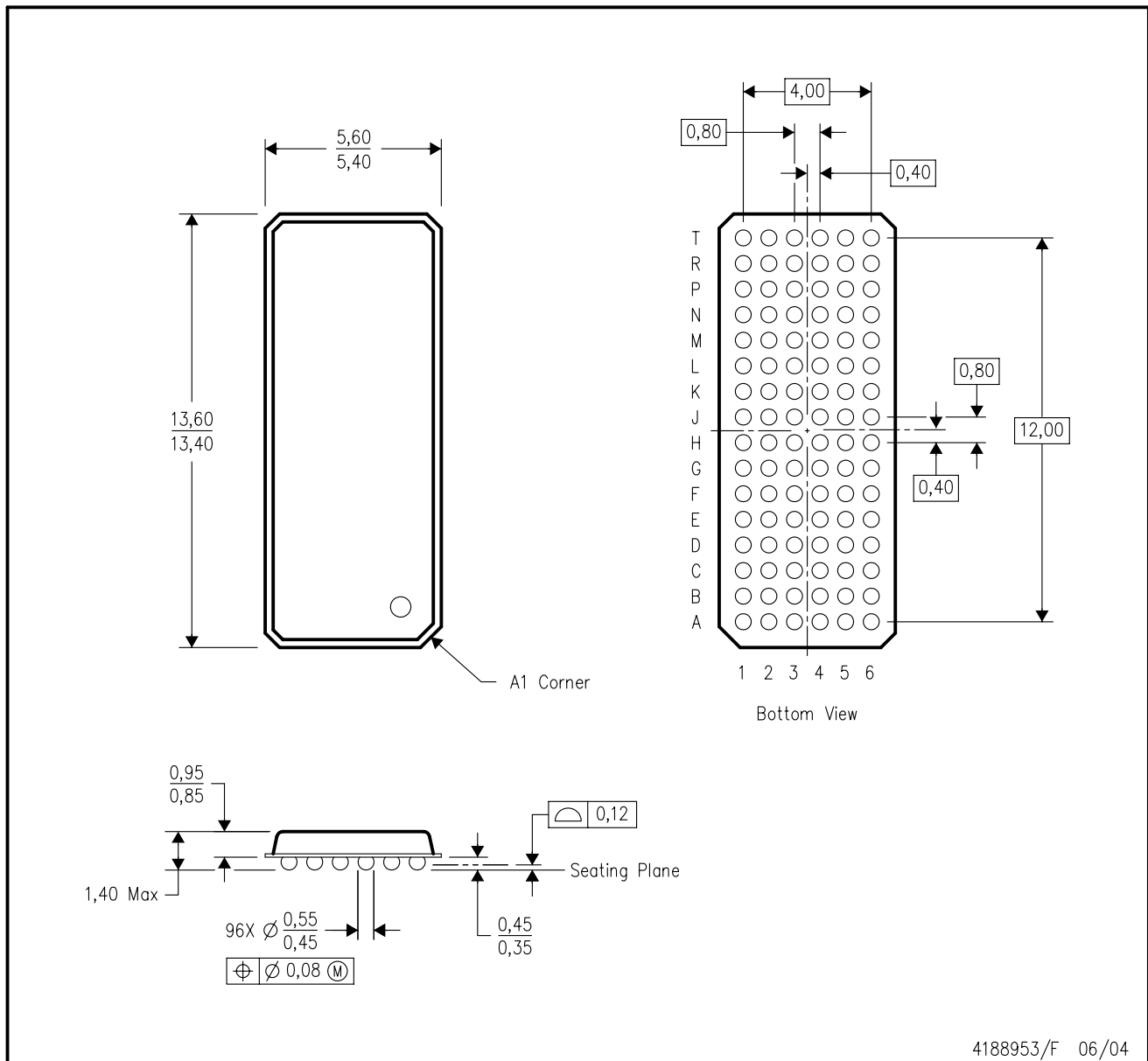


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AUCH32244GKER | LFBGA | GKE | 96 | 1000 | 333.2 | 345.9 | 31.8 |
| SN74AUCH32244ZKER | LFBGA | ZKE | 96 | 1000 | 333.2 | 345.9 | 31.8 |

GKE (R-PBGA-N96)

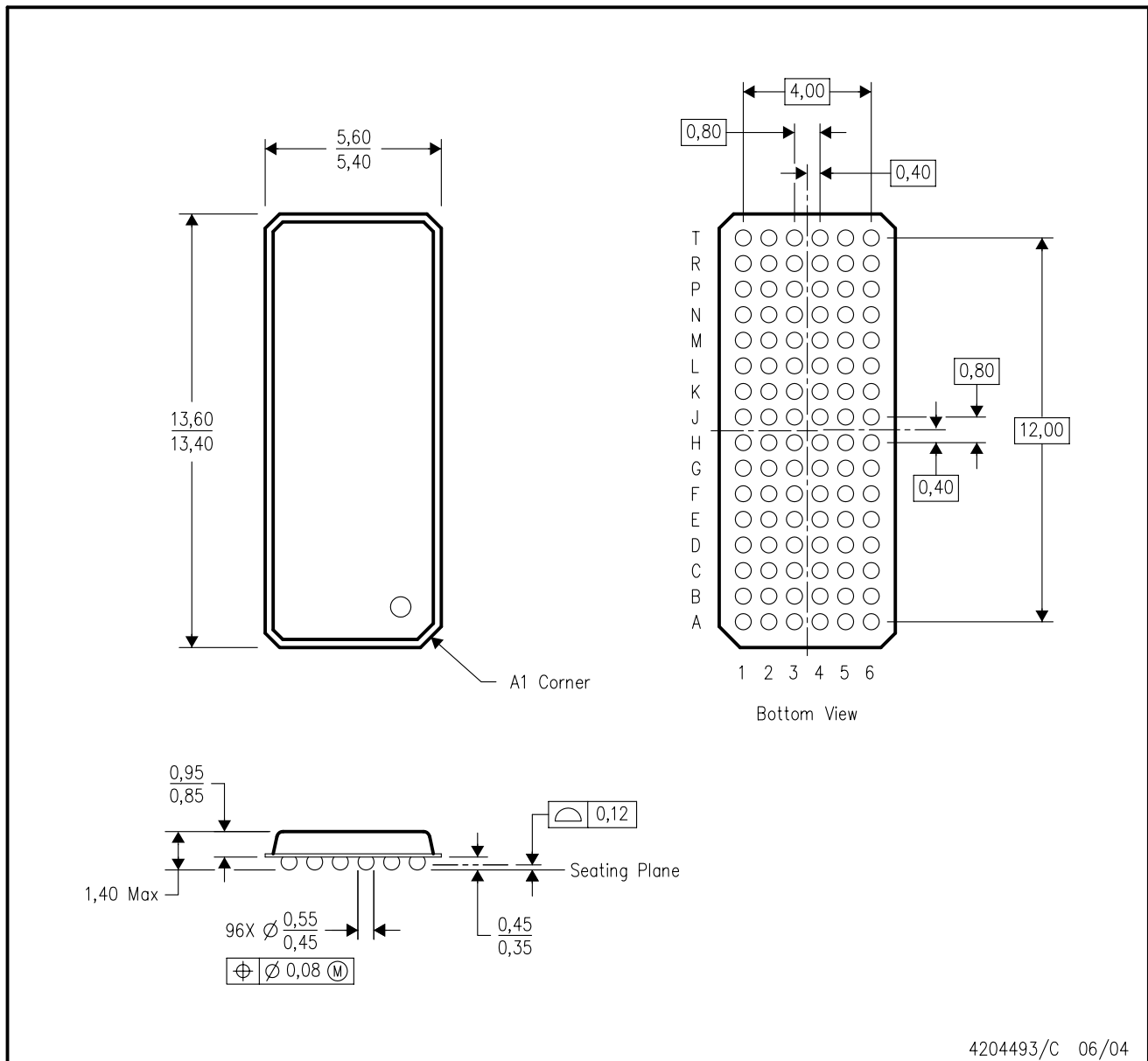
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-205 variation CC.
 - D. This package is tin-lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead-free.

ZKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-205 variation CC.
 - D. This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).

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