SN74BCT760-EP
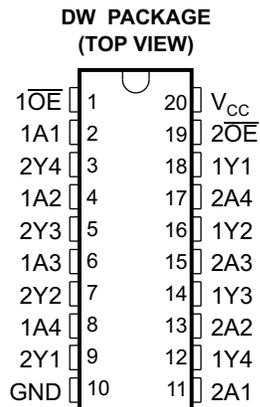# OCTAL BUFFER/DRIVER
WITH OPEN-COLLECTOR OUTPUTS

FEATURES

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of −55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** [1]
- **Open-Collector Version of 'BCT244**
- **Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C Method 3015**
- **Available In Plastic Small-Outline (DW) Package**

[1] Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

DW PACKAGE
(TOP VIEW)

1$\overline{OE}$	1	20	V_{CC}
1A1	2	19	2$\overline{OE}$
2Y4	3	18	1Y1
1A2	4	17	2A4
2Y3	5	16	1Y2
1A3	6	15	2A3
2Y2	7	14	1Y3
1A4	8	13	2A2
2Y1	9	12	1Y4
GND	10	11	2A1

DESCRIPTION/ORDERING INFORMATION

The SN74BCT760 octal buffer and line driver is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74BCT760 is organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The device is characterized for operation over the full military temperature range of −55°C to 125°C.

ORDERING INFORMATION

T_A	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−55°C to 125°C	SOIC – DW	Tape and reel	SN74BCT760MDWREP	BCT760MEP

[1] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each buffer)

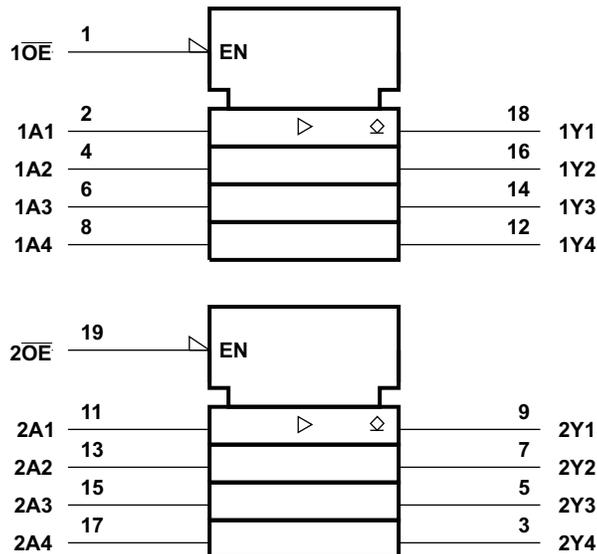| INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	H

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74BCT760-EP
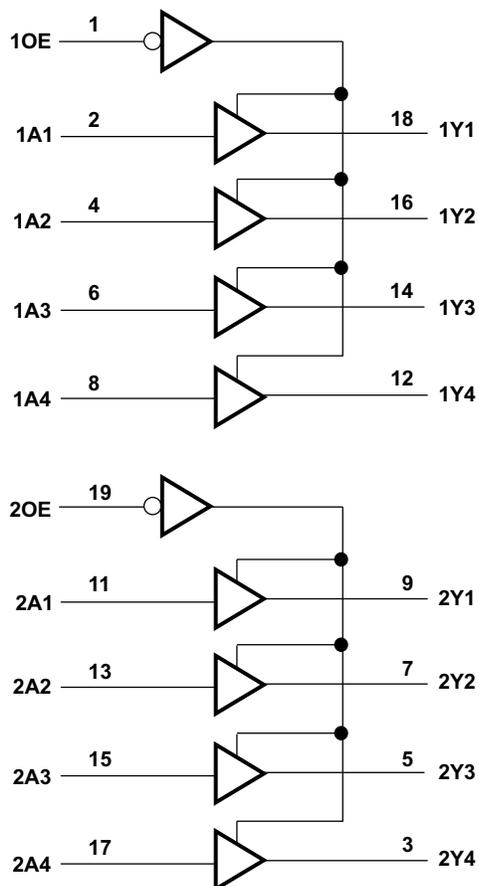## OCTAL BUFFER/DRIVER
WITH OPEN-COLLECTOR OUTPUTS

SCBS817B−JULY 2006−REVISED SEPTEMBER 2006

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LOGIC SYMBOL[1]

1OE — 1 — EN		
1A1 — 2	▷ ◇	18 — 1Y1
1A2 — 4		16 — 1Y2
1A3 — 6		14 — 1Y3
1A4 — 8		12 — 1Y4

2OE — 19 — EN		
2A1 — 11	▷ ◇	9 — 2Y1
2A2 — 13		7 — 2Y2
2A3 — 15		5 — 2Y3
2A4 — 17		3 — 2Y4

(1)   This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM (POSITIVE LOGIC)

1OE	1
1A1	2 — 18 — 1Y1
1A2	4 — 16 — 1Y2
1A3	6 — 14 — 1Y3
1A4	8 — 12 — 1Y4

2OE	19
2A1	11 — 9 — 2Y1
2A2	13 — 7 — 2Y2
2A3	15 — 5 — 2Y3
2A4	17 — 3 — 2Y4

Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	−0.5	7	V
V_I	Input voltage range[2]	−0.5	7	V
I_I	Input current range	−30	5	mA
V_O	Voltage range applied to any output in the disabled or power-off state	−0.5	5.5	V
V_O	Voltage range applied to any output in the high state	−0.5	V_{CC}	V
	Current into any output in the low state		96	mA
	Operating free-air temperature range[3]	−55	125	°C
T_{stg}	Storage temperature range	−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The negative input voltage rating may be exceeded if the input clamp current rating is observed.
(3) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage			5.5	V
I_{IK}	Input clamp current			−18	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	−55		125	°C

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.38	0.55	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−1	mA
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1	mA
I_{CC}	V_{CC} = 5.5 V,	Outputs open	Outputs high		21	33	mA
			Outputs low		48	76	
			$\overline{OE}$ disabled		6	10	
C_i	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		6		pF
C_o	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		10		pF

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

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Switching Characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX[1]		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	Any A	Y	6.3	8	9.5	6.3	11.1	ns
t_{PHL}			2.1	4.3	6.5	2.1	7.7	
t_{PLH}	$\overline{OE}$	Y	8.6	13	15.2	8.6	18.7	ns
t_{PHL}			3.2	6.2	8.9	3.2	10.4	

(1) For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

SN74BCT760MDWREP Operating Life Derating Chart
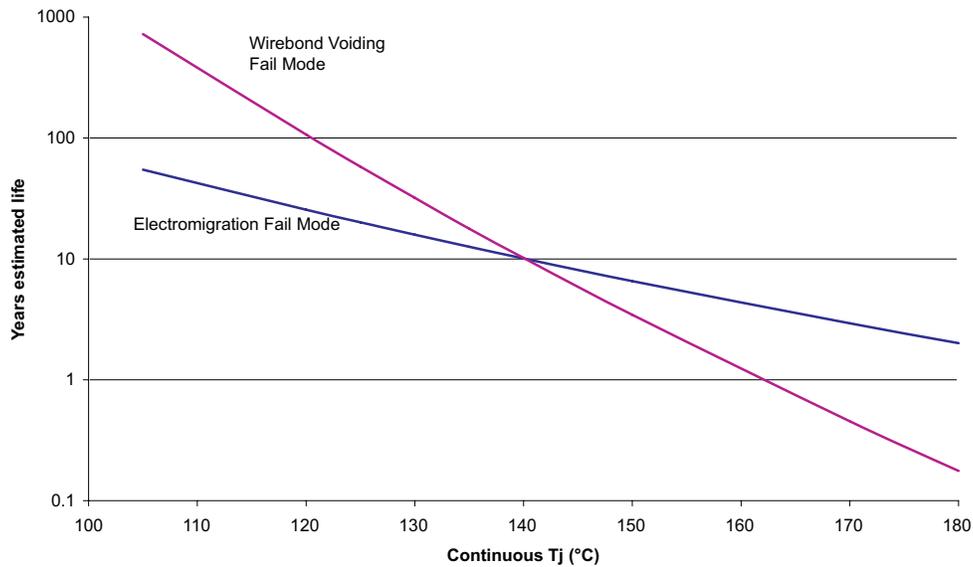
A. See datasheet for absolute maximum ratings and minimum recommended operating conditions.

B. Silicon operating life design goal is 10 years at 10°C junction temperature (does not include package interconnect life).

C. Enhanced plastic product disclaimer applies.

PARAMETER MEASUREMENT INFORMATION
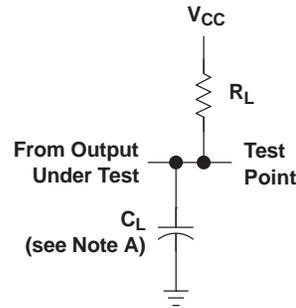
**LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS**
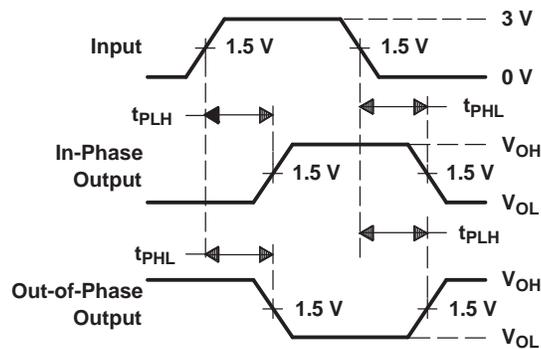
**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

A. C_L includes probe and jig capacitance.

B.   All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.

C.   The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

![Texas Instruments logo]

24-Jan-2013

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74BCT760MDWREP	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	BCT760MEP	Samples
V62/06672-01XE	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	BCT760MEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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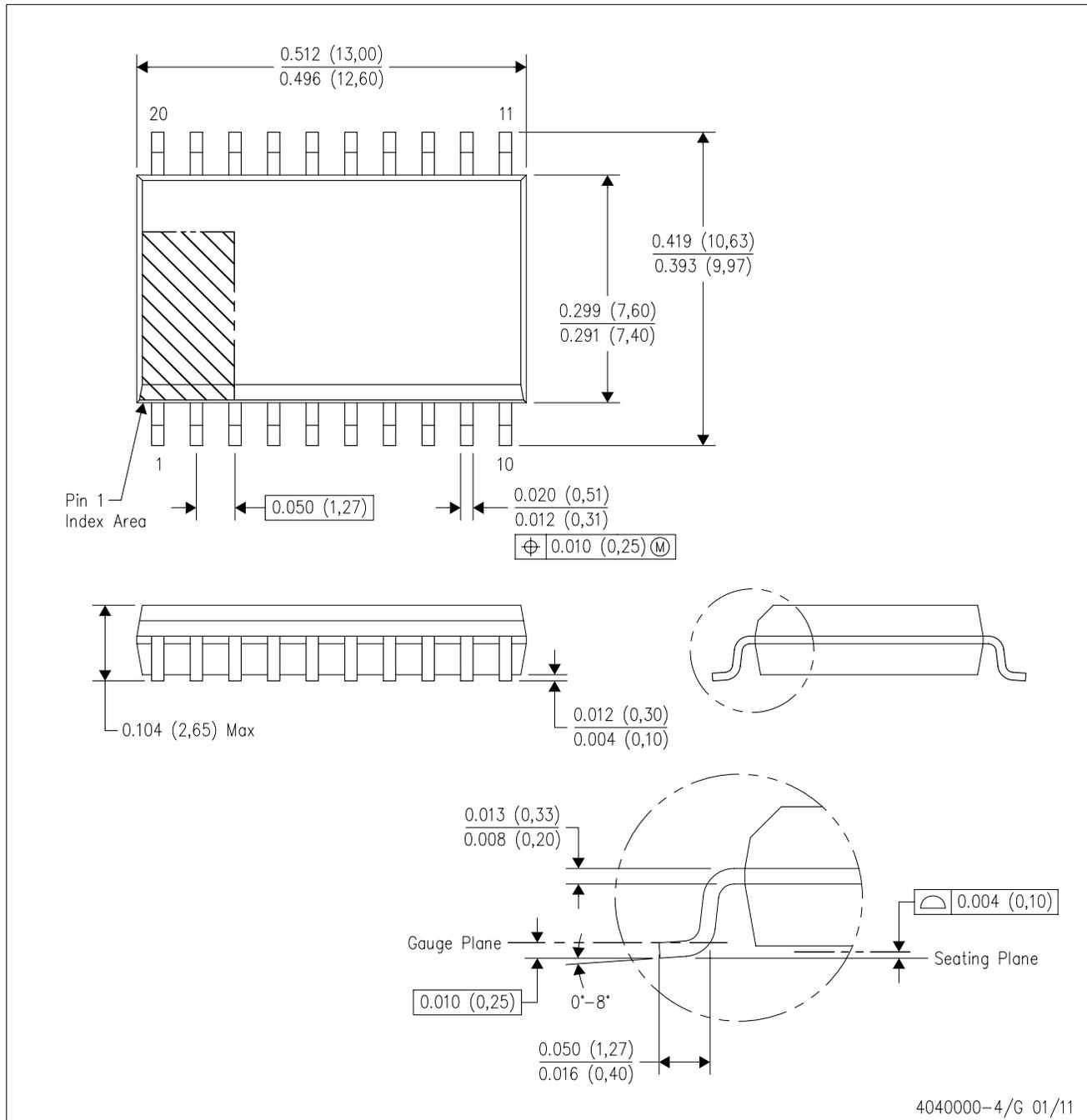**OTHER QUALIFIED VERSIONS OF SN74BCT760-EP :**

● Catalog: SN74BCT760

● Military: SN54BCT760

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications
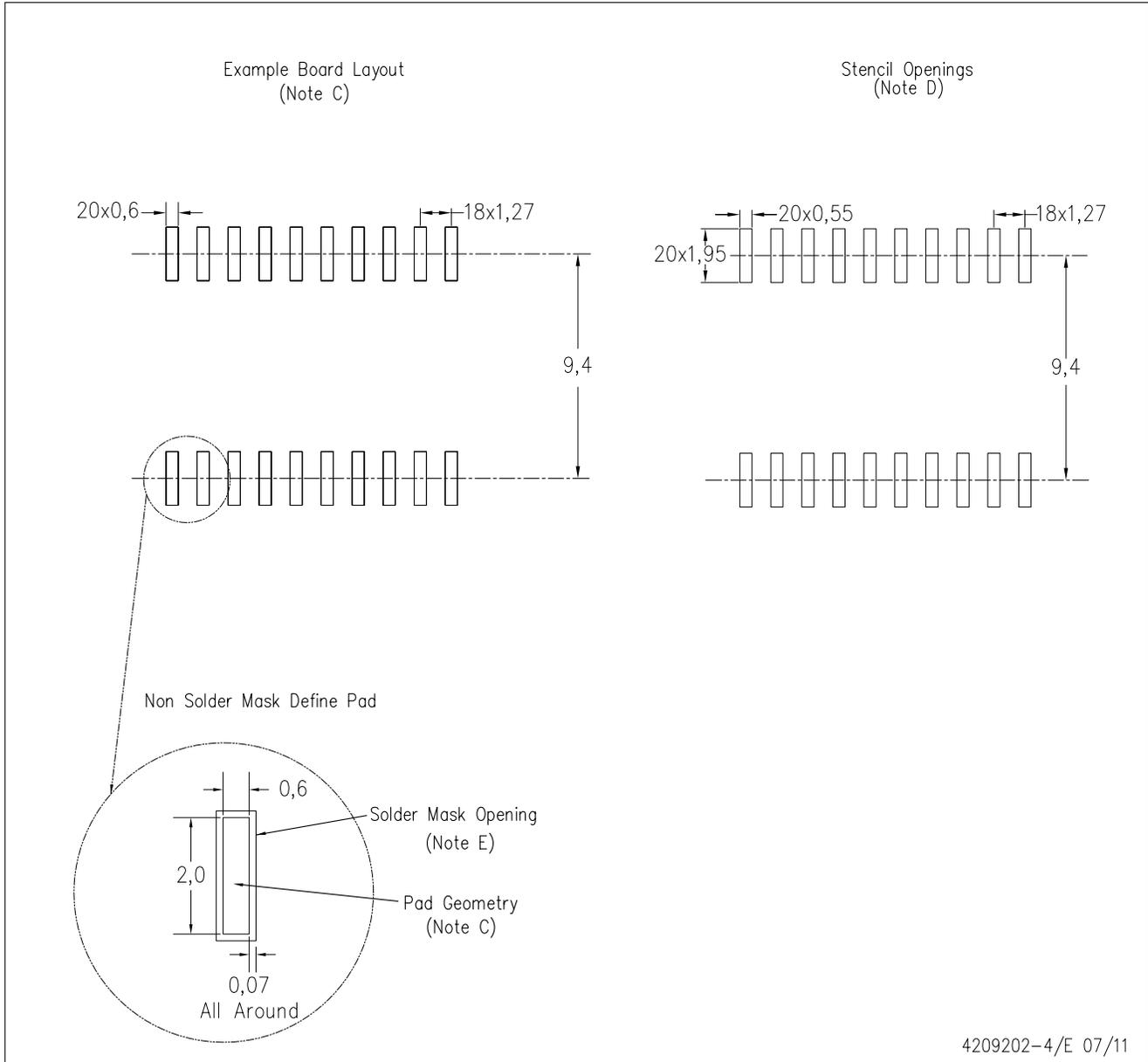
DW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

0.512 (13,00)
0.496 (12,60)

20   11

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   10

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040000−4/G 01/11

NOTES: A.   All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−013 variation AC.

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DW (R-PDSO-G20)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

20x0,6 → | ←   → | ← 18x1,27

20x0,55 → | ←   → | ← 18x1,27

20x1,95

9,4

9,4

Non Solder Mask Define Pad

← 0,6 →

Solder Mask Opening
(Note E)

2,0

Pad Geometry
(Note C)

0,07
All Around

4209202-4/E 07/11

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Refer to IPC7351 for alternate board design.

         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC-7525

         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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