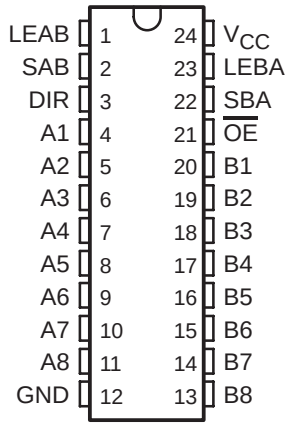
- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch Version of the ′BCT646**
- **Independent Latches and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (NT)**

DW OR NT PACKAGE
(TOP VIEW)



description

The SN74BCT956 consists of bus transceiver circuits, D-type latches, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal latches. Data on the A or B bus is stored in the latches when the appropriate latch-enable (LEAB or LEBA) input is low. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74BCT956.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode ($\overline{OE}$ low), data present at the high-impedance port may be stored in either latch or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. When the appropriate latch-enable input is high, the latch is transparent, and real-time data is output regardless of the level at the select control.

The direction control (DIR) determines which bus receives data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN74BCT956 is characterized for operation from 0°C to 70°C.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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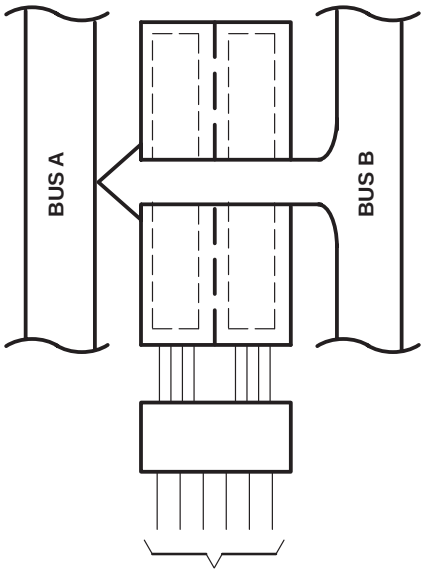
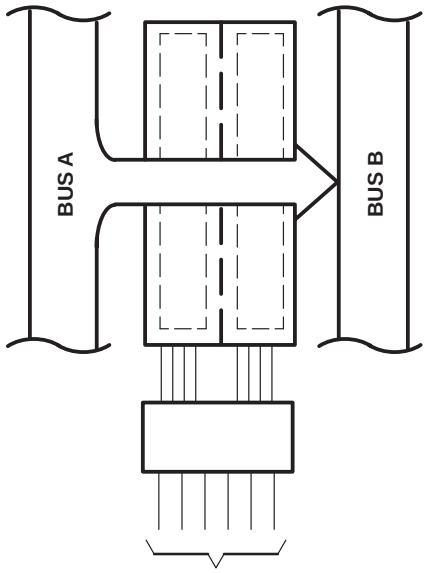


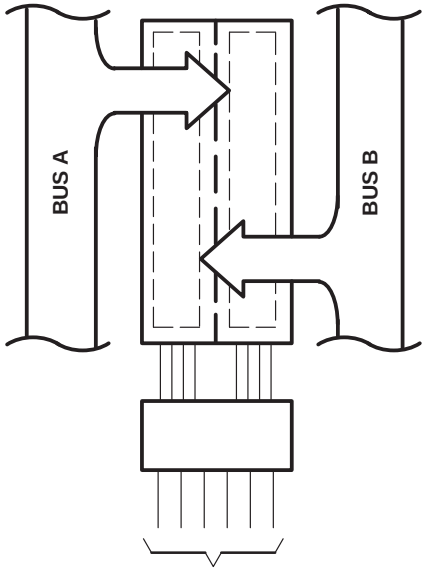
21 $\overline{OE}$	3 DIR	1 LEAB	23 LEBA	2 SAB	22 SBA	
L	L	X	X	X	L	(Thru)
L	L	X	H	X	H	(Latch)

REAL-TIME TRANSFER
BUS B TO BUS A



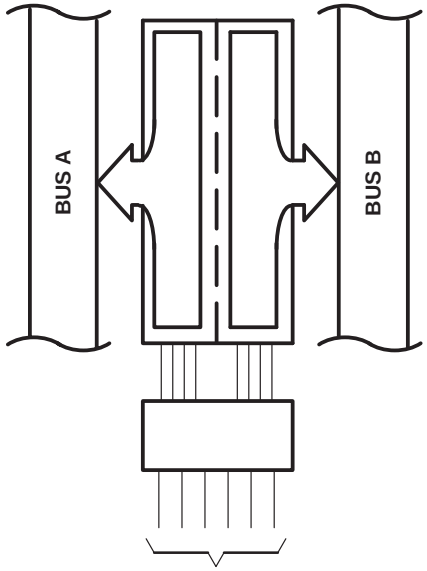
21 $\overline{OE}$	3 DIR	1 LEAB	23 LEBA	2 SAB	22 SBA	
L	H	X	X	L	X	(Thru)
L	H	H	X	H	X	(Latch)

REAL-TIME TRANSFER
BUS A TO BUS B



21 $\overline{OE}$	3 DIR	1 LEAB	23 LEBA	2 SAB	22 SBA
X	X	L	X	X	X
X	X	X	L	X	X
H	X	L	L	X	X

STORAGE FROM
A, B, OR A AND B



21 $\overline{OE}$	3 DIR	1 LEAB	23 LEBA	2 SAB	22 SBA
L	L	X	L	X	H
L	H	L	X	H	X

TRANSFER STORED DATA
TO A OR B

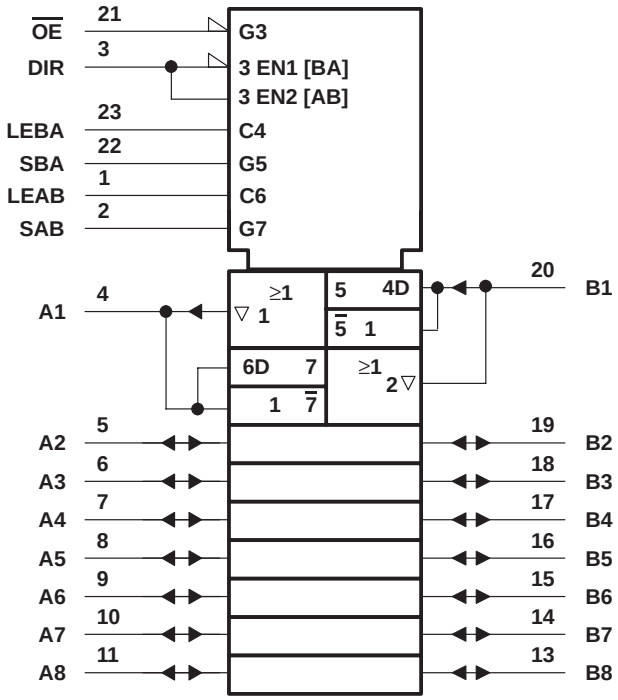
Figure 1. Bus-Management Functions

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	LEAB	LEBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	L	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	L	X	X	Unspecified†	Input	Store B, A unspecified†
L	H	X	X	L	X	Input	Output	A transparent, real-time A data to B bus (thru)
L	H	H	X	H	X	Input	Output	A transparent, real-time A data to B bus (latch)
L	H	L	X	L	X	Input	Output	A data latched, real-time A data to B bus (thru)
L	H	L	X	H	X	Input	Output	A data latched, latched A data to B bus (latch)
L	L	X	X	X	L	Output	Input	B transparent, real-time B data to A bus (thru)
L	L	X	H	X	H	Output	Input	B transparent, real-time B data to A bus (latch)
L	L	X	L	X	L	Output	Input	B data latched, real-time B data to A bus (thru)
L	L	X	L	X	H	Output	Input	B data latched, latched B data to A bus (latch)
H	X	L	L	X	X	Input	Input	Isolation, A and B data latched
H	X	H	H	X	X	Input	Input	Isolation, no storage

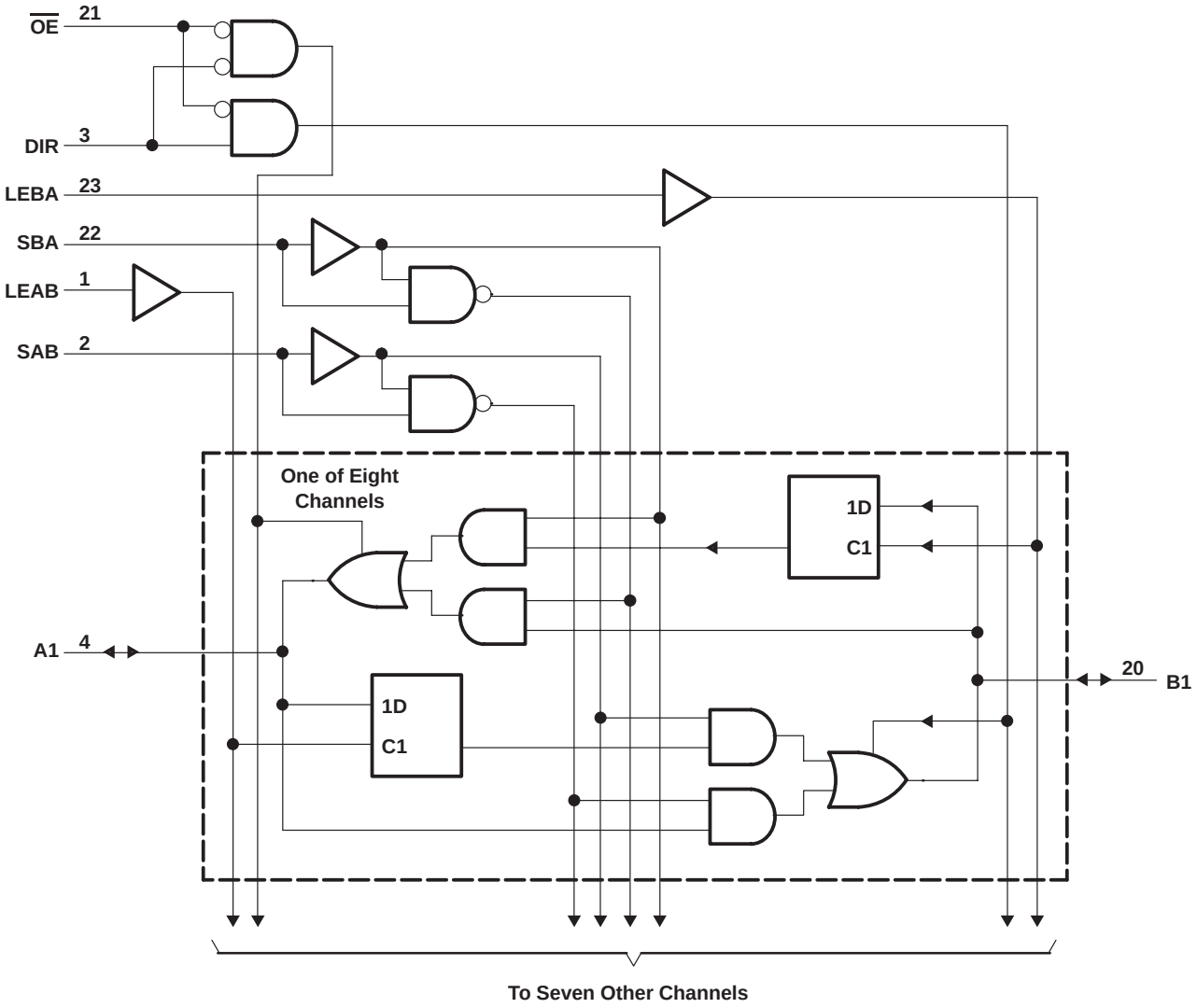
† The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins is latched whenever the appropriate latch-enable input is low.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O . . . . . −0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O . . . . . −0.5 V to V_{CC}
Input clamp current, I_{IK} (V_I < 0) . . . . . −30 mA
Current into any output in the low state, I_O . . . . . 128 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		V
			I_{OH} = −15 mA	2	3.1		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 64 mA		0.42	0.55	V
I_I	Any input	V_{CC} = 5.5 V,	V_I = 5.5 V			1	mA
I_{IH}‡	A or B ports	V_{CC} = 5.5 V,	V_I = 2.7 V			70	µA
	Control input					20	
I_{IL}‡	Any input	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.7	mA
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0	−100		−225	mA
I_{CCL}		V_{CC} = 5.5 V,	Outputs open		42	67	mA
I_{CCH}		V_{CC} = 5.5 V,	Outputs open		5	8	mA
I_{CCZ}		V_{CC} = 5.5 V,	Outputs open		6.7	11	mA
C_i	Control input	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		5		pF
C_{io}	A to B	V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V		11		pF
	B to A				11		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration, LE high		4		4		ns
t_{su}	Setup time, data before LE↓	High	0		0		ns
		Low	3		3		
t_h	Hold time, data after LE↓	High	0		0		ns
		Low	2.5		2.5		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B SAB or SBA high (latch)	B or A	2.2	5.1	7.3	2.2	8.3	ns
t_{PHL}			3.6	6.7	10	3.6	11.7	
t_{PLH}	A or B SAB or SBA low (thru)	B or A	2	5.1	7.2	2	8.2	ns
t_{PHL}			3.3	6.7	9.3	3.3	11.1	
t_{PLH}	LEBA or LEAB	A or B	2.2	5.5	7.9	2.2	9.3	ns
t_{PHL}			2.9	6	8.5	2.9	9.8	
t_{PLH}	SAB or SBA† A or B high	B or A	3.7	6.8	10.6	3.7	13.3	ns
t_{PHL}			2.6	5.3	7.4	2.6	8.2	
t_{PLH}	SAB or SBA† A or B low	B or A	3.2	7.4	9.5	3.2	11.2	ns
t_{PHL}			3.8	7.7	10.1	3.8	12.2	
t_{PZH}	$\overline{OE}$	A or B	3.1	6.9	9.5	3.1	11.7	ns
t_{PZL}			3.9	7.8	10.7	3.9	13.1	
t_{PHZ}	$\overline{OE}$	A or B	3.5	6.6	8.9	3.5	10.7	ns
t_{PLZ}			2.6	5.9	8.3	2.6	9.5	
t_{PZH}	DIR	A or B	2.1	5	9.8	2.1	12	ns
t_{PZL}			2.9	6	10.9	2.9	13.1	
t_{PHZ}	DIR	A or B	3.6	6.3	10.2	3.6	12.5	ns
t_{PLZ}			2.5	5.7	8.9	2.5	10.8	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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