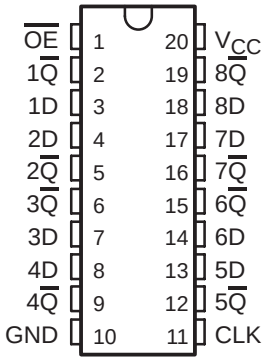
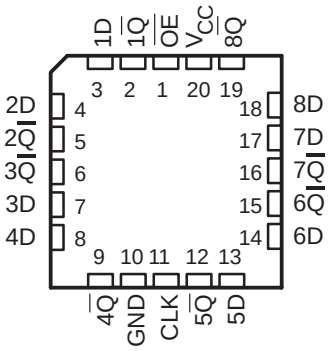
- **3-State Bus-Driving Inverting Outputs**
- **Buffered Control Inputs**
- **Package Options Incude Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54F534A . . . J PACKAGE
SN74F534A . . . DW OR N PACKAGE
(TOP VIEW)



SN54F534A . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ′F534A are edge-triggered D-type flip-flops. On the positive transition of the clock, the $\overline{Q}$ outputs are set to the complement of the logic states that were set up at the data (D) inputs. The ′F534A is equivalent to the ′F374 except for having inverted outputs.

A buffered output enable ($\overline{OE}$) control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output enable ($\overline{OE}$) does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN54F534A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F534A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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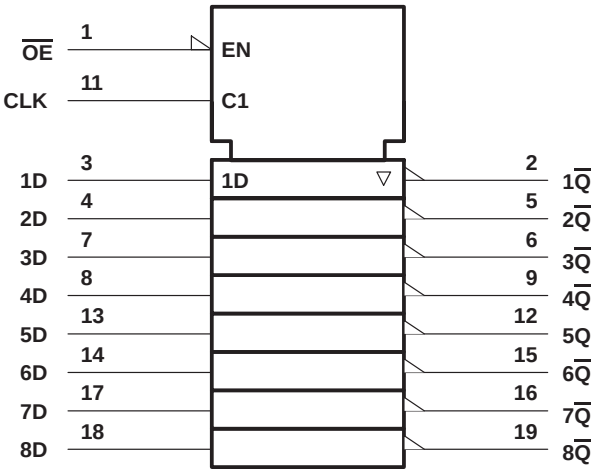
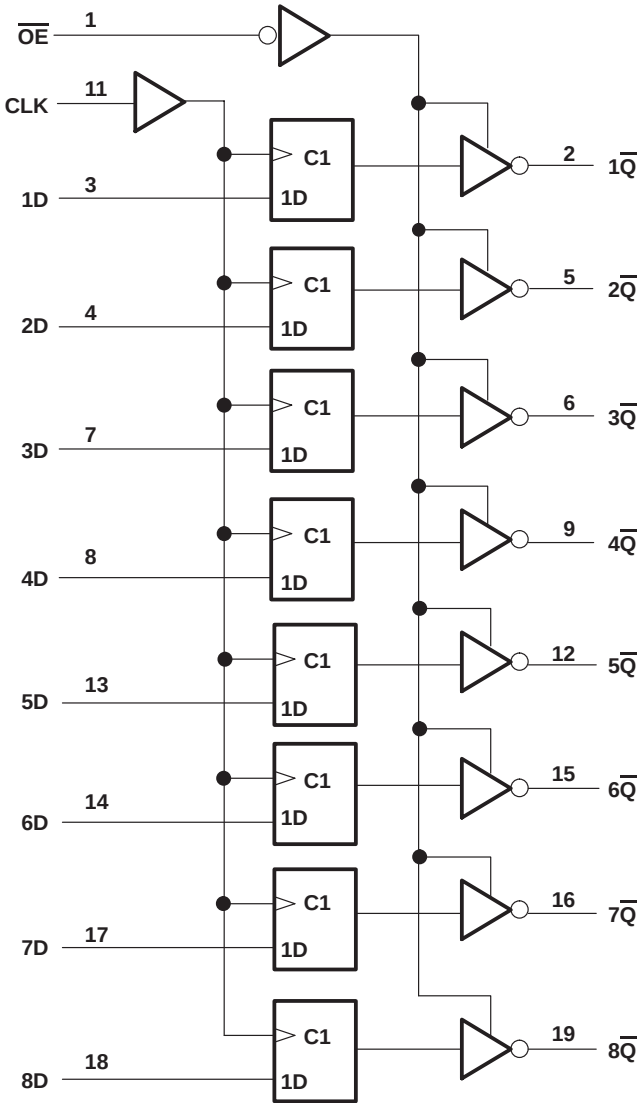
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range (see Note 1) . . . . . −1.2 V to 7 V
Input current . . . . . ±20 mA
Voltage range applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage range applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F534A . . . . . 40 mA
SN74F534A . . . . . 48 mA
Operating free-air temperature range: SN54F534A . . . . . −55°C to 125°C
SN74F534A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

recommended operating conditions

		SN54F534A			SN74F534A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			− 18			− 18	mA
I_{OH}	High-level output current			− 3			− 3	mA
I_{OL}	Low-level output current			20			24	mA
T_A	Operating free-air temperature	− 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F534A			SN74F534A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = − 18 mA			− 1.2			− 1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = − 1 mA	2.5	3.4		2.5	3.4		V
		I_{OH} = − 3 mA	2.4	3.3		2.4	3.3		
	V_{CC} = 4.75 V,	I_{OH} = − 1 mA to − 3 mA				2.7			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.3	0.5				V
		I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	µA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			− 0.6			− 0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	− 60		− 150	− 60		− 150	mA
I_{CCZ}	V_{CC} = 5.5 V,	See Note 2		55	86		55	86	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: I_{CCZ} is measured with $\overline{OE}$ at 4.5 V and all other inputs grounded.

timing requirements

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX§				UNIT
			′F534A		SN54F534A		SN74F534A		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100	0	60	0	70	MHz
t_w	Pulse duration	CLK high	7		7		7		ns
		CLK low	6		6		6		
t_{su}	Setup time before CLK↑	Data high	2		2.5		2		ns
		Data low	2		2.5		2		
t_h	Hold time after CLK↑	Data high	2		2		2		ns
		Data low	2		2.5		2		

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX †				UNIT
			′F534A			SN54F534A		SN74F534A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100			60		70		MHz
t_{PLH}	CLK	Any $\overline{Q}$	3	4.5	7	2.5	10.5	2.5	7.5	ns
t_{PHL}			3	4.5	7	2.5	11	2.5	7.5	
t_{PZH}	$\overline{OE}$	Any $\overline{Q}$	1.2	4.5	7.5	1.2	14	1.2	8.5	ns
t_{PZL}			1.2	5	7.5	1.2	10	1.2	8.5	
t_{PHZ}	$\overline{OE}$	Any $\overline{Q}$	1.2	3.5	6.5	1.2	8	1.2	7.5	ns
t_{PLZ}			1.2	3.5	5.5	1.2	7.5	1.2	6.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.

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