- **Member of the Texas Instruments Widebus+™ Family**
- **Output Edge-Control Circuitry Minimizes Switching Noise in an Unterminated DIMM Load**
- **Supports SSTL_2 Data Inputs**
- **Differential Clock (CLK and $\overline{\text{CLK}}$) Inputs**
- **Supports LVCMOS Switching Levels on the $\overline{\text{RESET}}$ Input**
- **$\overline{\text{RESET}}$ Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

## description

This 26-bit registered buffer is designed for 2.3-V to 2.7-V $V_{CC}$ operation.

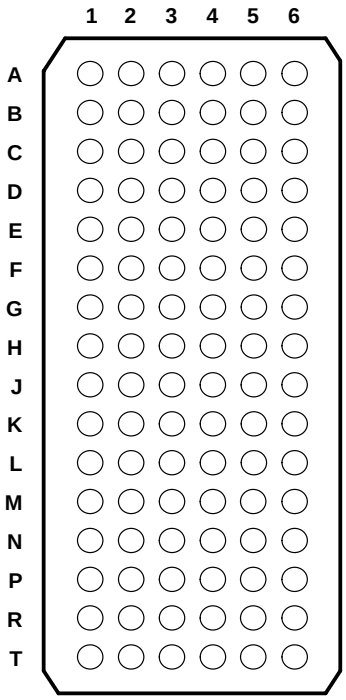
All inputs are SSTL_2, except the LVCMOS reset ($\overline{\text{RESET}}$) input. All outputs are edge-controlled LVCMOS circuits optimized for unterminated DIMM loads.

The SN74SSTV32867 operates from a differential clock (CLK and $\overline{\text{CLK}}$). Data are registered at the crossing of CLK going high and $\overline{\text{CLK}}$ going low.

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage ($V_{REF}$) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are forced low. The LVCMOS $\overline{\text{RESET}}$ always must be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

**GKE PACKAGE**
**(TOP VIEW)**




## terminal assignments

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| A | D1 | $V_{CC}$ | GND | $V_{DDQ}$ | Q1 | Q2 |
| B | D3 | D2 | $V_{REF}$ | GND | Q3 | Q4 |
| C | D5 | D4 | NC | GND | Q5 | Q6 |
| D | D7 | D6 | GND | $V_{DDQ}$ | Q7 | Q8 |
| E | D9 | D8 | $V_{CC}$ | GND | Q9 | $V_{DDQ}$ |
| F | D11 | D10 | GND | $V_{DDQ}$ | Q10 | GND |
| G | D13 | D12 | $V_{CC}$ | $V_{DDQ}$ | Q12 | Q11 |
| H | D15 | D14 | GND | GND | GND | Q13 |
| J | CLK | NC | GND | GND | GND | Q14 |
| K | $\overline{CLK}$ | $\overline{RESET}$ | $V_{CC}$ | $V_{DDQ}$ | Q15 | Q16 |
| L | D16 | D17 | GND | $V_{DDQ}$ | Q17 | GND |
| M | D18 | D19 | $V_{CC}$ | GND | Q18 | $V_{DDQ}$ |
| N | D20 | D21 | GND | $V_{DDQ}$ | Q20 | Q19 |
| P | D22 | D23 | NC | GND | Q22 | Q21 |
| R | D24 | D25 | NC | GND | Q24 | Q23 |
| T | D26 | $V_{CC}$ | GND | $V_{DDQ}$ | Q26 | Q25 |

## ORDERING INFORMATION

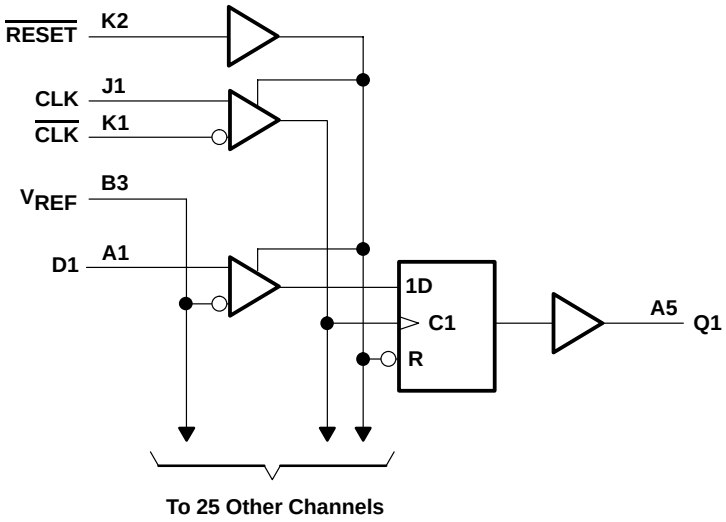
| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| 0°C to 70°C | LFBGA – GKE | Tape and reel | SN74SSTV32867GKER | SV867 |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{RESET}$ | CLK | $\overline{CLK}$ | D | Q |
| H | ↑ | ↓ | H | H |
| H | ↑ | ↓ | L | L |
| H | L or H | L or H | X | $Q_0$ |
| L | X or floating | X or floating | X or floating | L |

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ or $V_{DDQ}$ . . . . . –0.5 V to 3.6 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Notes 1 and 2) . . . . . –0.5 V to $V_{DDQ}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{DDQ}$) . . . . . ±50 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{DDQ}$) . . . . . ±50 mA
Continuous current through each $V_{CC}$, $V_{DDQ}$, or GND . . . . . ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3) . . . . . 40°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 3.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | $V_{DDQ}$ | | 2.7 | V |
| $V_{DDQ}$ | Output supply voltage | | 2.3 | | 2.7 | V |
| $V_{REF}$ | Reference voltage ($V_{REF} = V_{DDQ}/2$) | | 1.15 | 1.25 | 1.35 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF}$–40mV | $V_{REF}$ | $V_{REF}$+40mV | V |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | V |
| $V_{IH}$ | AC high-level input voltage | Data input | $V_{REF}$+310mV | | | V |
| $V_{IL}$ | AC low-level input voltage | Data input | | | $V_{REF}$–310mV | V |
| $V_{IH}$ | DC high-level input voltage | Data input | $V_{REF}$+150mV | | | V |
| $V_{IL}$ | DC low-level input voltage | Data input | | | $V_{REF}$–150mV | V |
| $V_{IH}$ | High-level input voltage | $\overline{\text{RESET}}$ | 1.7 | | | V |
| $V_{IL}$ | Low-level input voltage | $\overline{\text{RESET}}$ | | | 0.7 | V |
| $V_{ICR}$ | Common-mode input voltage range | CLK, $\overline{\text{CLK}}$ | 0.97 | | 1.53 | V |
| $V_{I(PP)}$ | Peak-to-peak input voltage | CLK, $\overline{\text{CLK}}$ | 360 | | | mV |
| $I_{OH}$ | High-level output current | | | | –8 | mA |
| $I_{OL}$ | Low-level output current | | | | 8 | mA |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

NOTE 4: The $\overline{\text{RESET}}$ input of the device must be held at $V_{CC}$ or GND to ensure proper device operation. The differential inputs must not be floating unless $\overline{\text{RESET}}$ is low. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $I_I$ = –18 mA | | 2.3 V | | | –1.2 | V |
| $V_{OH}$ | | $I_{OH}$ = –100 μA | | 2.3 V to 2.7 V | $V_{DDQ}$–0.2 | | | V |
| | | $I_{OH}$ = –8 mA | | 2.3 V | 1.7 | | | |
| $V_{OL}$ | | $I_{OL}$ = 100 μA | | 2.3 V to 2.7 V | | | 0.2 | V |
| | | $I_{OL}$ = 8 mA | | 2.3 V | | | 0.4 | |
| $I_I$ | All inputs | $V_I = V_{CC}$ or GND | | 2.7 V | | | ±5 | μA |
| $I_{CC}$ | Static standby | $\overline{RESET}$ = GND | $I_O$ = 0 | 2.7 V | | | 40 | μA |
| | Static operating | $\overline{RESET} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ | | | | | 95 | mA |
| $I_{CCD}$ | Dynamic operating – clock only | $\overline{RESET} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle | $I_O$ = 0 | 2.5 V | | 44 | | μA/ MHz |
| | Dynamic operating – per each data input | $\overline{RESET} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle | | | | 5 | | μA/ clock MHz/ D input |
| $C_i$‡ | Data inputs | $V_I = V_{REF} \pm 310$ mV | | 2.5 V | 2.5 | 3.5 | 4.5 | pF |
| | CLK, $\overline{CLK}$ | $V_{ICR}$ = 1.25 V, | $V_{I(PP)}$ = 360mV | | 4 | 4.5 | 5 | |
| | $\overline{RESET}$ | $V_I = V_{CC}$ or GND | | | 3.9 | 5 | 5.5 | |

† All typical values are at $V_{CC}$ = 2.5 V, $T_A$ = 25°C.
‡ Measured with 50-MHz input frequency

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| | | | | $V_{CC}$ = 2.5 V ± 0.2 V | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | | | 200 | MHz |
| $t_w$ | Pulse duration | | CLK, $\overline{CLK}$ high or low | 2.5 | | ns |
| $t_{act}$ | Differential inputs active time (see Note 5) | | | | 22 | ns |
| $t_{inact}$ | Differential inputs inactive time (see Note 6) | | | | 22 | ns |
| $t_{su}$ | Setup time | Fast slew rate (see Notes 7 and 9) | Data before CLK↑, $\overline{CLK}$↓ | 0.75 | | ns |
| | | Slow slew rate (see Notes 8 and 9) | | 0.9 | | |
| $t_h$ | Hold time | Fast slew rate (see Notes 7 and 9) | Data after CLK↑, $\overline{CLK}$↓ | 0.75 | | ns |
| | | Slow slew rate (see Notes 8 and 9) | | 0.9 | | |

NOTES: 5. Data inputs must be low a minimum time of $t_{act}$ min, after $\overline{RESET}$ is taken high.
6. Data and clock inputs must be held at valid levels (not floating) a minimum time of $t_{inact}$ min, after $\overline{RESET}$ is taken low.
7. Data signal input slew rate ≥1 V/ns
8. Data signal input slew rate ≥0.5 V/ns and <1 V/ns
9. CLK, $\overline{CLK}$ input slew rates are ≥1 V/ns.

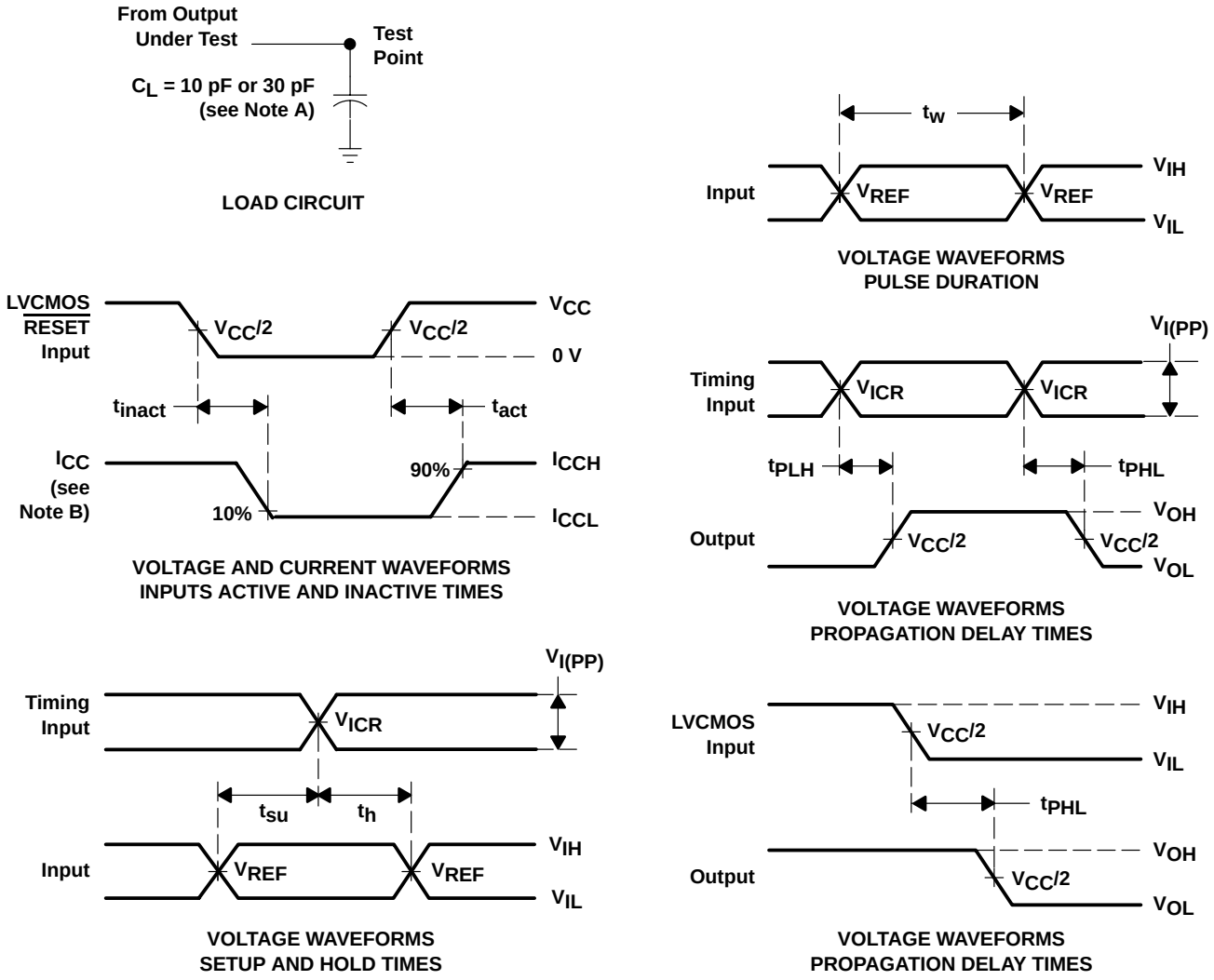
**switching characteristics over recommended operating free-air temperature range, $V_{REF} = V_{DDQ}/2$ and $C_L$ = 10 pF (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 2.5 V ± 0.2 V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $f_{max}$ | | | 200 | | MHz |
| $t_{pd}$ | CLK and $\overline{CLK}$ | Q | 1.1 | 2.8 | ns |
| $t_{PHL}$ | $\overline{RESET}$ | Q | | 5 | ns |

**switching characteristics over recommended operating free-air temperature range, $V_{REF} = V_{DDQ}/2$ and $C_L$ = 30 pF (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 2.5 V ± 0.2 V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $f_{max}$ | | | 200 | | MHz |
| $t_{pd}$ | CLK and $\overline{CLK}$ | Q | 1.1 | 3.8 | ns |
| $t_{PHL}$ | $\overline{RESET}$ | Q | | 5 | ns |

## PARAMETER MEASUREMENT INFORMATION

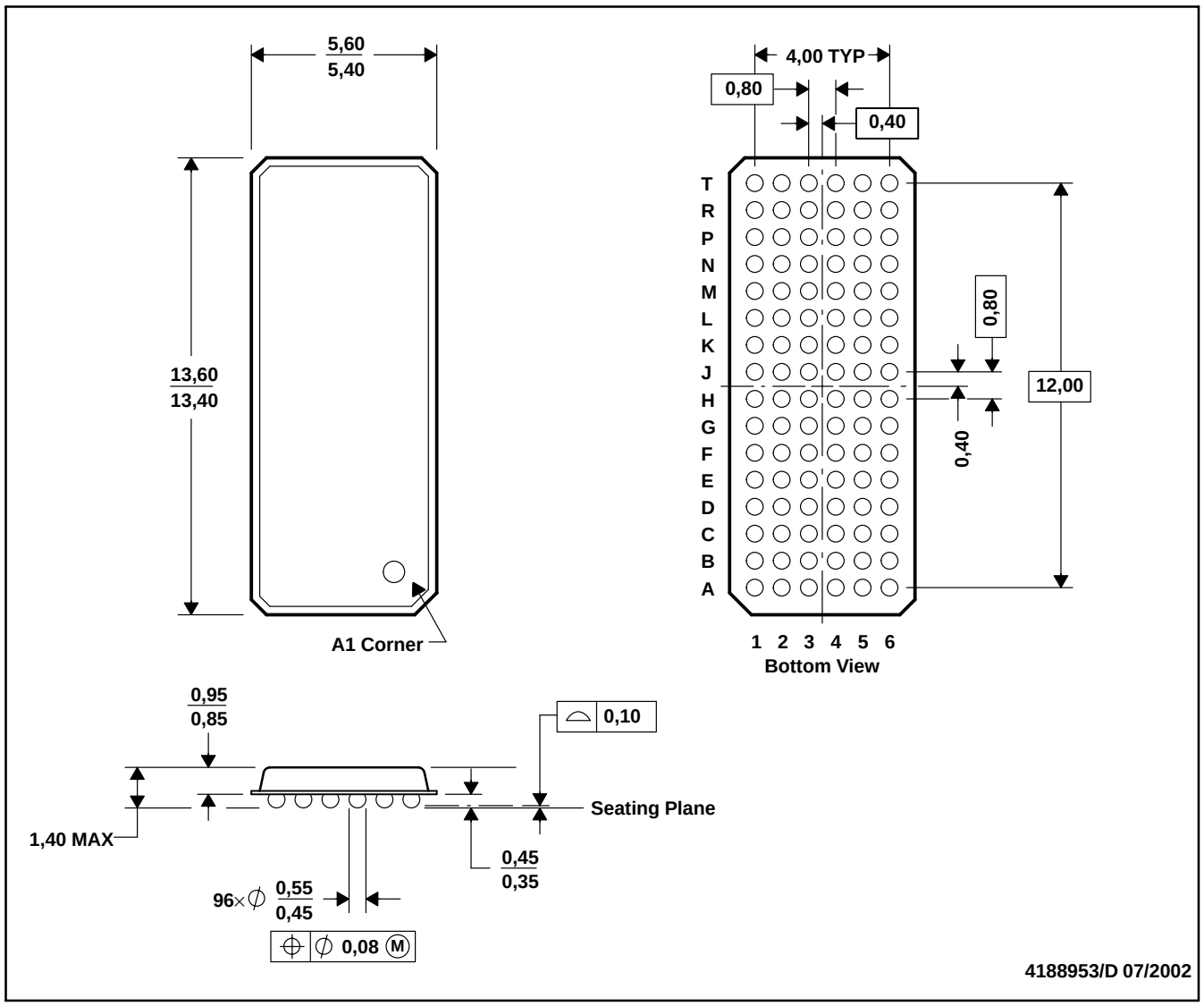



NOTES: A. $C_L$ includes probe and jig capacitance.
B. $I_{CC}$ tested with clock and data inputs held at $V_{CC}$ or GND, and $I_O$ = 0 mA.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise noted).
D. The outputs are measured one at a time with one transition per measurement.
E. $V_{REF} = V_{DDQ}/2$
F. $V_{IH} = V_{REF}$ + 310 mV (ac voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVCMOS input.
G. $V_{IL} = V_{REF}$ – 310 mV (ac voltage levels) for differential inputs. $V_{IL}$ = GND for LVCMOS input.
H. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 1. Load Circuit and Voltage Waveforms**

MPBG095B – MARCH 1999 – REVISED AUGUST 2002

**GKE (R-PBGA-N96)** **PLASTIC BALL GRID ARRAY**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration
D. Falls within JEDEC MO-205 variation CC.
E. This package is tin-lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead-free.

MicroStar BGA is a trademark of Texas Instruments.

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