

Speech Synthesizer

FEATURES

- Double Buffered Input Memory
- Single +5 Volt Supply
- On Chip Oscillator with External Crystal Control
- On Chip Digital to Analog Converter
- 12 Coefficient Registers
- Vocal Tract Model

DESCRIPTION

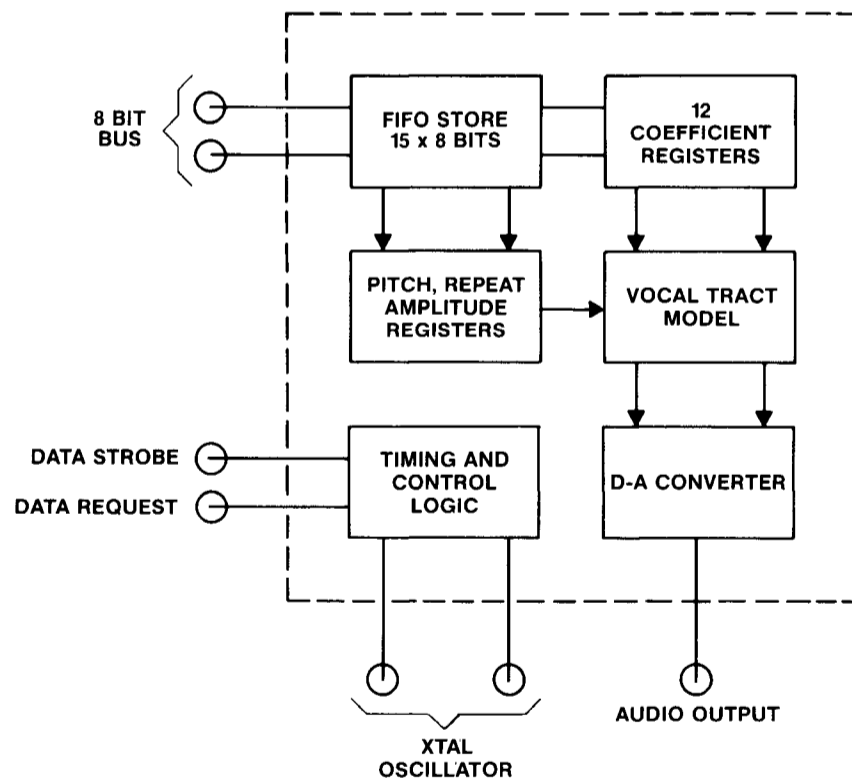
The SP-0250 is a single chip speech synthesizer with a time shared 2 stage filter section which simulates a 12 stage cascade filter. This filter is a model of the human vocal tract. The SP-0250 can be interfaced with the General Instrument microcomputer PIC1650, and requires a single +5 volt supply.

The SP-0250 is fabricated with N-channel Ion Implant technology resulting in a high performance product with proven reliability and production history.

PIN CONFIGURATION 28 LEAD DUAL IN LINE

Top View			
V _{SS} = GND	1	28	D5
D6	2	27	D4
D7	3	26	D3
GND	4	25	D2
DATA PRESENT	5	24	D1
DATA REQUEST	6	23	D0
(DIRECT DATA) TEST	7	22	RESET
(DATA CLK 1.56M) TEST	8	21	TEST (SERIAL DATA)
(CPU CLK) 3.12MHz	9	20	TEST (SYNC)
XTAL OUT	10	19	DIGITAL OUT
NC	11	18	TEST (ROM TEST)
XTAL IN	12	17	NC
(PIC CLK 1.04M) TEST	13	16	GND
(GROM CLK) 445.7kHz	14	15	V _{DD} = +5V NOMINAL

BLOCK DIAGRAM OF SP-0250





SP-0250

PIN FUNCTIONS

Pin Number	Name	Function
15	V _{DD}	Positive Power Supply
1	V _{SS}	Ground
Clock		
12	XTAL IN	The 3.12MHz crystal and associated circuitry are connected here.
10	XTAL OUT	
Inputs		
22	Reset	A logic "0" on this input resets the chip.
23-28, 2, 3	D0-D7 Data Bus	The input 8 bit data bus.
5	Data Present	This input strobes the data on D0-D7 into the chip.
4, 16, 7, 18		Must be grounded for proper chip operation.
Outputs		
6	Data Request	This output requests data be sent to the chip.
19	Digital Out	The output of the chip. This output is open collector and requires a pull-up.
9	3.120MHz CPU Clock	A buffered push-pull output.
14	0.4457MHz GROM Clock	A buffered push-pull output with a 3:4 high to low ratio.

TEST PINS

Pin Number	Name	Function
Test Inputs		
7	Direct Data Mode	A logic "1" on this input causes the data bus to be loaded directly into the source register in the chip.
18	ROM Test	A logic "1" on this input causes the ROM outputs to appear on the "SERIAL DATA" Pin.
Test Outputs		
20	SYNC	A buffered push-pull test output that is a 640ns positive pulse with a duty cycle of 312 clocks.
21	Serial Data	A buffered push-pull test output that monitors a point in the internal data bus.
8	1.56MHz Data Clock	A buffered push-pull output square wave.
13	1.04MHz PIC Clock	A buffered push-pull output with a 1:2 high to low ratio.



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V _{CC}	-0.3V to +12V
Storage Temperature	-25°C to +125°C
Lead Temp (Soldering)	10Sec @ +330°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise stated)

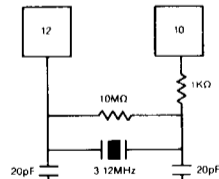
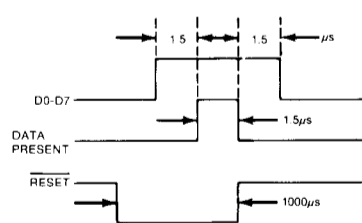
V_{CC} = +4.6V to +5.5V
 Operating Temperature = 0°C to +55°C

DC CHARACTERISTICS

Characteristic	Min	Typ	Max	Units	Conditions
10 Inputs:					
Reset D0-D7, Data Present					
Logic 0	0.0	—	0.6	V	5.5V
Logic 1	2.4	—	V _{CC}	V	
Leakage	—	—	10	μA	
1 Clock Input:					
Logic 0	0.0	—	0.6	V	5.5V
Logic 1	4.0	—	V _{CC}	V	
Leakage	—	—	10	μA	
2 Test Inputs					
Direct Data Mode, ROM Test					
Logic 0	0.0	—	0.6	V	5.5V
Logic 1	2.4	—	V _{CC}	V	
Capacitance	—	—	10	pF	
Leakage	—	—	10	μA	
3 P/P Outputs					
Data Request, CPU CLock, GROM Clock					
Logic 0	0.0	—	0.6	V	.72mA
Logic 1	3.50	—	V _{CC}	V	-50μA
1 O/C Output					
Digital Out					
Logic 0	0.0	—	0.6	V	2.2K
Logic 1	—	—	10	μA	5.0V Source
Power on V _{DD} = I _{CC}	—	50	75	mA@ 25°C	V _{DD} =5.5 V _{SS} =0.0 No Loads

AC CHARACTERISTICS

Characteristic	Min	Typ	Max	Units	Conditions
Clock Frequency	—	3.12	—	MHz	Square Wave
	—	320	—	ns	
Data Present					
Logic 1	1.5	—	—	μS	No Load
Logic 0	10.0	—	—	μS	
Reset D0-D7	1000	—	—	μS	
Set Up	1.5	—	—	μS	
Hold	1.5	—	—	μS	
P/P Test Output					
Serial Data					
Logic 0	0.0	—	0.6	V	No Load
Logic 1	3.50	—	V _{CC}	V	



CHIP WILL OSCILLATE WITH PASSIVE COMPONENTS SHOWN. F = 3.12



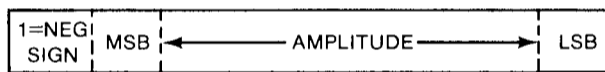
SP-0250

PARAMETER ASSIGNMENT

The 15 parameters are input in the following manner:

Byte	Name	Data Bus Pins						
		3	2	28	27	26	25	24
0	C21	1=POS SIGN	MSB	COEFFICIENT				LSB
1	C11							
2	Amplitude*	← EXP →		← AMPLITUDE →				
3	C22							
4	C12							
5	Pitch	MSB	← PITCH →				LSB	
6	C23							
7	C13							
8	Repeat	0	V(u)	MSB	REPEAT		LSB	
9	C24	1=POS SIGN	MSB					LSB
10	C14							
11	C25							
12	C15							
13	C26							
14	C16							

* Amplitude Direct Data Mode



Exponent From Normal Mode Remains Until Changed

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