PLESSEY
SEMICONDUCTORS

# SP1600 SERIES

ECL III

# SP1650B (HIGH Z)

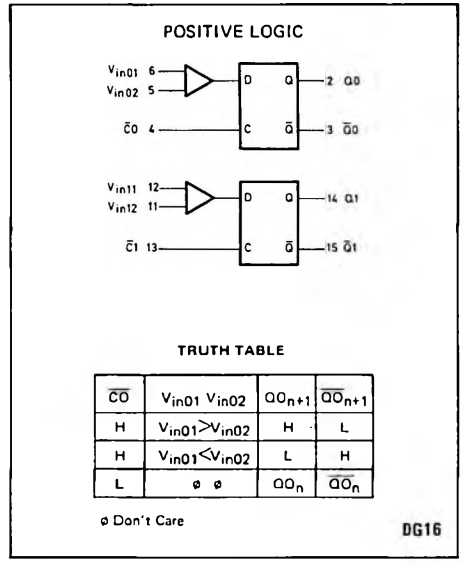
# SP1651B (LOW Z)

## DUAL A/D COMPARATOR

The SP1650 and the SP1651 are very high speed comparators utilizing differential amplifier inputs to sense analog signals above or below a reference level. An output latch provides a unique sample-hold feature. The SP1650 provides high impedance Darlington inputs, while the SP1651 is a lower impedance option, with higher input slew rate and higher speed capability.

Complementary outputs permit maximum utility for applications in high speed test equipment, frequency measurement, sample and hold, peak voltage detection and transmitters, receivers, memory translation and more.

The clock inputs ($\overline{C0}$ and $\overline{C1}$) operate from PECL III or PECL 10,000 digital levels. When $\overline{C0}$ is at a logic high level, Q0 will be at a logic high level provided that $V_{in01} > V_{in02}$ ($V_{in01}$ is more positive than $V_{in02}$). $\overline{Q0}$ is the logic complement of Q0. When the clock input goes to a low logic level, the outputs are latched in their present state.




TRUTH TABLE

| $\overline{C0}$ | $V_{in01}$ $V_{in02}$ | $Q0_{n+1}$ | $\overline{Q0}_{n+1}$ |
|---|---|---|---|
| H | $V_{in01} > V_{in02}$ | H | L |
| H | $V_{in01} < V_{in02}$ | L | H |
| L | ø ø | $Q0_n$ | $\overline{Q0}_n$ |

ø Don't Care

DG16

*Fig. 1 Logic diagram of SP1651*

## FEATURES

- $P_D$ = 275 mW typ/pkg (No Load)
- Very High Speed – 3.5 ns Delay (SP1650)
  – 2.5 ns Delay (SP1651)
- High Input Slew Rate – 350 V/μs (SP1651)
- Positive Transition Region – Input Hysterisis.