PLESSEY
SEMICONDUCTORS

SP 8000 SERIES
HIGH SPEED DIVIDERS

SP8760 B & M
GENERAL PURPOSE SYNTHESISER CIRCUIT

The SP8760 is a multi-function device for use in phase-lock-loop systems. It contains a crystal oscillator maintaining circuit, followed by a divide-by-four stage; a digital phase/frequency comparator; and a two-modulus divider programmable to divide by 15 or 16.

It may be used with a prescaler to phase-lock single frequency transmitters or receivers in the HF, VHF or UHF bands.

The addition of an MOS/CMOS programmable plus fixed divider will generate a complete frequency synthesiser. The maximum frequency requirement of the control device is only 1MHz, enabling complex functions to be performed using LSI technologies. With suitable prescalers, the controlled frequency source may extend into the 1GHz region.

The SP8760 is available in two temperature grades: 0°C to +70°C ('B' grade) and −40°C to +85°C ('M' grade).

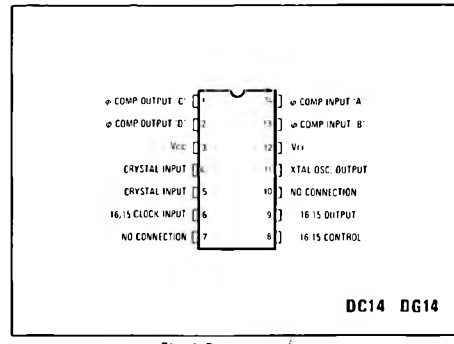

Fig. 1 Pin connections

FEATURES

- TTL/MOS Compatible Inputs and Outputs
- Low Power Consumption (<250mW Typ)
- Minimum External Components
- Voltage Pump Outputs on Phase/ Frequency Comparator
- Zero Phase Difference Pulses <30nSec
- Crystal Oscillator Stability + 5 ppm at 4MHz, 0°C to + 70°C
- Crystal Oscillator Interfaces with SL680 for Very High Stability Applications

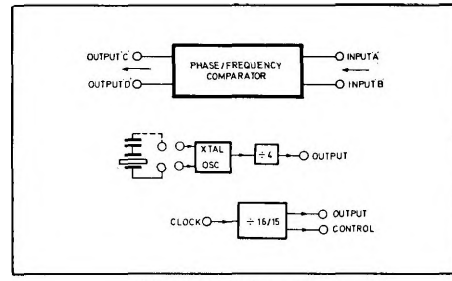

Fig. 2 SP8760 block diagram

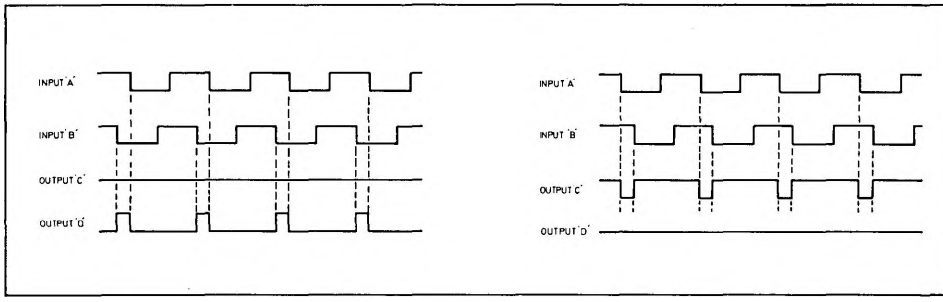

Fig. 3 Phase/frequency comparator waveforms

ELECTRICAL CHARACTERISTICS

Supply voltage 5V ± 0.5V
Supply current 45mA typ

Test conditions (unless otherwise stated):
V_{CC} = 4.5V to 5.5V
V_{EE} = 0V
T_{AMB} 0 C to +70 C ('B' grade)
−40 C to + 85 C ('M' grade)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Power Supply Current		45	65	mA	
Crystal Osc. ÷ 4					
Crystal series capacitor		28		pF	at 4MHz
Crystal series capacitor		20		pF	at 10 MHz
Temperature Stability			0.2	ppm/ C	at 4MHz, excluding crystal temperature coefficient.
Supply voltage stability		−1		ppm/V	at 4 MHz
External oscillator drive required		±1		mA	See Fig. 8.
Divide-by-four output, external current sink capability	5			mA	at 0.5V
Phase/Frequency Comparator					
Input current		250	350	uA	at Vin = 2.4V
Output 'C' current sink capability	6			mA	at 0.5V
Output 'D' current source capability	6				at (V_{CC} - 1.15V)
Zero phase pulse width			30	ns	
Input to Output delay		40		ns	
Divide by 16/15					
Control input current		250	350	µA	at Vin = 2.4V
Clock input current		−1.0	−1.6	mA	at Vin = 0.4V
Output external current sink capability	5			mA	at 0.5V
Maximum clock frequency	16	28		MHz	Divide by 16
	12	18		MHz	Divide by 15
Clock to output delay		35		ns	Output 1 - 0

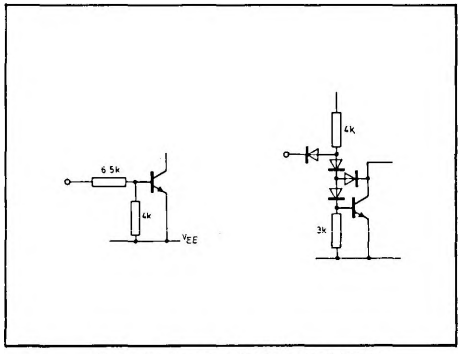

Fig. 4 Phase comp./divider control inputs

ABSOLUTE MAXIMUM RATINGS

Power supply V_{CC} − V_{EE} 0V to +10V
Output current 20mA
Operating junction temperature +150°C
Storage temperature −55°C to +150°C

OPERATING NOTES

The crystal oscillator is an emitter coupled circuit with an internal roll off capacitor to prevent oscillation at overtone frequencies. The crystal is connected in series with a capacitor between pins 4 and 5. It may be used with series resonant crystals at frequencies up to 10MHz. The stability of the crystal oscillator is better than ±5 p.p.m. at 4MHz over the temp range 0 C to 70 C (excluding the temperature coefficient of the crystal). If a higher stability is required the SL680 crystal oscillator maintaining circuit should be used. This may be interfaced to the SP8760 as shown in Fig. 8. The divide by four has a free collector output with an internal 2.5 KΩ resistor to Vcc.

The phase frequency comparator is an infinite pull-in range circuit which gives zero phase shift lock. The circuit triggers on the 1 - 0 edge of each input and gives an output which is proportional to the phase difference between the two edges (see Fig. 3). When the input 'A' edge precedes the input 'B' edge output 'C' will pulse to a low level while output 'D' will remain at a permanent low level. When the input 'B' edge precedes the input 'A' edge, output 'D' will pulse to a high level while output 'C' will remain at a permanent high level. The two outputs may be used to drive a charge pump and filler as shown in Figs. 5 and 6. The output of the filter may be used to drive directly the varactor line of a voltage controlled oscillator. For optimum 'noise' performance the output pulses from the phase detector must tend to zero when 'in lock'. The leakage on the filter output must therefore be kept to a minimum. If the varactor line draws a significant current it should be buffered using an emitter follower arrangement as shown in Fig. 7.

The phase/frequency comparator inputs are of the current source type as shown in Fig. 4. These may be driven by standard TTL or CMOS. Output 'C' is a free collector with an internal 10KΩ resistor to Vcc. Output 'D' is an emitter follower with an internal 10KΩ resistor to VEE.

The two-modulus prescaler may be controlled to divide by 16 or 15 using the control input. With the control input high the circuit will divide by 16. When a counter is used to control the two-modulus it should be clocked on the 1 - 0 edge of the 16/15 output. If the two-modulus is used only as a fixed divide-by-16 the control input - should be tied to Vcc. The prescaler clock input is a current sink input with a standard TTL fan in of one. It may be driven by standard or low power Schottky TTL. The control input is identical to the phase/frequency comparator inputs as shown in Fig. 4. The two modulus output is a free collector with an internal 1.5KΩ resistor to Vcc.

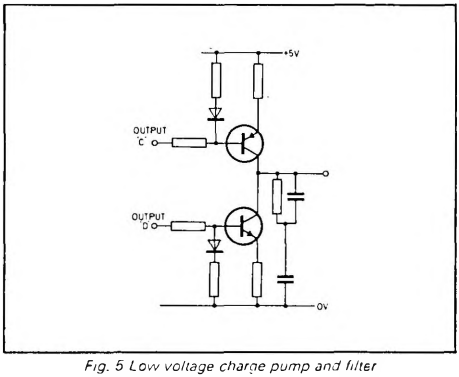

Fig. 5 Low voltage charge pump and filter

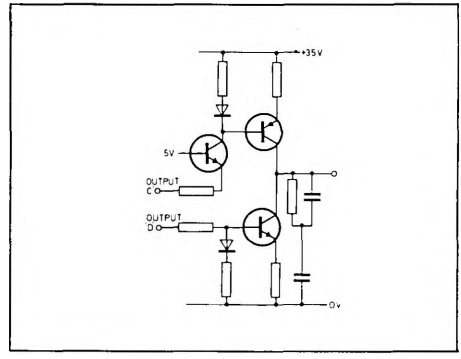

Fig. 6 High voltage charge pump and filter

Divider clock input

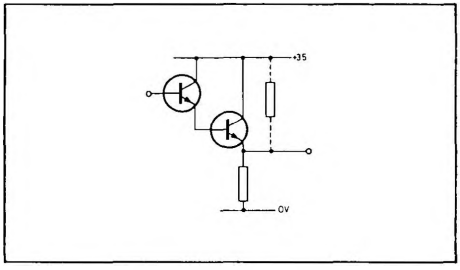

Fig. 7 Emitter follower buffer

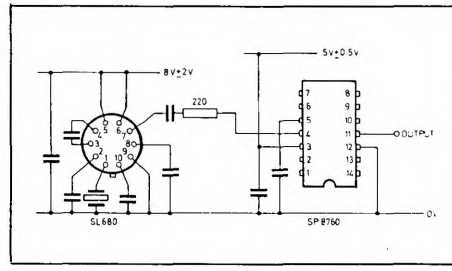

Fig. 8 SL680 to SP8760 interface