

PROGRAMMABLE STANDARD PULSE GENERATOR

SPG 8600 SERIES

SPG series is high precision time-base frequency generators each comprised of a small quartz-crystal element and a CMOS monolithic chip integrated into hybrid configuration. Manufactured with SEIKO EPSON CORP'S qualified quartz technology, the devices feature low current consumption high quality and low cost, providing a broad range of applications as OEM devices.

SPECIFICATIONS

SPG STANDARD TYPE

Model	Base frequency	Frequency characteristics				Current consumption
		Frequency tolerance	Freq. temp. coefficient	Voltage coefficient	Aging	
8640AN	600KHz	± 100ppm	+10/-120ppm	± 20ppm	± 5ppm/Y	MAX.1mA
8640BN	1MHz			± 10ppm		MAX.2mA
8650A	60KHz	± 50ppm	+10/-120ppm	± 10ppm	± 5ppm/Y	MAX.0.5mA
8650B	100KHz					
8650E	32.768KHz	± 5ppm	+10/-120ppm	± 5ppm	± 3ppm/Y	MAX.0.5mA
8651A	60KHz					
8651B	100KHz					
8651E	32.768KHz					

SPG BAUDRATE GENERATOR

Model	Base frequency	Frequency characteristics				Current consumption
		Frequency tolerance	Freq. temp. Coefficient	Voltage Coefficient	Aging	
8640C	768kHz	± 100ppm	+10/-120ppm	± 10ppm	± 5ppm/Y	MAX.1.5mA
8650C	96kHz					MAX.0.5mA
8650D	153.6kHz	± 50ppm				

ELECTRICAL CHARACTERISTICS $V_{DD}=5V \pm 0.5V, T_a = -10 \sim +70^\circ C, C_L = 15pF$

Item	Symbol	MIN.	TYP.	MAX.	Unit	Remarks
L.Input voltage	V_{IL}	0		0.8	V	
H.Input voltage	V_{IH}	$V_{DD}-1.0$		V_{DD}	V	
L.Input current : RESET	I_{IL}	-5		-30	μA	RESET = V_{SS}
H.Input current : RESET	I_{IH}			0.5	μA	RESET = V_{DD}
L.Input current (OTL1-6, TEST (CSEL, EXO))	I_{IL}	-0.5			μA	(8640N)
H.Input current (OTL1-6, TEST (CSEL, EXO))	I_{IH}	5		30	μA	(8640N)
L.Output voltage	V_{OL}			0.4	V	$I_{OL} = 1.6mA$
H.Output voltage	V_{OH}	$V_{DD}-1.0$			V	$I_{OH} = -40 \mu A$
L.Output current	I_{OL}	1.6			mA	$V_{OL} = 0.4V$
H.Output current	I_{OH}			-40	μA	$V_{OH} = V_{DD} - 1.0V$
Rise time	t_{rLH}		30	60	nsec	
Fall time	t_{rHL}		25	50	nsec	
Symmetry		40		60	%	Except 1/3, 1/6, divided frequency
RESET pulse range	t_{RW}	1.0			μsec	
RESET delay time	t_R			1.0	μsec	
Timing error after RESET released	t_E	$t_w - 1/2 t_w^{*1}$		t_w^{*2}	μsec	
External clock input frequency	F_{IN}			1M	Hz	8640N
External clock input pulse range	t_{IN}	0.5			μsec	8640N
Start-up time			0.2	1	sec	

*1 to : One period of base frequency *2 t_w : 1/2 period of programmed output frequency

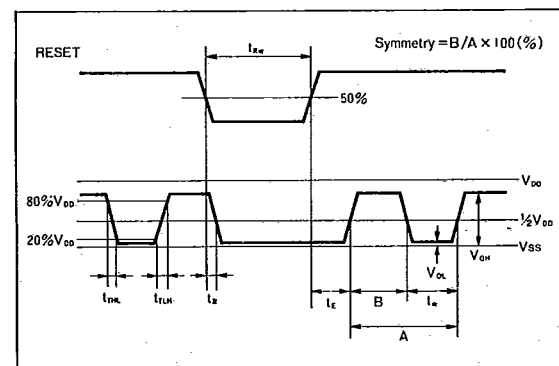
ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rated Value	Unit
Supply voltage	V_{DD}	-0.3 - +7.0	V
Storage temperature	Tstg	-55 - +125	$^\circ C$
Solder heat resistance	T_{sol}	MAX.260	$^\circ C$
		MAX.10	sec

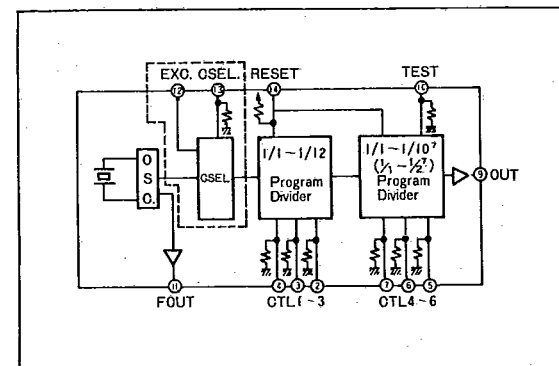
OPERATING RANGE

Item	Symbol	Range	Unit
Supply voltage	V_{DD}	4.5 - 5.5	V
Operating temperature	T_{OPR}	-10 - +70	$^\circ C$

TIMING CHART

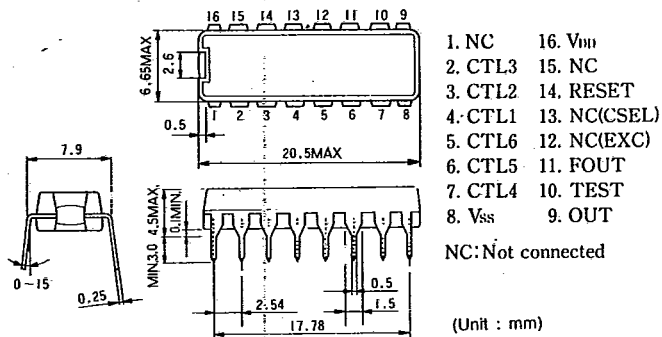


FUNCTION BLOCK DIAGRAM



□ 8640N series only
○ 8650D only

DIMENSIONS AND TERMINAL CONNECTIONS



PIN FUNCTIONS

- (a) CTL1~6
 CTL1~6 control the divide ratio of the base frequency. CTL has a pull-down resistor.
- (b) OUT
 Supplies programmed output frequency.
- (c) FOUT
 Supplies base frequency of internal quartz crystal.
- (d) RESET
 Setting this terminal L resets all counters and sets output to L. Reset has a pull-up resistor.
- (e) TEST
 Setting this terminal H multiplies programmed output frequency by 1000, except when the programmed divide ratio is less than 1/1000. Test has a pull-down resistor.
- (f) EXC (8640N)
 External clock input
- (g) CSEL (8640N)
 Clock select. Setting this terminal H causes the divider to count the frequency of an external clock instead of the internal clock. CSEL has a pull-down resistor.

SET OF OUTPUT FREQUENCY

CTL1	CTL2	CTL3	dividing ratio
0	0	0	1/1
0	0	1	1/10
0	1	0	1/2
0	1	1	1/3
1	0	0	1/4
1	0	1	1/5
1	1	0	1/6
1	1	1	1/12

CTL4	CTL5	CTL6	dividing ratio
0	0	0	1/2 (1/2)
0	0	1	1/6 (1/2)
0	1	0	1/8 (1/2 ²)
0	1	1	1/6 (1/2 ²)
1	0	0	1/8 (1/2 ³)
1	0	1	1/6 (1/2 ³)
1	1	0	1/8 (1/2 ³)
1	1	1	1/6 (1/2 ³)

OUTPUT FREQUENCIES

8640A

UNIT: Hz

SETTING		CTL4	CTL5	CTL6	CTL3	0	1	1	1	1
0	0	0	0	0	0	0	1	1	1	1
0	0	1	0	0	0	1	0	0	1	1
0	1	0	0	0	0	1	0	1	0	1
0	1	1	0	0	0	1	0	1	0	1
1	0	0	0	0	0	600K	60K	6 K	600	60
1	0	1	0	0	0	60K	6K	600	60	6
1	1	0	0	0	0	300K	30K	3 K	300	30
1	1	1	0	0	0	200K	20K	2 K	200	20
1	0	0	1	0	0	150K	15K	1.5K	150	15
1	0	1	1	0	0	120K	12K	1.2K	120	12
1	1	0	1	0	0	100K	10K	1 K	100	10
1	1	1	1	0	0	50K	5K	500	50	5

8640B

SETTING		CTL4	CTL5	CTL6	CTL3	0	1	1	1	1
0	0	0	0	0	0	1M	100 K	10 K	1K	100
0	0	1	0	0	0	100 K	10 K	1 K	100	10
0	1	0	0	0	0	500 K	50 K	5 K	500	50
0	1	1	0	0	0	333.3K	33.3K	3.3K	333.3	33.3
1	0	0	0	0	0	250 K	25 K	2.5K	250	25
1	0	1	0	0	0	200K	20 K	2 K	200	20
1	1	0	0	0	0	166.6K	16.6K	1.6K	166.6	16.6
1	1	1	0	0	0	83.3K	8.3K	833.3	83.3	8.3

8650A 8651A

SETTING		CTL4	CTL5	CTL6	CTL3	0	1	1	1	1
0	0	0	0	0	0	60K	6K	600	60	6
0	0	1	0	0	0	6K	600	60	6	0.6
0	1	0	0	0	0	30K	3K	300	30	3
0	1	1	0	0	0	20K	2K	200	20	2
1	0	0	0	0	0	15K	1.5K	150	15	1.5
1	0	1	0	0	0	12K	1.2K	120	12	1.2
1	1	0	0	0	0	10K	1K	100	10	1
1	1	1	0	0	0	5K	500	50	5	0.5

8650B 8651B

SETTING		CTL4	CTL5	CTL6	CTL3	0	1	1	1	1
0	0	0	0	0	0	100K	10 K	1K	100	10
0	0	1	0	0	0	10K	1 K	100	10	1
0	1	0	0	0	0	50K	5 K	500	50	5
0	1	1	0	0	0	33.3K	3.3K	333.3	33.3	3.33
1	0	0	0	0	0	25K	2.5K	250	25	2.5
1	0	1	0	0	0	20K	2 K	200	20	2
1	1	0	0	0	0	16.6K	1.6K	166.6	16.6	1.6
1	1	1	0	0	0	8.3K	833.3	83.3	8.3	0.83

8650E 8651E

SETTING		CTL4	CTL5	CTL6	CTL3	0	1	1	1	1
0	0	0	0	0	0	32768	3276.8	327.68	32.768	3.276
0	0	1	0	0	0	3276.8	327.68	32.768	3.276	0.3276
0	1	0	0	0	0	16384	1638.4	163.84	16.384	1.638
0	1	1	0	0	0	10922.6	1092.26	109.226	10.922	1.092
1	0	0	0	0	0	8192	819.2	81.92	8.192	0.819
1	0	1	0	0	0	6553.6	655.36	65.536	6.553	0.655
1	1	0	0	0	0	5461.3	546.13	54.613	5.461	0.546
1	1	1	0	0	0	2730.6	273.06	27.306	2.730	0.273

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BAUDRATE GENERATOR

8640 CN

CTL1	CTL2	CTL3	CTL4	CTL5	CTL6	OUTPUT (f)	(f/16) Baudrate output
0	0	0	0	0	0	768 kHz	48000bits/sec
1	0	1	0	0	0	153.6	9600
0	0	1	0	0	0	76.8	4800
0	1	0	0	0	1	38.4	2400
1	0	0	0	0	1	19.2	1200

8650 C

CTL1	CTL2	CTL3	CTL4	CTL5	CTL6	OUTPUT (f)	(f/16) Baudrate output
0	0	0	0	0	0	96.0kHz	6000bits/sec
1	0	1	0	0	0	19.2	1200
0	0	1	0	0	0	9.6	600
0	1	0	0	0	1	4.8	300
0	1	1	0	0	1	3.2	200
1	0	0	0	0	1	2.4	150
1	1	0	0	0	1	1.6	100
1	1	1	0	0	1	0.8	50

8650 D

CTL1	CTL2	CTL3	CTL4	CTL5	CTL6	OUTPUT (f)	(f/16) Baudrate output
0	0	0	0	0	0	153.6kHz	9600bits/sec
0	0	0	0	0	1	76.8	4800
0	0	0	0	1	0	38.4	2400
0	0	0	0	1	1	19.2	1200
0	0	0	1	0	0	9.6	600
0	0	0	1	0	1	4.8	300
0	1	1	1	0	0	3.2	200
0	0	0	1	1	0	2.4	150
1	1	0	1	0	0	1.6	100
0	0	0	1	1	1	1.2	75
1	1	1	1	0	0	0.8	50

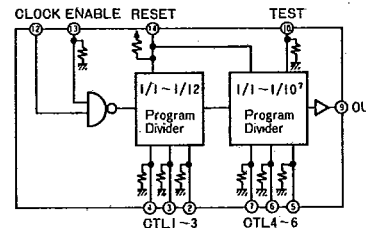
8650 O

SPG DIVIDING IC

Model	Clock input	Current consumption
86500	MAX.1MHz	Approx.2mA

※Other specifications are same as the SPG standard type.

FUNCTION BLOCK DIAGRAM **PIN CONNECTIONS**



- 1. NC
- 2. CTL 3
- 3. CTL 2
- 4. CTL 1
- 5. CTL 6
- 6. CTL 5
- 7. CTL 4
- 8. Vss
- 9. OUT
- 10. TEST
- 11. NC
- 12. CLOCK
- 13. ENABLE
- 14. RESET
- 15. NC
- 16. VDD

NC:Not connected

PIN FUNCTIONS

- (a) CLOCK
CLOCK input (1MHz MAX.)
- (b) ENABLE
Setting this terminal H starts clock count down.
ENABLE has a pull-down resistor.

Note:

- This device is made with C-MOS circuitry. Please take precautions to prevent damage due to static discharge.
- We recommend placing a 0.1μF capacitor between VDD and VSS to protect against power line ripple. And start-up time of input voltage is greater than 1 msec.
- Standard ultrasonic cleaning can be used on the SPG, but please exercise caution in choosing a cleaning solution as the SPG could be damaged.
- Allow a few hundred milli-seconds for the crystal to stabilize after power on because this is a flexure mode crystal.

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● All specifications of this device are subject to change without notice

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