

FEATURES

- Pin-to-Pin Compatible with National DS26C31C
- Low Power CMOS Design
- Three-State Outputs with Enable Pin
- Meets the EIA RS-422 Requirements
- Low Propagation Delays
- High Speed

GENERAL DESCRIPTION

The ST26C31 is a CMOS quad differential line driver designed to meet the standard RS-422 requirements and digital data transmission over balanced lines. To improve noise margin and output stability for slow changing input signals, special hysteresis is built in the ST26C31 circuit.

The ST26C31 is a high speed CMOS line driver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 digital data transmission applications. ST26C31 is suitable for low power 5V operation with high input voltage protection devices.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
ST26C31CP16	16 Lead 300 Mil PDIP	0°C to +70°C
ST26C31CF16	16 Lead 150 Mil JEDEC SOIC	0°C to +70°C
ST26C31IP16	16 Lead 300 Mil PDIP	-40°C to +85°C
ST26C31IF16	16 Lead 150 Mil JEDEC SOIC	-40°C to +85°C

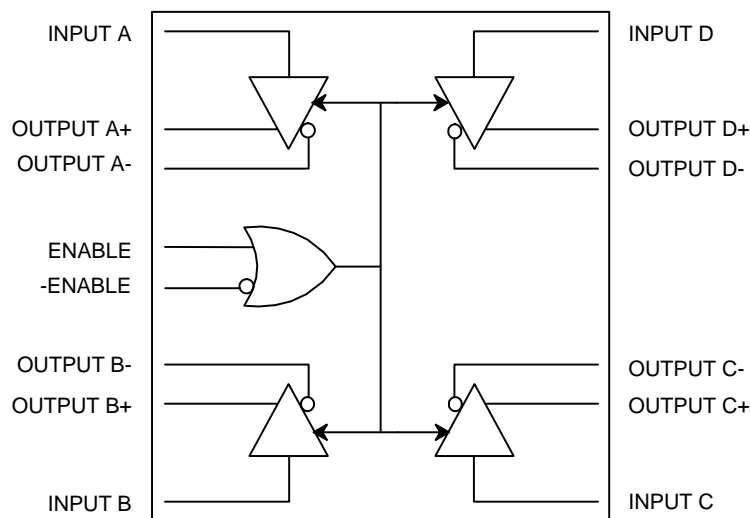
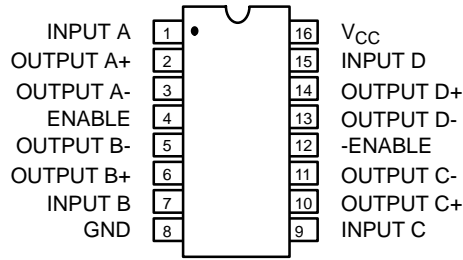
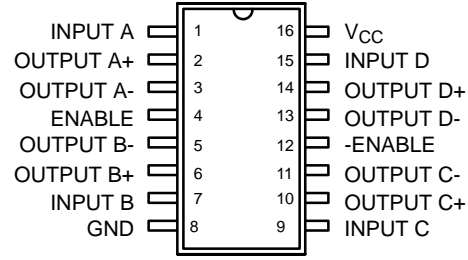


Figure 1. Block Diagram

PIN CONFIGURATION



16 Lead PDIP (0.300")



16 Lead SOIC (Jedec, 0.150")

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	INPUT A	I	Driver A input pin.
2	OUTPUT A+	O	Driver A differential non-inverting output pin.
3	OUTPUT A-	O	Driver A differential inverting output pin.
4	ENABLE	I	Gate control (active high). This pin is one of the two control pins which enables or disables all four drivers. All four drivers are gated with two input or gate.
5	OUTPUT B-	O	Driver B differential inverting output pin.
6	OUTPUT B+	O	Driver B differential non-inverting output pin.
7	INPUT B	I	Driver B input pin.
8	GND	O	Signal and power ground.
9	INPUT C	I	Driver C input pin.
10	OUTPUT C+	O	Driver C differential non-inverting output pin.
11	OUTPUT C-	O	Driver C differential inverting output pin.
12	-ENABLE	I	Gate control (active low). See ENABLE pin description.
13	OUTPUT D-	O	Driver D differential inverting output pin.
14	OUTPUT D+	O	Driver D differential non-inverting output pin.
15	INPUT D	I	Driver D input pin.
16	V _{CC}	I	Power supply pin.

AC ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = -40^{\circ}\text{C} - +85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T_1	Propagation Delay, Input to Output		8	10	ns	S1 open
T_2	Differential Output Rise and Fall Time		8	10	ns	S1 open
T_3	Output Enable Time		18	20	ns	S1 close
T_4	Output Disable Time		18	20	ns	S1 close
T_5^1	Skew			2	ns	S1 open

Note

¹ Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

DC ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = -40^{\circ}\text{C} - +85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_{IN}	Input Current			+1.0	μA	
I_{CC}	Operating Current		600		μA	
I_{OZ}	Three-State Output Leakage		+2.0		μA	
V_{IH}	Input High Level	2.0			V	
V_{IL}	Input Low Level			0.8	V	
V_{OH}	Output High Level	2.5			V	
V_{OL}	Output Low Level			0.5	V	
V_{OS}	Differential Output Level	2.0			V	$R_L=100\Omega$
V_{OC}	Common Mode Output Voltage			3.0	V	$R_L=100\Omega$
V_{OD}	Difference in Common Mode Output			0.4		$R_L=100\Omega$
C_{IN}	Input Capacitance	7	10	15	pF	
C_{PD}	Power Dissipation Capacitance		100		pF	
I_{OS}	Output Short Current	-200		-30	mA	$V_{IN}=V_{CC}$ or GND
I_{OFF}	Output Leakage Current Power Off			100	μA	$V_{OUT}=6\text{V}$
				-100	μA	$V_{OUT}=0.25\text{V}$
I_{DC}	Output Current			± 150	mA	

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Supply Range 7V
 Voltage at Any Pin GND-0.3V to $V_{CC} + 0.3V$
 Operating Temperature $-40^{\circ}C$ to $+85^{\circ}C$

Storage Temperature $-60^{\circ}C$ to $+160^{\circ}C$
 Package Dissipation 500mW

Enable	-Enable	Input	Differential Non-Inverting Output	Differential Inverting Output
L	H	X	Z	Z
L	L	L	L	H
L	L	H	H	L
H	L	L	L	H
H	L	H	H	L
H	H	L	L	H
H	H	H	H	L

Notes

X = Don't care
 Z = Three-State (high impedance)

Table 1. Functional Table

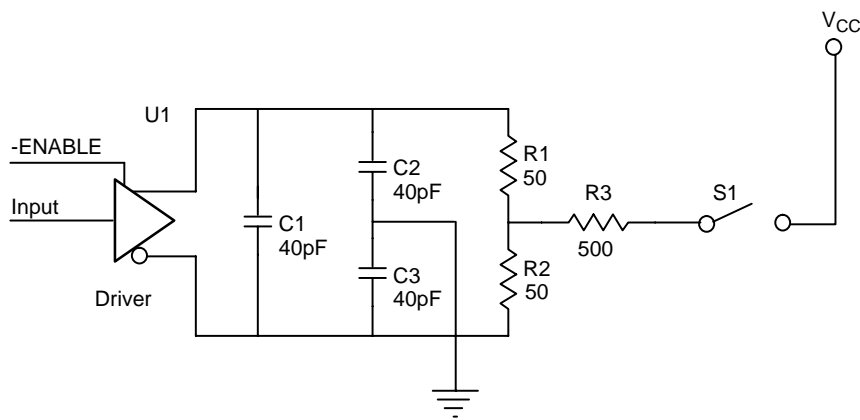


Figure 2. Test Condition

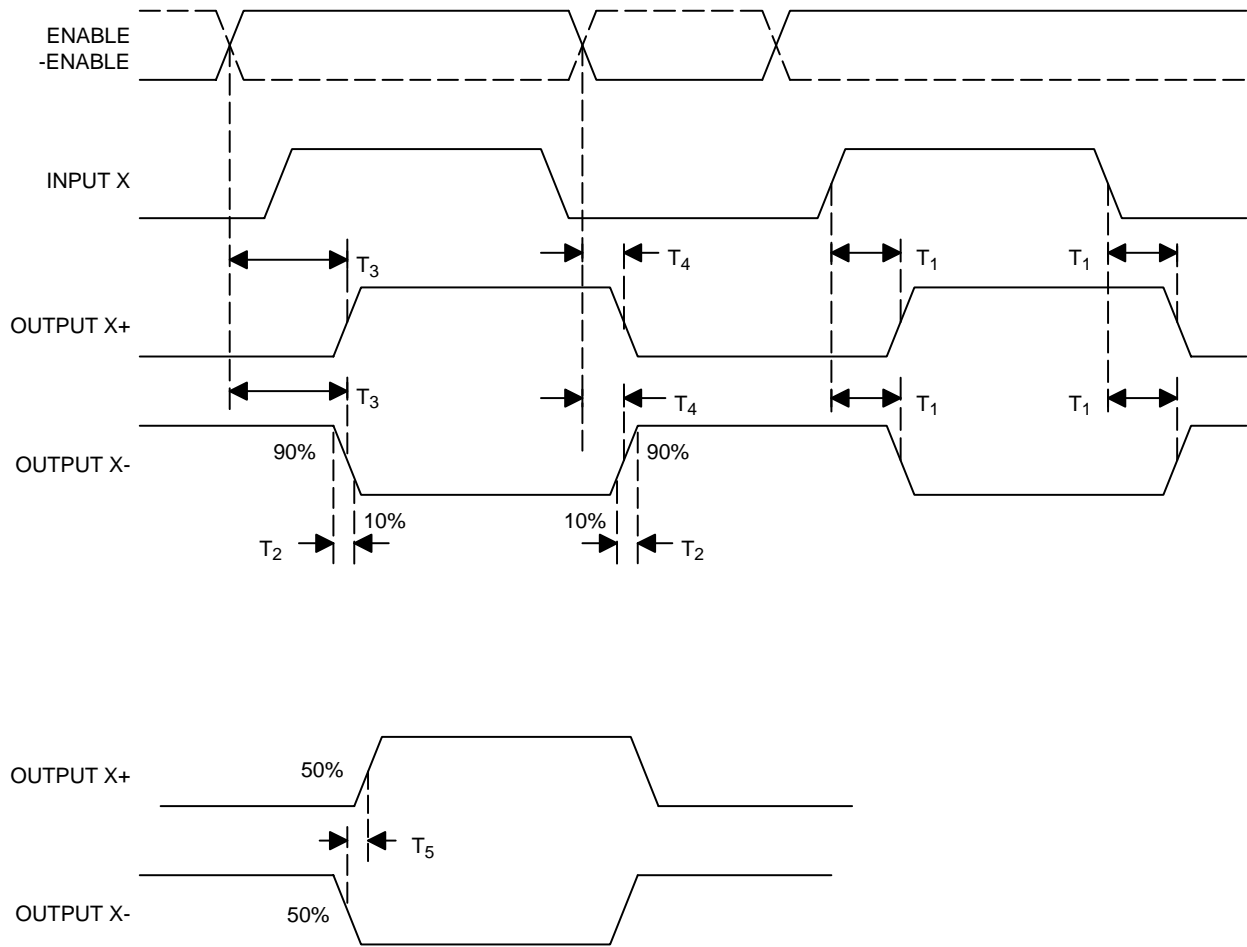
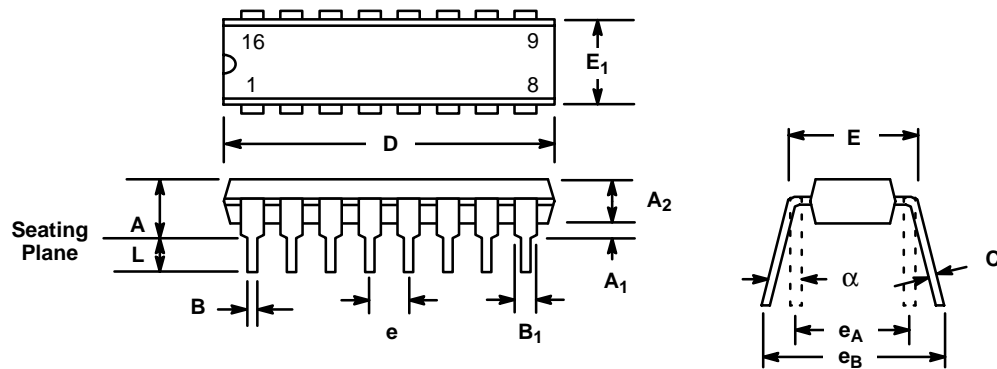


Figure 3. Differential Line Driver Timing

16 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00

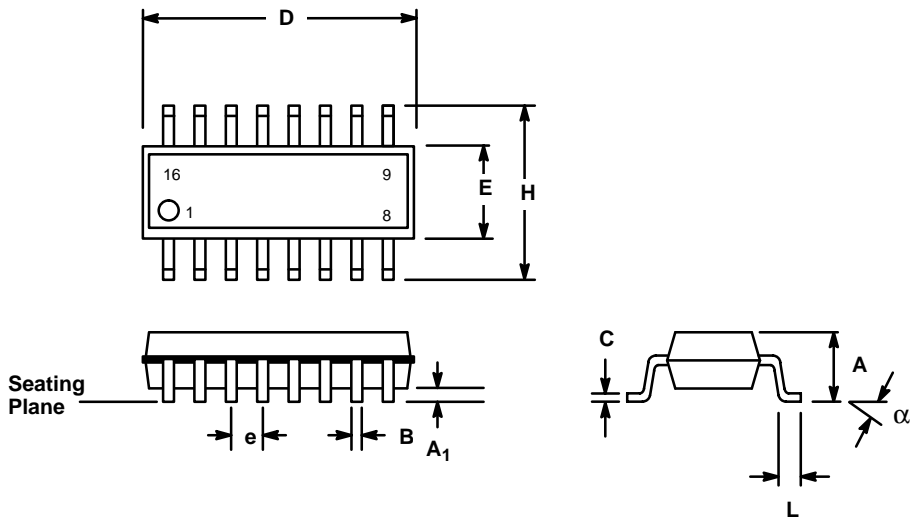


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A ₁	0.015	0.070	0.38	1.78
A ₂	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B ₁	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.745	0.840	18.92	21.34
E	0.300	0.325	7.62	8.26
E ₁	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e _A	0.300 BSC		7.62 BSC	
e _B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

**16 LEAD SMALL OUTLINE
(150 MIL JEDEC SOIC)**

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A ₁	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.386	0.394	9.80	10.00
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

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