Ordering number: EN 4589A

xThick Film Hybrid IC

STK301-090

7-Band, 2-Channel Electronic Graphic Equalizer

Overview

The STK301-090 is an electronic graphic equalizer hybrid IC that incorporates electronic volume control for 7-band, 2-channel equalization for one-touch up/down control of all band gains. Further, low-profile packaging is realized using Sanyo's insulated metal substrate technology (IMST) for the base, SC system and photoresist technologies and folded board construction.

Applications

- Car stereos
- Radio cassette recorders
- Home stereos

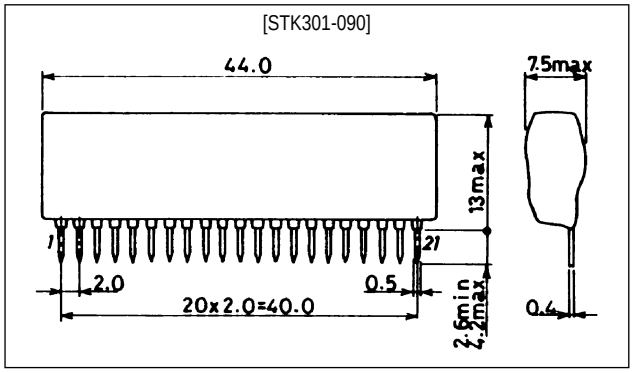
Features

- Gain adjustable in ±2dB steps in all bands
- 13-position control with +12dB maximum boost and –12dB maximum cut in all bands
- Band center frequencies (f_O): 60Hz, 150Hz, 400Hz, 1kHz, 2.5kHz, 6kHz, 15kHz
- A graphic equalization system can be constructed using 3 ICs—the STK301-090, a controller (general-purpose microcontroller) and a display LSI (LC75821 for LCDs; LC7565 for FLT/LEDs)—with the following features.
  - One-touch up/down gain control in all bands
  - One-touch memory recall of preset band settings for tailored frequency response for individual musical tastes.
  - One-touch gain reset to 0dB (flat response function) and gain boost/cut reverse around 0dB center (reverse response function) under supported software control
  - 2 control lines which can also be used to interface with the display LSI for easy connection between the display LSI and the microcontroller
- Low boost and cut operating shock noise

Package Dimensions

unit: mm

4143



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Specifications

Maximum Ratings at Ta = 25°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD} - V_{EE}$ max		16	V
	$V_{CC}1$ max		20	V
	$V_{CC}2$ max		7	V
Input voltage	V_I1	CLK, DI, IN1, IN2	0 to $V_{CC}2$ + 0.3	V
	V_I2	CLK, DI, IN1, IN2	V_{EE} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max		1080	mW
Operating temperature	Topr		–20 to +70	°C
Storage temperature	Tstg		–40 to +100	°C

Recommended Operating Voltages at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{DD} - V_{EE}$, $V_{CC}1$	$V_{EE} = V_{SS}$ = 0V	14	V
	$V_{CC}2$	$V_{EE} = V_{SS}$ = 0V	5	V

Allowable Operating Ranges at Ta = 25°C, V_{SS} = 0V

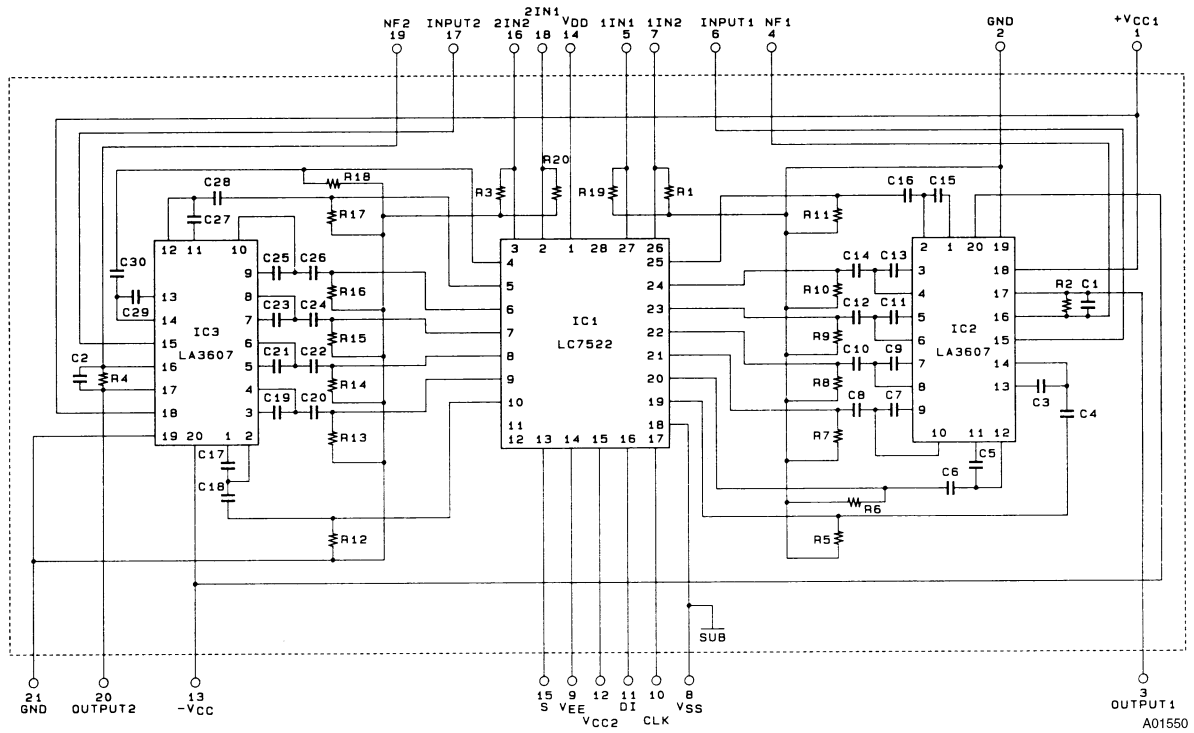
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{DD} - V_{EE}$, $V_{CC}1$		7.5 to 15.0	V
	$V_{CC}2$		4.5 to 5.5	V
Input high level voltage	V_{IH}	CLK, DI	0.8$V_{CC}2$ to $V_{CC}2$	V
Input low level voltage	V_{IL}	CLK, DI	0 to 0.2$V_{CC}2$	V
Input pulse width	$t_{\phi W}$	CLK	≥ 1	μs
Setup time	t_{setup}	DI	≥ 1	μs
Hold time	t_{hold}	DI	≥ 1	μs
Operating frequency	f_{opg}	CLK	≤ 330	kHz

Operating Characteristics at Ta = 25°C, $V_{SS} = V_{EE}$ = 0V, $V_{DD} = V_{CC}1$ = 14V, $V_{CC}2$ = 5V, f = 1kHz, flat frequency response, regulated voltage supply, specified test circuit

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current consumption 1	I_{DD}	$V_{SS} = V_{EE}$ = 0V, $V_{DD} = V_{CC}1$ = 14V, $V_{CC}2$ = 5V	–	–	1	mA
	$I_{CC}1$		–	23	32	mA
	$I_{CC}2$		–	–	1	mA
Current consumption 2	I_{DD}	$V_{CC}1$ = ±7V, V_{DD}/V_{EE} = ±7V	–	–	1	mA
	$I_{CC}1$	$V_{CC}1$ = ±7V, V_{DD}/V_{EE} = ±7V	–	23	32	mA
Voltage gain	VG	V_{IN} = –10dBm	–4.8	–1.8	+1.2	dB
Total harmonic distortion	THD	f = 1kHz, V_O = 1V, 30kHz LPF	–	0.02	0.1	%
Crosstalk	C.T.	f = 20kHz, V_{IN} = 0dBm	45	55	–	dB
Output noise voltage	V_{NO}	Rg = 0Ω, 10Hz to 30kHz BPF	–	7	40	μV
Setting error	ΔB		–1	–	+1	dB

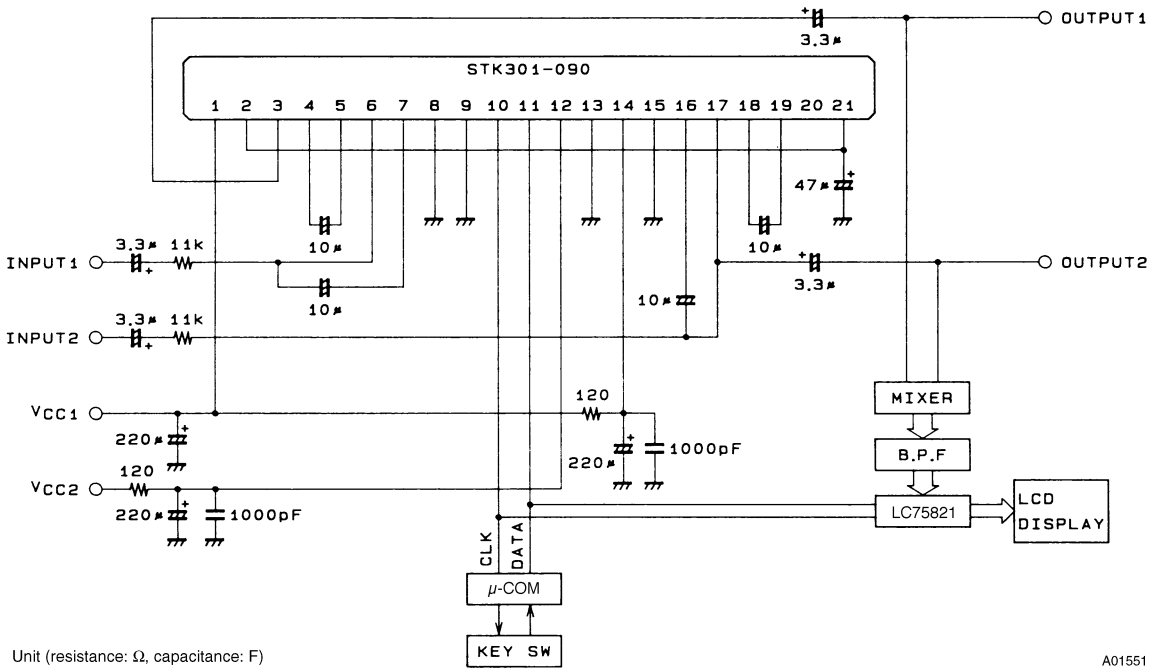
Parameter	Symbol	Conditions		Ratings			Unit
				min	typ	max	
Frequency response	f(1)	f = 60Hz	f = 1kHz, flat frequency response, V_O = –10dB set at 0dB	±10	±12	±14	dB
	f(2)	f = 150Hz		±10	±12	±14	dB
	f(3)	f = 400Hz		±10	±12	±14	dB
	f(4)	f = 1kHz		±10	±12	±14	dB
	f(5)	f = 2.5kHz		±10	±12	±14	dB
	f(6)	f = 6kHz		±10	±12	±14	dB
	f(7)	f = 15kHz		±10	±12	±14	dB

Equivalent Circuit



Sample Application Circuits

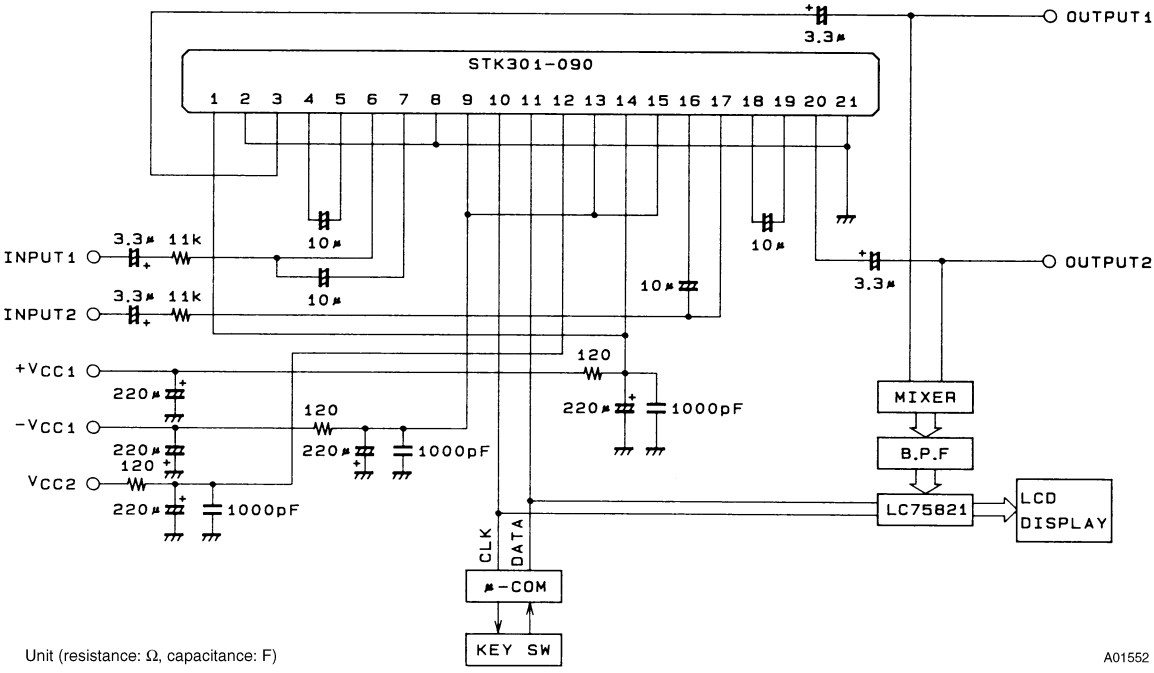
Single Supply



Unit (resistance: Ω, capacitance: F)

A01551

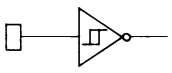
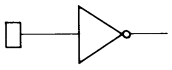
Split Supply



Unit (resistance: Ω, capacitance: F)

A01552

Pin Functions

Number	Name	Function	
1	$+V_{CC}1$	Graphic equalizer IC2 and IC3 positive supply pin	
2, 21	DC	Graphic equalizer IC1 1/2 $V_{CC}1$ decoupling capacitor. A small capacitor value can introduce supply effects and cause ripple.	
3	OUTPUT1	Output 1	
4	NF1	Graphic equalizer IC2 built-in op-amp inverting input	
5	1IN1	Electronic volume control IC1 audio signal input 1 (for INPUT1)	
6	INPUT1	Input 1. Approximately 60kΩ input impedance (1kHz, flat frequency response)	
7	1IN2	Electronic volume control IC1 audio signal input 2 (for INPUT1)	
8	V_{SS}	Ground	
9	V_{EE}	Electronic volume control audio signal circuit supply. Connect to V_{SS} if using a single-sided supply.	
10	CLK	 A01554	Clock input pin from the CPU. Schmitt inverter input.
11	DI		Data input pin from the CPU. Schmitt inverter input.
12	$+V_{CC}2$	+5V supply pin. V_{DD} supply should be applied before the $V_{CC}2$ supply.	
13	GND ($-V_{CC}1$)	Graphic equalizer IC2 and IC3 ground (or negative supply)	
14	V_{DD}	Electronic volume control audio signal circuit supply	
15	S	 A01555	IC select pin when using 2 ICs. When HIGH, initiates keycode 7C3 to select connection to V_{DD}. When LOW, initiates keycode 7C2 to select connection to V_{EE}.
16	2IN2	Electronic volume control IC1 audio signal input 2 (for INPUT2)	
17	INPUT2	Input 2. Approximately 60kΩ input impedance (1kHz, flat frequency response)	
18	2IN1	Electronic volume control IC1 audio signal input 1 (for INPUT2)	
19	NF2	Graphic equalizer IC3 built-in op-amp inverting input	
20	OUTPUT2	Output 2	

Note. Refer to LC7522 and LC7523 data sheets for pin function information concerning pins connected internally in the hybrid IC.

Operating Description

The STK301-090 comprises an LC7522 graphic equalizer electronic volume control IC and an LA3607 7-band graphic equalizer IC to form a 7-band, 2-channel electronic graphic equalizer hybrid IC.

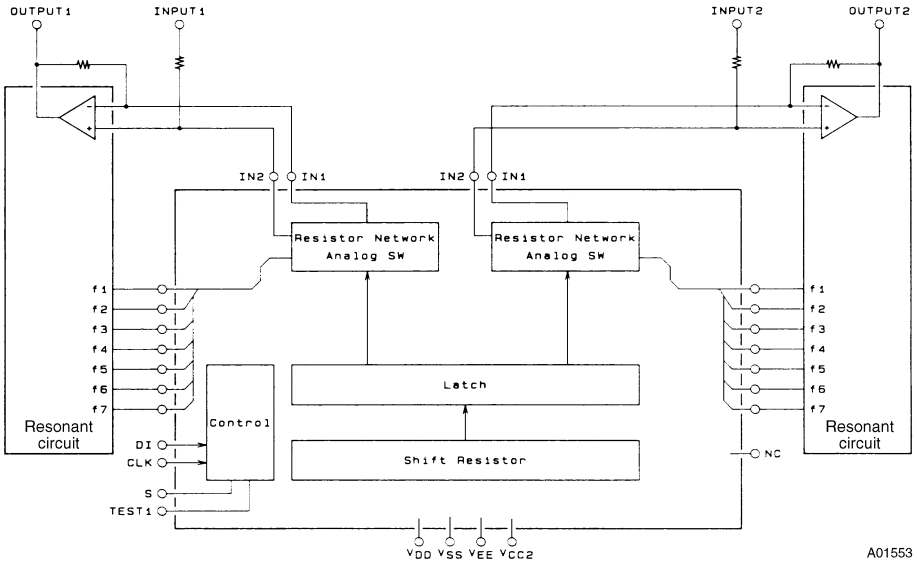
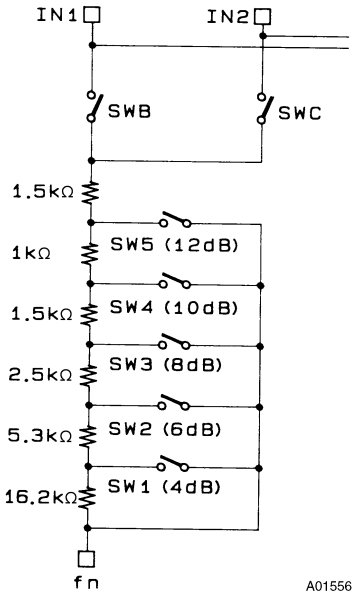


Figure 1. Equivalent Circuit Block Diagram

The LC7522 band filter connection pins, f(1) to f(7), are used. The center frequency corresponding to each band is shown below.

Pin name	Frequency
f(1)	60Hz
f(2)	150Hz
f(3)	400Hz
f(4)	1kHz
f(5)	2.5kHz
f(6)	6kHz
f(7)	15kHz

A 1MΩ resistor is connected from each pin to 1/2 V_{CC}1 to prevent pop noise when switching.



Resistor equivalent circuit (1 band only shown)

The graphic equalizer circuit comprises 7 resonant circuits and an output buffer amplifier (per channel). The variable resistor (LC7522) and resonant circuit capacitors C1 and C2 are built-in. The resonant circuits, employing semiconductor inductor elements, use resonance to reduce impedance and thereby change the gain.

Resonant Circuit

The resonant circuit uses semiconductor inductors, formed by RC elements buffered by op-amp and transistor active elements, to form an equivalent RLC series-resonant circuit. The STK301-090 resonant circuit buffer is formed by the transistor as shown in Figure 2.

The resonant frequency f_O is given by:

$$f_O = \frac{1}{2\pi\sqrt{C1 \times C2 \times R1 \times R2}}$$

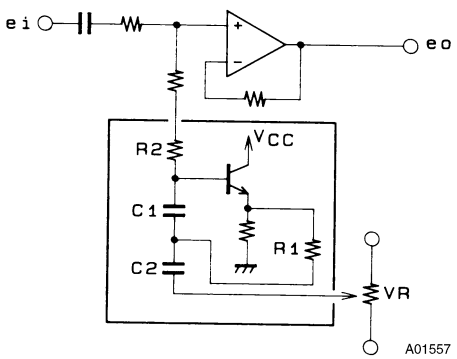
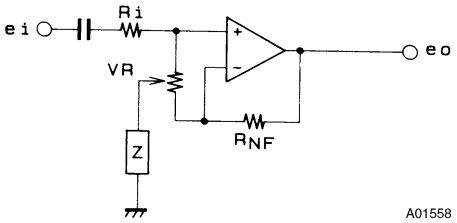


Figure 2. Resonant circuit

Flat Response, Boost and Cut

The built-in resonant and electronic volume control circuits are changed to vary the gain for the corresponding resonant frequency. An equivalent circuit for the sake of explanation is shown in Figure 3. Z represents the impedance of the resonant circuit shown in Figure 2.



Z is the resonant circuit impedance.
VR is the LC7522 IC.

Figure 3. Equivalent circuit

Flat Response

When the volume control is set to the center position and if Ri = R_{NF} and the following relationships are established:

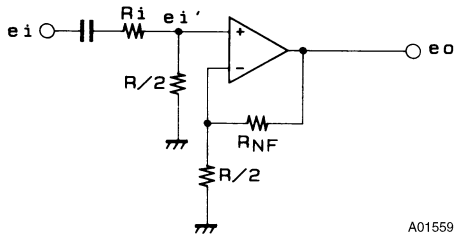
$$ei' = \frac{R/2}{Ri + R/2} \times ei$$

$$A_V = \frac{R_{NF} + R/2}{R/2}$$

In this case,

$$eo = A_V \times ei' = ei$$

so that the gain is independent of the resonant circuit and the frequency response becomes flat. If the maximum VR resistance is R, the resistance value at the center position is R/2.



Boost

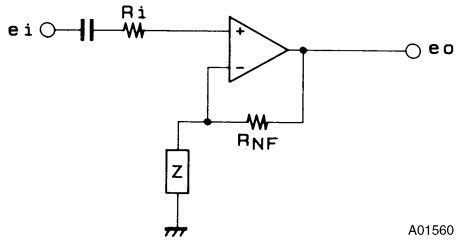
When the volume control is set to the boost position, the resonant circuit is connected in the output buffer amplifier negative feedback loop. In this case, if R >> Ri, R_{NF}, then:

$$A_V = \frac{R_{NF} + Z}{Z}$$

and the output voltage is given by:

$$eo = A_V \times ei = \frac{R_{NF} + Z}{Z} \times ei$$

The gain of the resonant circuit is at maximum when Z is at minimum, boosting the gain at that resonant frequency.



Cut

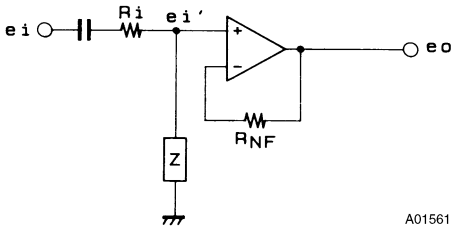
When the volume control is set to the cut position, the resonant circuit is connected in the output buffer amplifier input. In this case, if again ignoring R, then:

$$ei' = \frac{Z}{Ri + Z} \times ei,\ A_V = 1$$

and the output voltage is given by:

$$eo = A_V \times ei' = \frac{Z}{Ri + Z} \times ei$$

The gain of the resonant circuit is at minimum when Z is at minimum, cutting the gain at that resonant frequency.

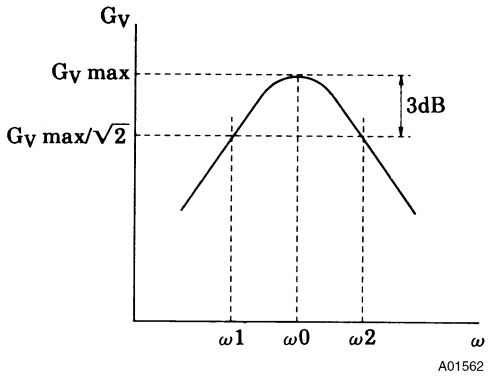


Resonance Peak Sharpness (Q)

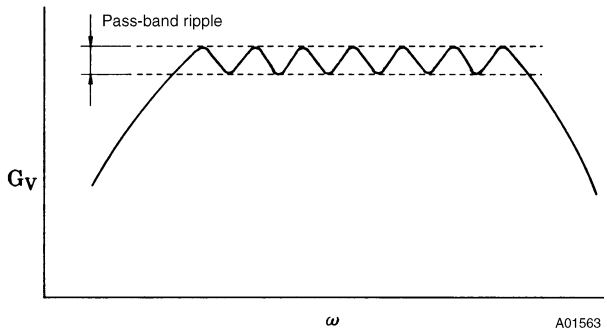
The resonance peak sharpness is determined by the maximum resonance peak value (G_V max at ω0) and the −3dB value (G_V max/$\sqrt{2}$) over the frequency interval ω2 − ω1. The value for Q is given by the following equation.

$$Q = \sqrt{\frac{C1 \times R2}{C2 \times R1}}$$

A larger Q indicates that the frequency bandwidth of the resonant circuit is narrower and hence the crossover between adjacent bands becomes more distinct. Under full boost conditions, the wave-like shape of the frequency response ripple increases whereas the peak of the resultant frequency is lowered.



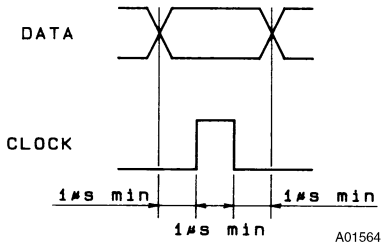
As the STK301-090 has only a limited number of frequency bands, the ripple increases under all bands maximum boost conditions. The value of Q is set to 3.5 under all bands maximum boost for a pass-band ripple of 4dB.

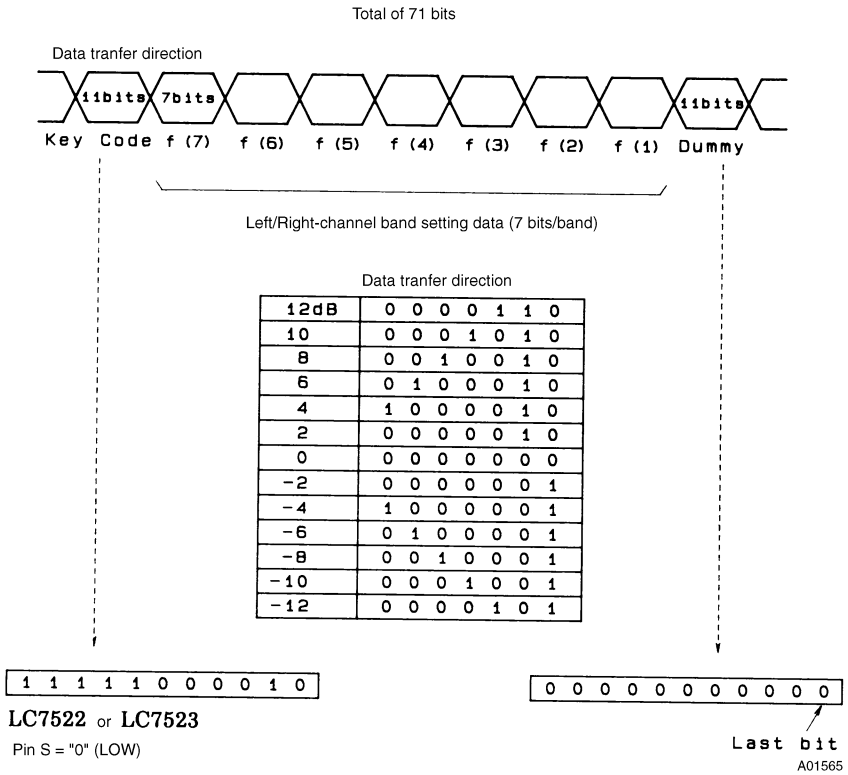


Data Codes

Turning on the power starts a process which transmits all 0 data for 60 clock cycles (initialization). Also, if the flow of data is interrupted, the remaining data or new data should be transferred after re-initialization.

When DI and CLK are connected to the LC75821 and other devices, the full initialization clock cycle is also sent to these devices.

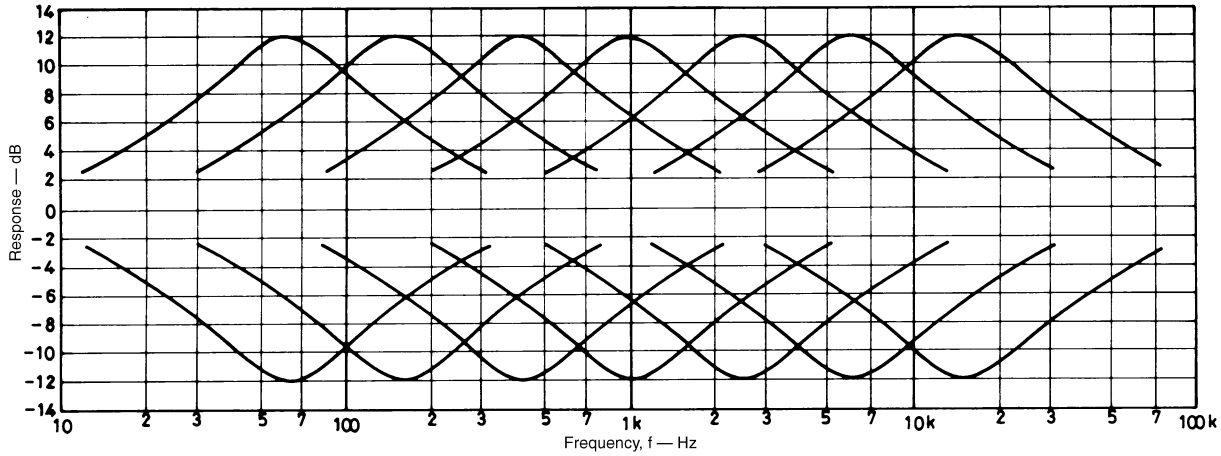




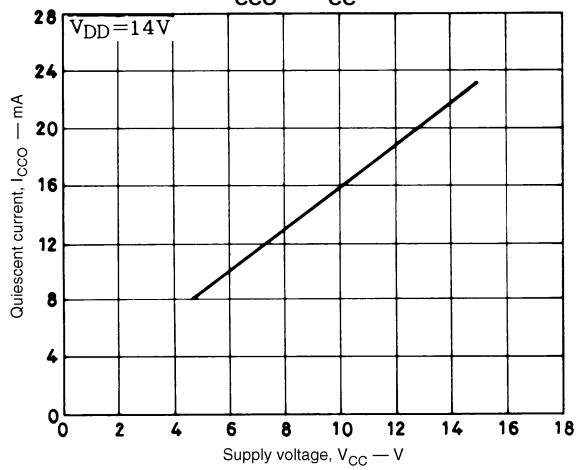
Design Notes

- A 1000pF or larger capacitor should be connected between supply pins and V_{SS}.
- A 2kΩ resistor should be connected in the CLK and DI lines if the microcontroller transfers control signals before the STK301-090 V_{DD} supply stabilizes.
- Caution should be taken when handling the STK301-090 because the internal CMOS LSIs are prone to damage from static electricity.
- Refer to the LC7522 data sheet for specific details about that device.

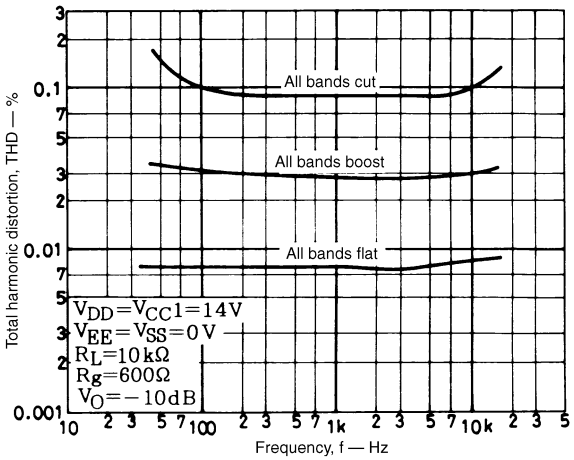
Frequency response



I_{CCO} — V_{CC}



THD — f



THD — V_O