Ordering number : EN4621A

Thick Film Hybrid IC

No. 4621A

SANYO

STK4040XI

AF Power Amplifier (Split Power Supply) (70 W min, THD = 0.008%)

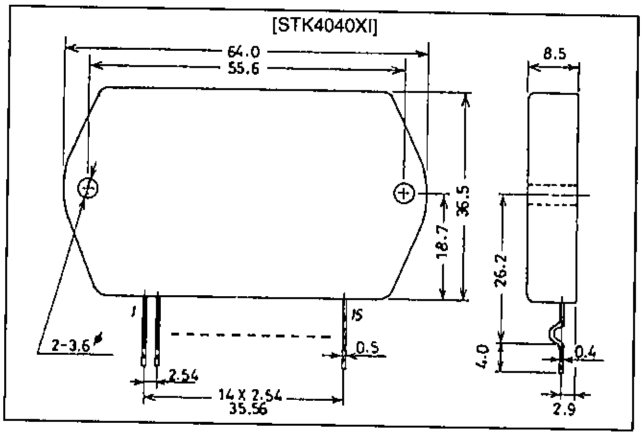
Features

- Compact packaging supports slimmer set designs
- Series designed from 50 up to 150 W and pin-compatibility
- Simpler heat sink design facilitates thermal design of slim stereo sets
- Current mirror circuit, cascade circuit and pure-complimentary circuit application reduce distortion to 0.008 %
- Supports addition of electronic circuits for thermal shutdown and load-short protection circuit as well as pop noise muting which occurs when the power supply switch is turned on and off.

Package Dimensions

unit: mm

4075



Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Condition	Rating	Unit
Maximum supply voltage	V_{CC} max		± 63	V
Thermal resistance	θj-c		1.4	°C/W
Junction temperature	Tj		150	°C
Operating substrate temperature	Tc		125	°C
Storage temperature	Tstg		−30 to +125	°C
Available time for load shorted	t_s *1	V_{CC} = ± 43.5 V, R_L = 8 Ω, f = 50 Hz, P_O = 70 W	1	s

Recommended Operational Conditions at Ta = 25°C

Parameter	Symbol	Condition	Rating	Unit
Recommended supply voltage	V_{CC}		± 43.5	V
Load resistance	R_L		8	Ω

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Operating Characteristics

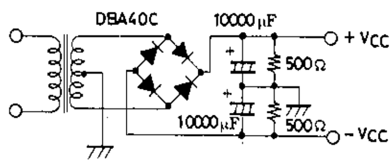
at Ta = 25°C, V_{CC} = ± 43.5 V, R_L = 8 Ω, VG = 40 dB, Rg = 600 Ω, 100 k LPF ON, R_L (non-inductive)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Quiescent current	I_{CCO}	V_{CC} = ± 52.5 V	15		120	mA
Output power	P_O	THD = 0.008 %, f = 20 Hz to 20 kHz	70			W
Total harmonic distortion	THD	P_O = 1.0 W, f = 1 kHz			0.008	%
Frequency response	f_L, f_H	P_O = 1.0 W, $^{+0}_{-3}$ dB		20 to 50k		Hz
Input resistance	r_i	P_O = 1.0 W, f = 1 kHz		55		kΩ
Output noise voltage	V_{NO}*2	V_{CC} = ± 52.5 V, Rg = 10 kΩ			1.2	mVrms
Neutral voltage	V_N	V_{CC} = ± 52.5 V	−70	0	+ 70	mV

Note: Use rated power supply for test unless otherwise specified.

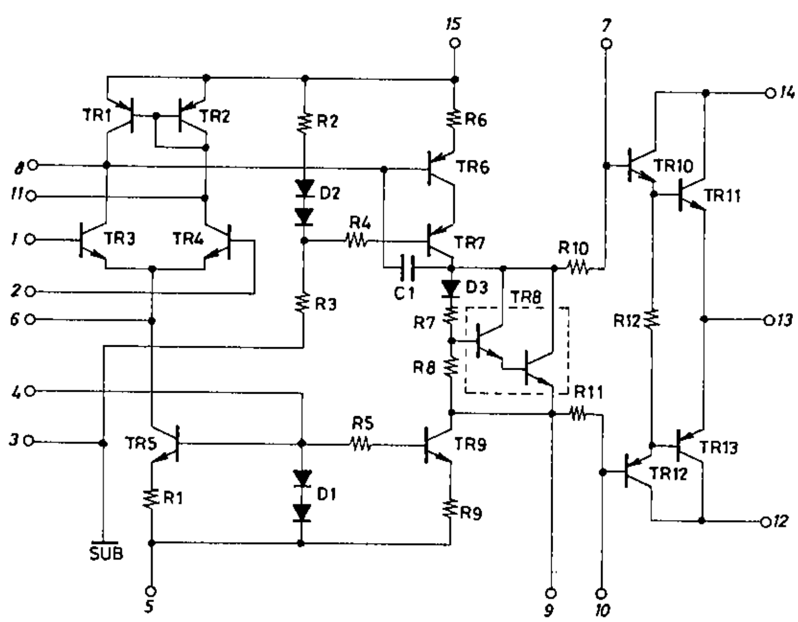
*1 When measuring permissible load short time and output noise voltage use transformer power supply indicated below.

*2 Output noise voltage represents the peak value on the rms scale (VTVM). The noise voltage waveform does not include the pulse noise.

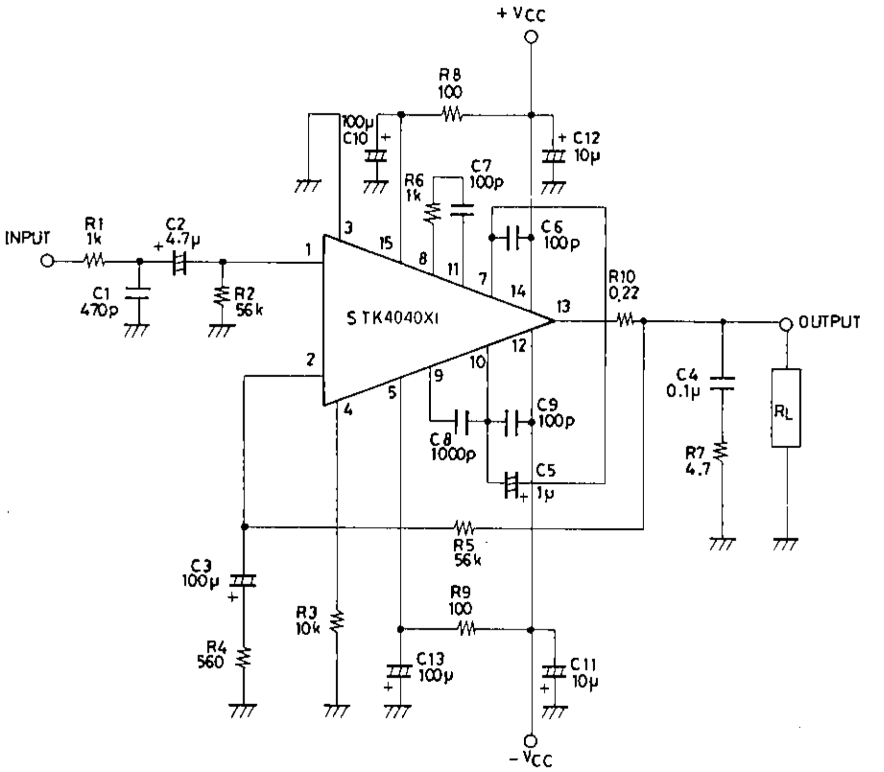


Specified Transformer Power Supply (MG-200 Equivalent)

Equivalent Circuit

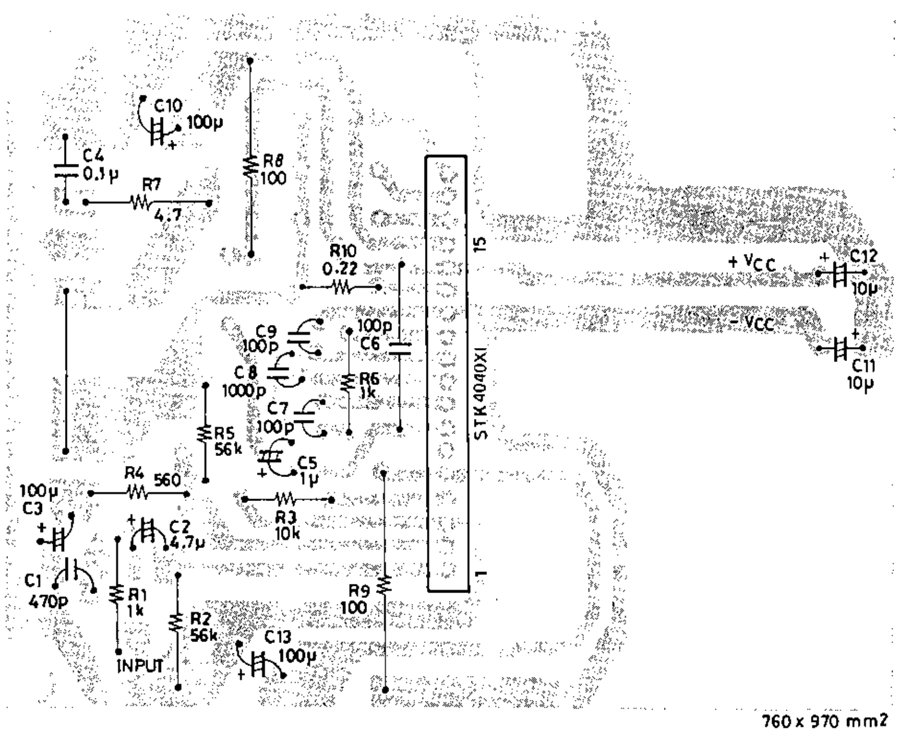


Application Circuit: 70W min Single Channel AF Power Amplifier



Unit (resistance: Ω, capacitance: F)

Sample Printed Circuit Pattern for Application Circuit (Copper-foiled side)



Unit (resistance: Ω, capacitance: F)

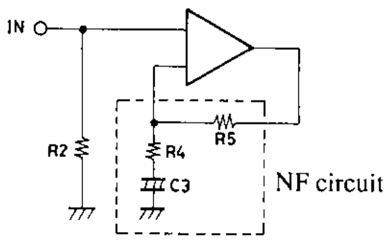
Description of External Parts

R_1, C_1 : Input filter circuit
- Reduces high-frequency noise.

C_2 : Input coupling capacitor
- DC current suppression. A reduction in reactance is effective because of increases in capacitor reactance at low frequencies and 1/f noise dependence on signal source resistance which result in output noise worsening.

R_2 : Input bias resistor
- Biases the input pin to zero.
- Effects V_N stability (refer to NF circuit).
- Due to differential input, input resistance is more or less determined by this resistance value.

R_4, R_5 : NFB circuit (AC NF circuit). Use of resistor with 1% error is suggested.
C_3 (R_2)



C_3 : AC NF capacitor
R_4, R_5 : Used for VG setting.

- VG settings are obtained using R_4 and R_5 according to the following equation:

$\log 20 \cdot \frac{R_5}{R_4}$ 40 dB is recommended.

- Low-frequency cutoff frequency settings are obtained using R_4 and C_3 according to the following equation:

$$f_L = \frac{1}{2\pi \cdot R_4 \cdot C_3} \quad [Hz]$$

When changing the VG setting, you should change R_4 which requires a recheck of the low cutoff frequency setting. When the VG setting is changed using R_5, the setting should ensure R_2 equals R_5 so that V_N balance stability is maintained. If the resistor value is increased more than the existing value, V_N balance may be disturbed and result in deterioration of V_N temperature characteristics.

R_3 : Differential constant-current bias resistor

R_6, R_7 : For oscillation suppression and phase compensation applications
(For use with differential stage applications)

R_7, C_4 : For oscillation suppression and phase compensation applications
(A Mylar capacitor is recommended for C_4 for use with output stage applications)

C_6, C_9 : For oscillation suppression and phase compensation applications
Power stage (Must be connected near the pin) C_6: Positive (+) power C_9: Negative (–) power

C_8 : For oscillation suppression and phase compensation applications
(Oscillation suppression before power step clip)

C_5 : For oscillation suppression and distortion improvement applications

R_8, C_{10} : Ripple filter circuit on positive (+) side.

R_9, C_{13} : Ripple filter circuit on negative (–) side.

C_{11}, C_{12} : For oscillation suppression applications
- Used for reducing power supply impedance to stable IC operation and should be connected near the IC pin. We recommend that you use an electrolytic capacitor.

R_{10} : Output resistor
Increases load shorting endurance capacity during times of high output.