SGS-THOMSON MICROELECTRONICS

STV9410

CRT AND LCD SEMI-GRAPHIC DISPLAY PROCESSOR

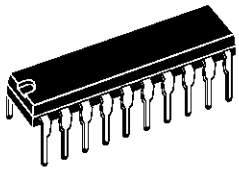
- CMOS SINGLE CHIP CRT AND LCD DISPLAY PROCESSOR
- BUILT IN 6 KBYTE RAM
- 25 ROWS OR MORE OF 40 CHARACTERS
- CRT MODE :
  - ANALOG Y LUMINANCE OUTPUT OF 4-BIT DAC
  - R,G,B DIGITAL COLOR OUTPUTS
  - FAST BLANKING OUTPUT FOR VIDEO SWITCH COMMAND
  - SYNCHRONIZATION INPUT AND OUTPUT
  - MASTER AND SLAVE SYNCHRONIZATION MODES
- LCD MODE :
  - 8 GREY LEVELS
  - 4 BIT DATA WITH CLOCK OUTPUT
  - 3 OUTPUTS FOR LCD DRIVERS SYNCHRONIZATION
  - CONTRAST ANALOG COMMAND WITH DAC OUTPUT
- 128 ALPHANUMERIC CODES AND 128 SEMI-GRAPHIC CODES IN INTERNAL ROM
- PARALLEL ATTRIBUTES THANKS TO 2 BYTE CODES
- 128 ALPHANUMERIC AND 96 SEMI-GRAPHIC USER DEFINABLE CODES DOWN-LOADABLE IN RAM
- 3-WIRE ASYNCHRONOUS SERIAL MCU INTERFACE
- SQUARE WAVE OR LOGICAL PROGRAMMABLE OUTPUT
- FULLY PROGRAMMABLE WITH 7 16-BIT CONTROL REGISTERS
- 24-PIN SO OR 20-PIN DIP PACKAGES

DESCRIPTION

STV9410 controller is a VLSI CMOS Display Processor. Time base generator, display control & refresh logic, interface for transparent MCU memory access, ROM character sets, memory to store display data & page codes and control registers are gathered on a single chip component packed in a short 20 DIP or SO plastic package.

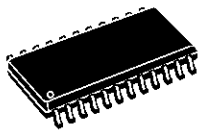
Using its 3-wire serial interface, working in both read and write mode to program 7 control registers and to access internal RAM, STV9410 is a highly flexible processor.

The STV9410 provides the user an easy to use and cost effective solution to display alphanumeric and semigraphic Information on CRT and LCD screens.



DIP20
(Plastic Package)

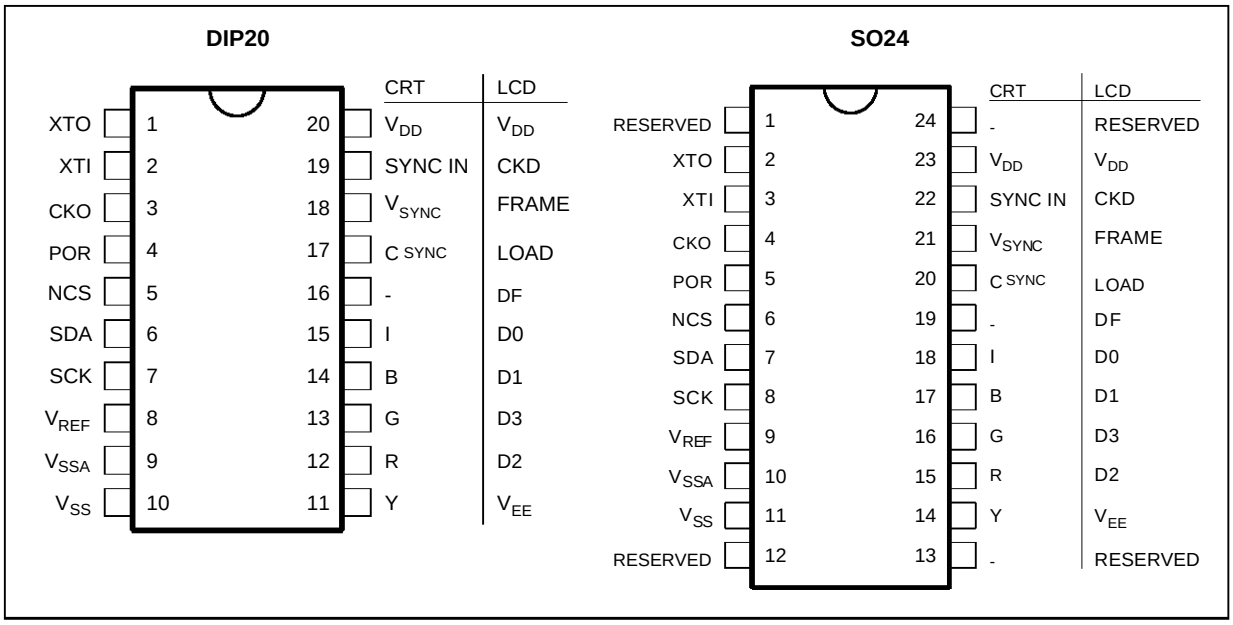
ORDER CODE : STV9410P



SO24
(Plastic Micropackage)

ORDER CODE : STV9410D

PIN CONNECTIONS



PIN DESCRIPTION

Symbol	Pin n°		I/O	Description
	DIP20	SO24		
CRT MODE				
-	-	1	-	Reserved
XTO	1	2	O	Crystal oscillator output
XTI	2	3	I	Crystal oscillator or clock input
CKO	3	4	O	Clock output
POR	4	5	O	Programmable output port
NCS	5	6	I	Serial interface selection
SDA	6	7	I/O	Serial data input/output
SCK	7	8	I	Serial interface clock input
V_{REF}	8	9	I	Reset input and ref supply of Y DAC
V_{SSA}	9	10	S	Ref ground of Y DAC
V_{SS}	10	11	S	Ground
-	-	12	-	Reserved
-	-	13	-	Reserved
Y	11	14	O	Luminance output
R	12	15	O	Red output
G	13	16	O	Green output
B	14	17	O	Blue output
I	15	18	O	Fast blanking output
-	16	19	O	Reserved
C_{SYNC}	17	20	O	Composite synchro output
V_{SYNC}	18	21	O	Vertical synchro output
SYNC IN	19	22	I/O	Synchro input
V_{DD}	20	23	S	+5v power supply
-	-	24	-	Reserved

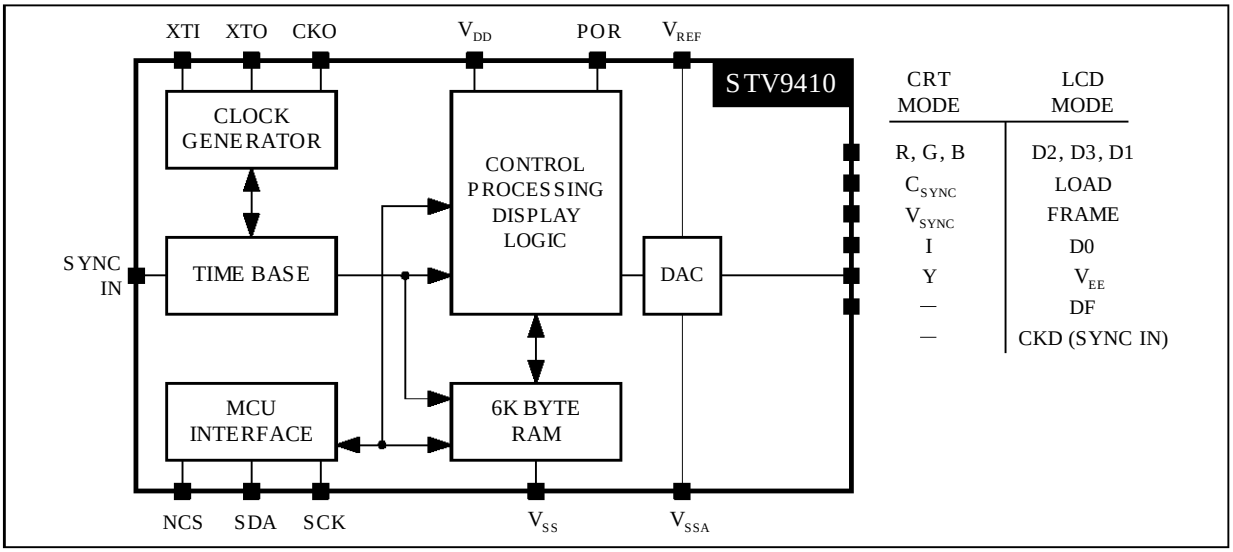
9410-01.TBL

PIN DESCRIPTION (continued)

Symbol	Pin n°		I/O	Description
	DIP20	SO24		
LCD MODE				
-	-	1	-	Reserved
XTO	1	2	O	Crystal oscillator output
XTI	2	3	I	Crystal oscillator or clock input
CKO	3	4	O	Clock output
POR	4	5	O	Programmable output port
NCS	5	6	I	Serial interface selection
SDA	6	7	I/O	Serial data input/output
SCK	7	8	I	Serial interface clock input
V_{REF}	8	9	I	Reset input and ref supply of contrast adjustment
V_{SSA}	9	10	S	Ref ground of contrast adjustment
V_{SS}	10	11	S	Ground
-	-	12	-	Reserved
-	-	13	-	Reserved
V_{EE}	11	14	O	Constrast adjustment
D2	12	15	O	D2 Data output
D3	13	16	O	D3 Data output
D1	14	17	O	D1 Data output
D0	15	18	O	D0 Data output
DF	16	19	O	LCD polarity output
LOAD	17	20	O	Load output (line)
FRAME	18	21	O	Frame output
CKD	19	22	I/O	Data Clock
V_{DD}	20	23	S	+5v power supply
-	-	24	-	Reserved

9410-02.TBL

BLOCK DIAGRAM



9410-03.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}*	Supply Voltage	-0.3, +7.0	V
V_{IN}*	Input Voltage	-0.3, +7.0	V
T_{oper}	Operating Temperature	0, +70	^oC
T_{stg}	Storage Temperature	-40, +125	^oC
P_{tot}	Power Dissipation	300	mW

9410-03.TBL

* with respect to V_{SS}

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V, V_{SS} = 0V, T_a = 0 to + 70^{o}C, fxtal = 8 to 10MHz, unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	4.75	5.0	5.25	V
I_{DD}	Supply current *	-	-	50	mA
INPUTS					
NCS, SDA, SCK, SYNC IN, XTI					
V_{IL}	Input low voltage	0	-	0.8	V
V_{IH}	Input high voltage (except XTI)	2	-	V_{DD}	V
I_{IL}	Input leakage current (except XTI) (0 < V_{IN} < V_{DD})	-10	-	+10	µA
C_{IN}	Input capacitance (except XTI)	-	10	-	pF
V_{REF}					
V_{rh}	Voltage reference of DAC	1.5	-	V_{DD}	V
V_{rst}	Reset level on V_{REF}	0	-	0.4	V
R_{IN}	V_{REF} to V_{SSA} internal resistance	0.4	-	1.0	kΩ
V_{SSA}	Reference level of DAC	0	-	V_{DD}	V
OUTPUTS					
SDA, C_{SYNC}, V_{SYNC}, R, G, B, I, SYNC IN, DF, XTO, CKO, POR					
V_{OL}	Output low voltage (I_{OL} = 1.6mA)	0	-	0.4	V
V_{OH}	Output high voltage (I_{OH} = - 0.1mA)	0.8 V_{DD}	-	V_{DD}	V
Y					
	Output voltage (V_{REF}=5V, V_{SSA}=0, I_{OUT}=0)				
L_I	Integral linearity	-	-	0.25	V
L_D	Differential linearity	-	-	0.1	V
Z_{OUT}	Output impedance	-	-	0.5	kΩ
T_p	Propagation time at V_{OUT} 90% of V_{FINAL}, C_L=20pF, I_{OUT}=0, V_{REF}=5V, V_{SSA}=0V	-	-	80	ns

9410-04.TBL

* no load on outputs

TIMINGS

(V_{DD} = 5V ±5%, V_{SS} = 0V, T_a = 0 to + 70°C, fxtal = 8 to 10MHz,
V_{IL} = 0.8V, V_{IH} = 2V, V_{OL} = 0.4V, V_{OH} = 2.4V, C_L = 50pF, unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
SERIAL INTERFACE NCS, SCK, SDA (Figure 1)					
T_{csl}	NCS low to SCK falling edge	0			ns
T_{sch}	SCK pulse width high	80			ns
T_{scl}	SCK pulse width low	80			ns
f_{SCK}	Serial Clock Frequency			4	MHz
T_{sds}	Set up time of SDA on SCK rising edge	20			ns
T_{sdh}	Hold time of SDA after SCK rising edge	20			ns
T_{sdv}	Access time in read mode		50		ns
T_{sdx}	Hold data in read mode	0			ns
T_{sdz}	Serial interface disable time		50		ns
T_{read}	Delay before Valid Data	2			µs
OSCILLATOR INPUT (XTI) (Figure 1)					
T_{wh}	Clock high level	30			ns
T_{wl}	Clock low level	30			ns
F_{clk}	Clock frequency	8		10	MHz
RESET (V_{REF})					
T_{res}	Reset Low level pulse	2			µs
OUTPUT SIGNALS SDA, C_{SYNC}, V_{SYNC}, R, G, B, I, SYNC IN, DF, XTO, CKO, POR (Figure 2)					
T_{ph},T_{pl}	Propagation time C_L = 30 pF C_L = 100 pF			50 100	ns ns
T_{skew}	Skew between R, G, B, I signals			30	ns

(V_{DD} = 5V ±5%, V_{SS} = 0V, T_a = 0 to + 70°C, fxtal = 8 to 10MHz,
V_{OL} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, C_L = 100pF, unless otherwise specified)

LCD INTERFACE D0, D1, D2, D3, CKD, LOAD, DF, FRAME (Figure 3)					
t_{CYC}	CKD Shift Clock Period	4 x Pxtal			ns
t_{CH}	CKD Clock High	150			ns
t_{CL}	CKD Clock Low	150			ns
t_{WLD}	Load Pulse Width	150			ns
t_{SU}	Data Set-up Time	150			ns
t_{DH}	Data Hold Time	150			ns
t_{DF}	DF Delay from Load			100	ns
t_{SUF}	Frame Set-up before Load	150			ns

9410-05.TBL

Figure 1 : Microcontroller Interface Timings

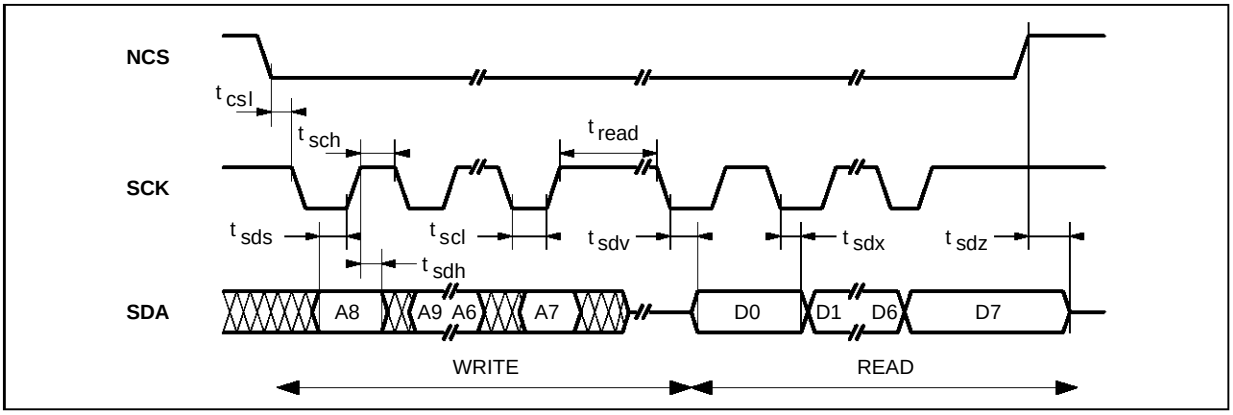


Figure 2 : Output Signals Delay versus Clock

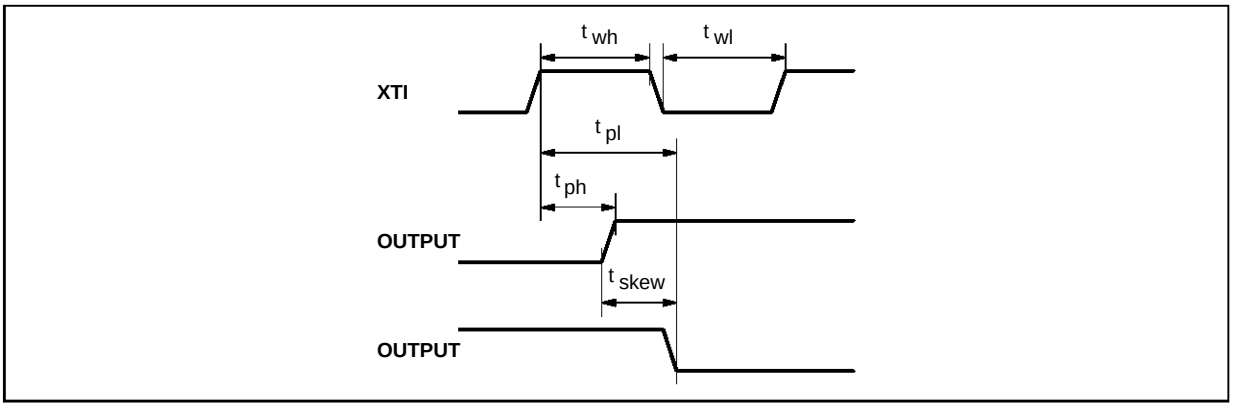
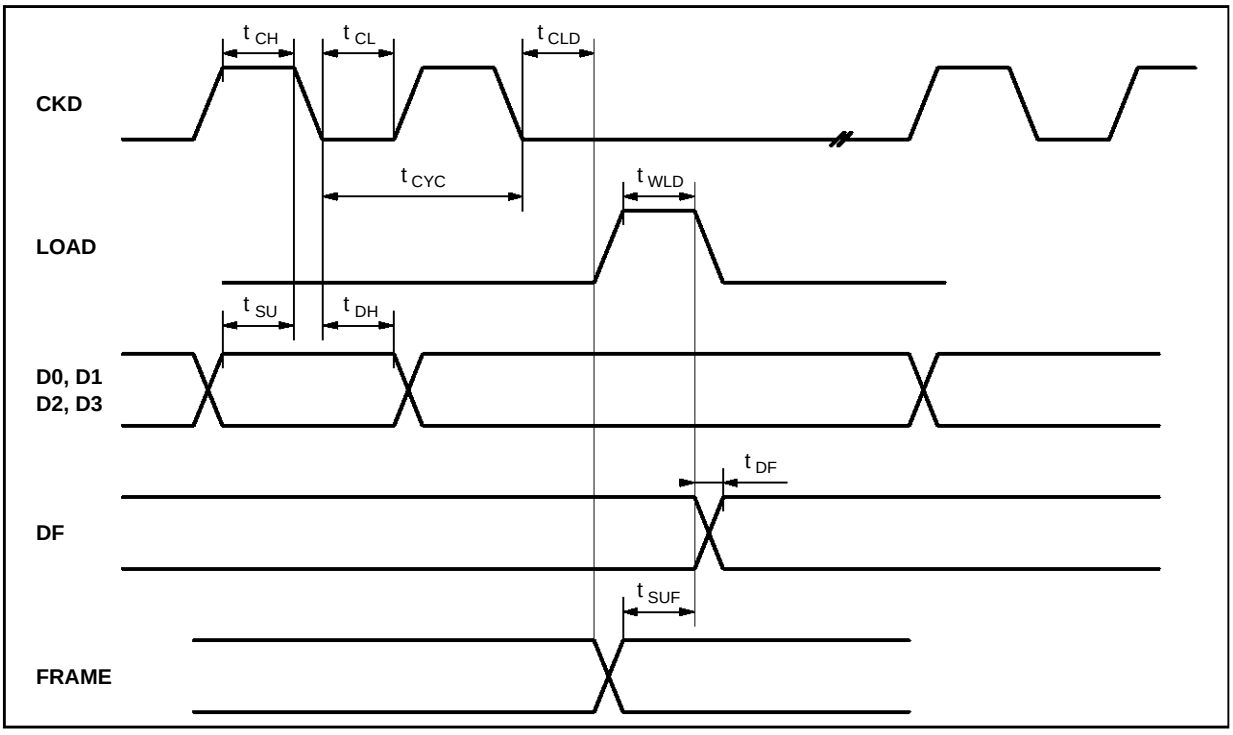


Figure 3 : LCD Interface Timings



2. FUNCTIONAL DESCRIPTION

STV9410 display processor operation is controlled by a host microcomputer via a 3-wire serial bus. It is fully programmable through seven internal read/write registers and performs all the display functions either for CRT screen or LCD passive matrix by generating pixels from data stored in its internal memory. In addition, the host microcomputer can have straightforward accesses to the on-chip 6 Kbytes RAM, even during the display operation.

The following functions are integrated in the STV9410 :

- Crystal oscillator,
- Programmable timing generator,
- Microcomputer 3-wire serial interface,
- ROM character generator including 128 alphanumeric and 128 semigraphic character sets,
- 6 Kbytes on chip RAM to store character codes, user definable character sets, and any host microcomputer data,

and in CRT mode :

- Y output driven by a 4-bit DAC,
- Programmable master or slave synchro modes,
- R, G, B, I outputs,

in LCD mode :

- LCD interface for passive multiplexed matrix,
- 7 grey levels plus black.

2.1 SERIAL INTERFACE

This 3-wire serial interface can be used with any microcomputer. Data transfer is supported by hardware peripherals like SPI or UART and can be emulated with standard I/O port using software routine (see application note).

NCS input enables transfer on high to low transition and transfer stays enabled as long as NCS input remains at logical low level. NCS input disables transfer as soon as low to high transition occurs, whatever transfer state is, and transfer remains disabled as long as NCS input remains at logical high level.

SCK input receives serial clock; it must be high at the beginning of the transfer; data is sampled on rising edge of SCK.

SDA input (in write mode) receives data which must be stable at least t_{sds} before and at least t_{sdh} after SCK rising edge. In read mode, SDA receives address and read command (R/W bit) and then it switches from input state to output state to send data (see Data transfer and Application Note).

Data Transfer in Write Mode

The host MCU writes data into STV9410 registers or memory. The MCU sends first MSB address with R/W bit clear, it sends secondly LSB address followed by data byte(s). STV9410, then, internally increments received address, ready to store a second data byte if needed, and so on, as long as NCS remains low (see Figure 4). LSB are sent first.

Data Transfer in Read Mode

The host MCU reads data from STV9410 registers or memory. The MCU sends first MSB address with R/W bit set, it sends secondly LSB address, then SDA pin switches from input state to output state and provides data byte(s) at SCK MCU clock rate. Notice that a minimum delay is needed before sending the first SCK rising edge to sample the first data bit (at least 2µs). After each data byte STV9410 internally increments address and it sends next data at SCK frequency. SDA remains in output state as long as NCS remains low (see Figure 5).

Address auto-incrementation allows host MCU to use 8, 16, 32-bit data words to optimize transfer rate. LSB are sent first. SCK max speed is 4MHz.

Figure 4 : Serial Interface Write Mode

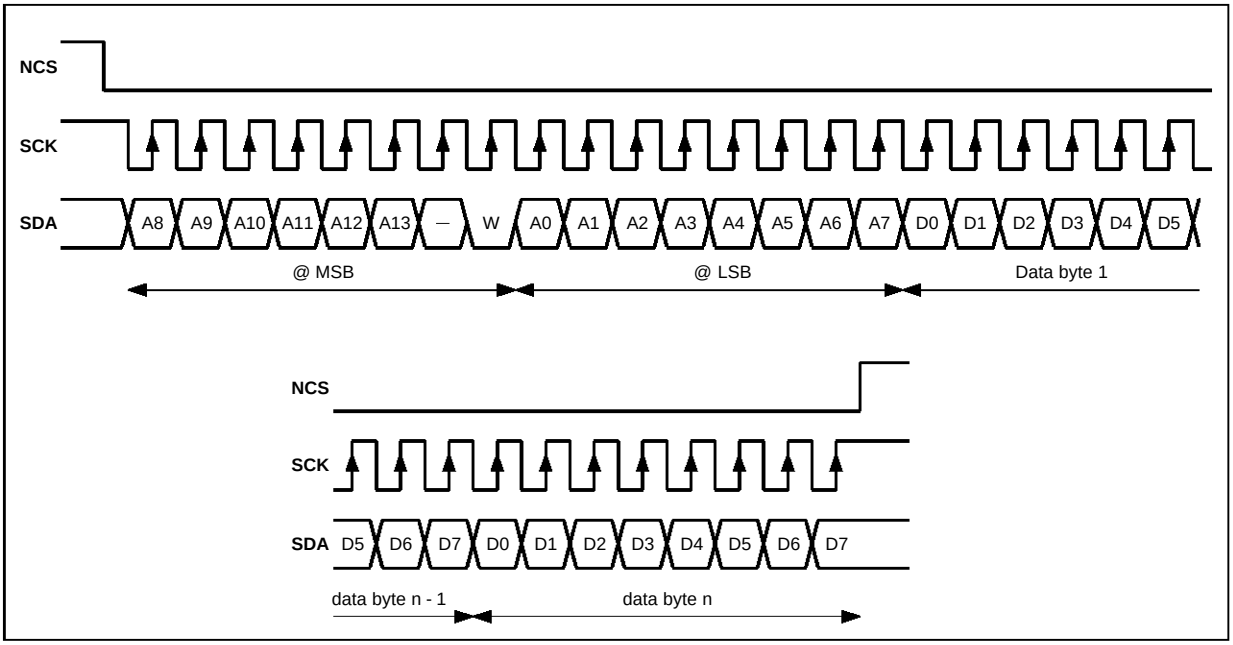
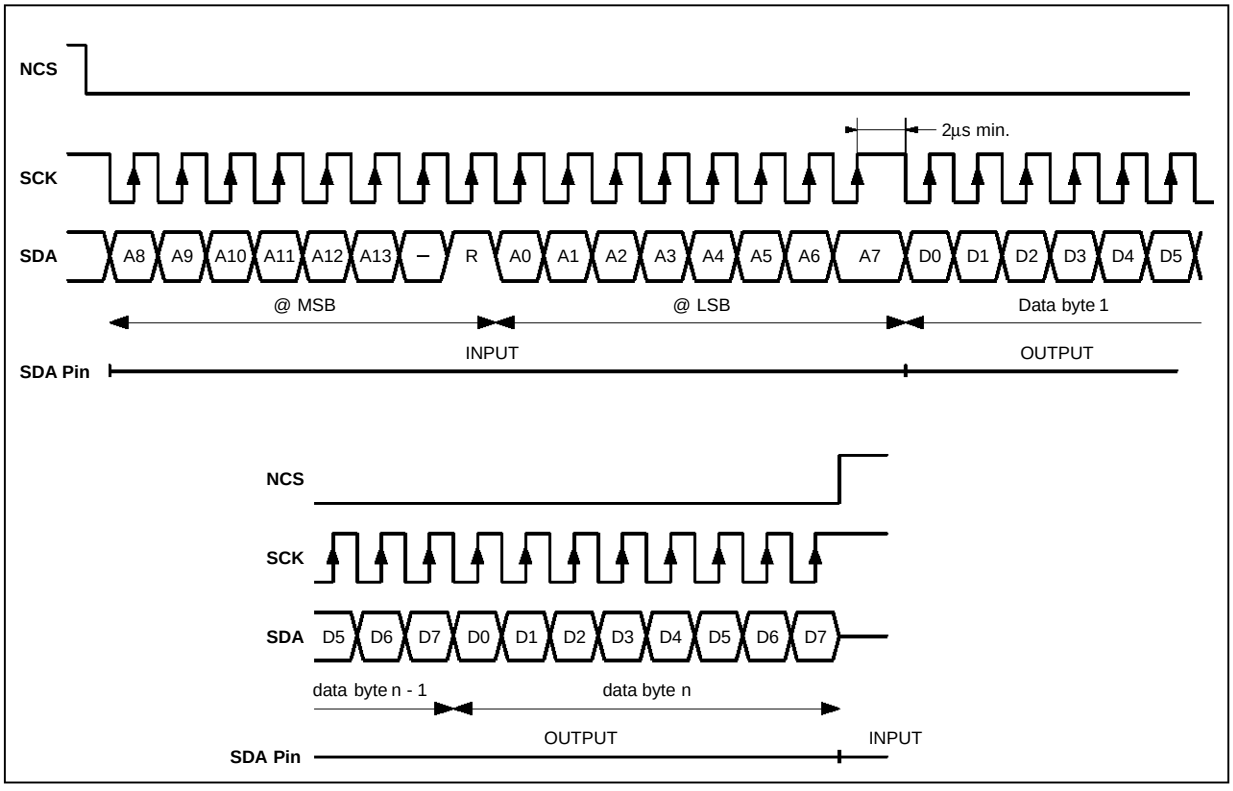
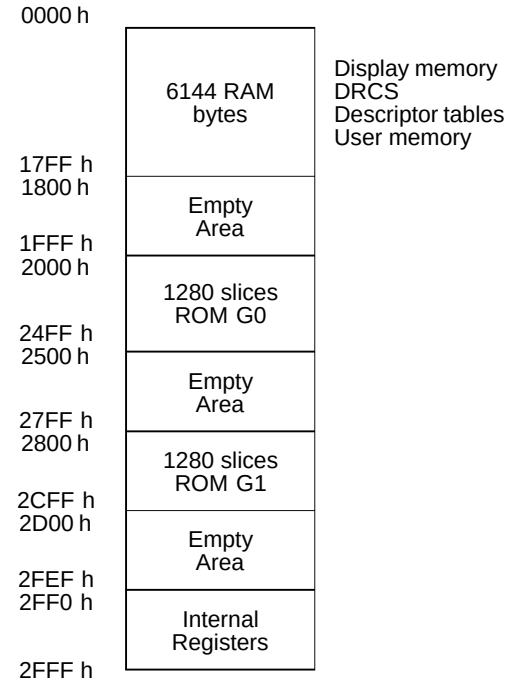


Figure 5 : Serial Interface Read Mode



2.2. ADDRESSING SPACE

STV9410 registers, RAM and ROM are mapped in a 12 kbytes addressing space. The mapping is the following :



2.2.1 Register Set

VERT

2FF1	LCD	ILC	C/H	V/P	VSE	HSE	-	F8
2FF0	F7	F6	F5	F4	F3	F2	F1	F0

LCD : LCD/CRT mode
ILC : Interlaced/non-interlaced
C/H : Composite/horizontal synchro
V/P : Vertical synchro/real time port
VSE : Vertical synchro enable
HSE : Horizontal synchro enable
F (8:0) : Number of scan line per frame

HORI

2FF3	-	-	-	-	-	MG2	MG1	MG0
2FF2	-	-	L5	L4	L3	L2	L1	L0

MG (2:0) : Margin duration
L (5:0) : Line duration

HSYN

2FF5	SU7	SU6	SU5	SU4	SU3	SU2	SU1	SU0
2FF4	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0

SU (7:0) : Synchro rising edge position
SD (7:0) : Synchro falling edge position

POR

2FF7	VOE	-	-	-	-	-	TE	PV
2FF6	N7	N6	N5	N4	N3	N2	N1	N0

VOE : Video output enable
TE : Timer enable
PV : Port value
N (7:0) : Square wave period

ADDR

2FF9	-	P12	P11	P10	P9	P8	P7	P6
2FF8	-	G12	G11	G10	-	A12	A11	A10

P (12:6) : Address of first descriptor of page to display
G (12:10) : User definable graphic character set address
A (12:10) : User definable alphanumeric character set address

DISP

2FFB	IMG	GMG	RMG	BMG	-	-	-	HIC
2FFA	FLE	CCE	IN1	IN2	BR3	BR2	BR1	BR0

IMG, GMG, RMG, BMG : Margin value of I, G, R, B outputs
HIC : High contrast, forces black and white on outputs
FLE : flashing enable
CCE : Conceal enable
IN1, IN0 : Fast blanking mode
BR (3:0) : Luminosity adjustment on Y output

CURS

2FFD	CEN	CBL	CUL	-	C12	C11	C10	C9
2FFC	C8	C7	C6	C5	C4	C3	C2	C1

CEN : Cursor enable
CBL : Cursor blinking
CUL : Cursor underlining
C (12:1) : Cursor address

2.2.2 Descriptor

UNIFORM

MSB	0	RTP	FFB	-	I	C2	C1	C0
LSB	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0

RTP : Real time port
FFB : Field flyback
I : Fast blanking
C (2:0) : Strip color (G, R, B)
SL (7:0) : Number of scan line of the strip

CHARACTER

MSB	1	RTP	DE	ZY	C12	C11	C10	C9
LSB	C8	C7	C6	C5	C4	C3	C2	C1

RTP : Real time port
DE : Display enable
ZY : Vertical zoom
C (12:1) : Address of first character to display

2.2.3 Code Format

ALPHANUM

MSB (ODD)	CHARACTER NUMBER							
LSB (EVEN)	0	IV	DW	DH	FL	FC2	FC1	FC0

CHARACTER NUMBER : lower than 80h in ROM
from 80h to FFh in RAM
IV : Inverted video
DW : Double width
DH : Double height
FL : Flashing
FC (2:0) : Foreground color (G, R, B)

GRAPHIC

MSB (ODD)	CHARACTER NUMBER							
LSB (EVEN)	1	BC2	BC1	BC0	FL	FC2	FC1	FC0

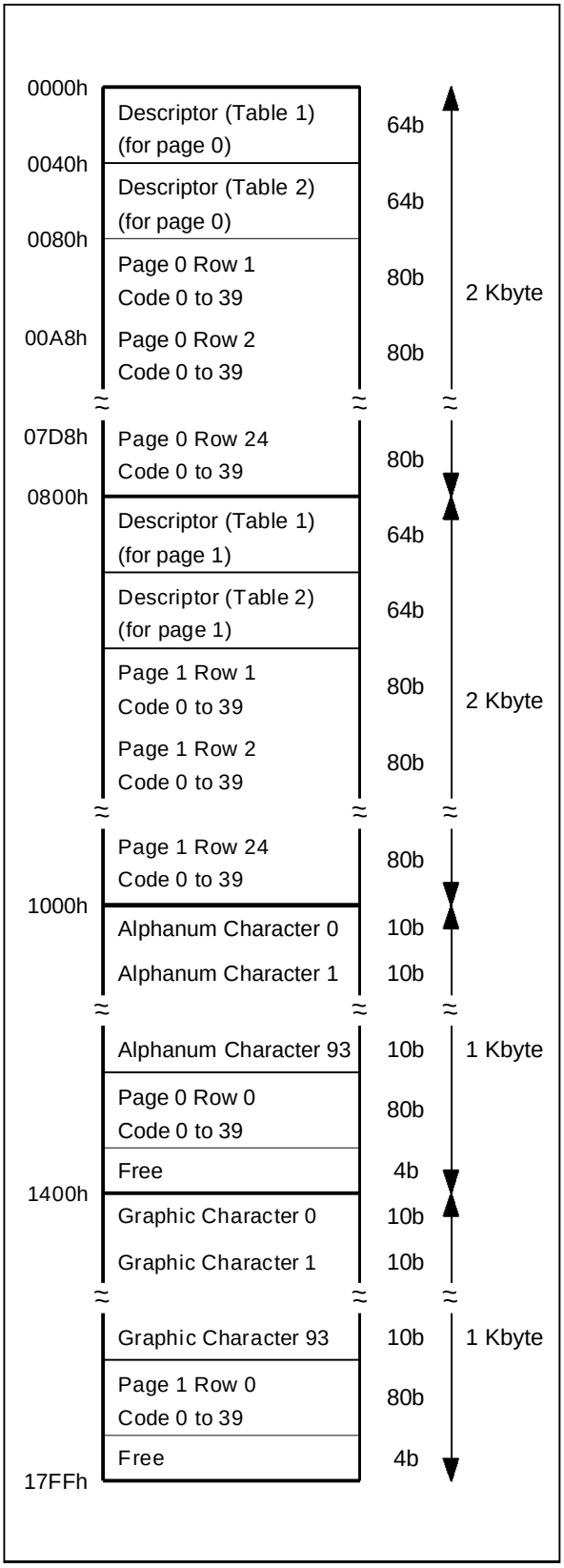
CHARACTER NUMBER : lower than 80h in ROM
from 80h to DFh in RAM
BC (2:0) : Background color (G, R, B)
FL : Flashing
FC (2:0) : Foreground color (G, R, B)

CONTROL

MSB (ODD)	1	1	1	EOL	IF	IB	UL	CC
LSB (EVEN)	1	BC2	BC1	BC0	HG	FC2	FC1	FC0

EOL : End of line
IF, IB : Fast blanking foreground/background
UL : Underline
CC : Conceal
BC (2:0) : Background color (G, R, B)
HG : Hold graphic
FC (2:0) : Foreground color (G, R, B)

2.2.4 Example of RAM Maping



2.3 CLOCK AND TIMING GENERATOR

The whole timing is derived from XTI input frequency which can be an external generator or a crystal signal thanks to XTO/XTI oscillator.This clock is also pixel frequency which can be chosen between 8MHz to 10MHz (pxlck). This clock is available on CKO pin. It should be use for the MCU, saving a crystal in the application.

The active area of a video line is 320 pixels periods long (40 characters of 8 pixels wide). Number of lines per frame, margin width, line duration, leading and trailing edges of horizontal synchronization are fully programmable in CRT mode using VERT, HORI, HSYN registers.

A RESET, can be applied to STV9410 by pulling low V_{REF} pin ($\leq$ 0.4V).

On RESET, default values are forced into configuration registers and video outputs are at low level.

All unused bit of registers are always read as ”0”.

2.3.1 Time Base Registers

Vertical Time Base and Configuration Register (VERT)
Internal address : 2FF1-2FF0 h
RESET value :01-36 h
(@ = RESET default configuration)

2FF1 h	LCD	ILC	C/H	V/P	VSE	HSE	-	F8
@	0	0	0	0	0	0	0	1

2FF0 h	F7	F6	F5	F4	F3	F2	F1	F0
@	0	0	1	1	0	1	1	0

LCD : 1 LCD mode
0 CRT mode @

ILC : 1 Interlaced scanning
0 non-interlaced scanning @

C/H : 1 C_{SYNC} is composite synchro
0 C_{SYNC} is horizontal synchro @

V/P : 1 V_{SYNC} is vertical synchro
0 V_{SYNC} is RTP bit of current descriptor @

VSE : 1 enable vertical synchro with SYNC IN
0 disable @

HSE : 1 enable horizontal synchro with SYNC IN
0 disable @

F (8:0) : scan line number per frame (@ 312)

Figure 6 : Vert Register Scan Lines Programmation

2FF1								2FF0								Nb of Scan Lines	LSB HEXA
LCD	ILC	C/H	V/P	VSE	HSE	-	F8	F7	F6	F5	F4	F3	F2	F1	F0	F(0:8) + 2	
X	X	X	X	X	X	-	0	0	0	0	0	0	0	0	0	Not allowed	-
							0	0	0	0	0	0	0	0	1	3	01
							0	0	0	0	0	1	1	1	0	16	0E
							0	0	0	1	1	1	1	1	0	64	3E
							0	0	1	1	0	0	0	1	0	100	62
							0	0	1	1	1	0	1	1	0	120	76
							0	1	1	1	0	1	1	1	0	240	EE
							0	1	1	1	1	1	0	0	0	250	F8
							1	0	0	0	0	0	1	0	0	262	04
							1	0	0	0	0	0	1	0	1	263	05
							1	0	0	1	1	0	1	0	0	310	34
							1	0	0	1	1	0	1	1	0	312	36
							1	0	0	1	1	0	1	1	1	313	37
							1	0	0	1	1	1	1	1	0	320	3E
							1	1	1	0	1	1	1	1	0	480	DE
							1	1	1	1	1	1	1	1	0	512	FE
							1	1	1	1	1	1	1	1	1	513	FF

F[8:0] = Scan Line Number - 2

9410-10.EPS

Margin and Horizontal Time Base Register (HORI)

Internal address : 2FF3-2FF2 h
RESET value :03-3F h
(@ = RESET default configuration)

2FF3	-	-	-	-	-	MG2	MG1	MG0
@	0	0	0	0	0	0	1	1
2FF2	-	-	L5	L4	L3	L2	L1	L0
@	0	0	1	1	1	1	1	1

MG(2:0) : Left and right margin duration (@ = 4µs)

$$MG = \left(\frac{\text{Margin Duration}}{8\ \text{pxlck}}\right) - 1$$

L(5:0) : Line duration (@= 64µs)

$$L = \left(\frac{\text{Line Duration}}{8\ \text{pxlck}}\right) - 1$$

Horizontal Synchronization Register (HSYN)

Internal address : 2FF5-2FF4 h
RESET value :E6-DC h
(@ = RESET default configuration)

2FF5	SU7	SU6	SU5	SU4	SU3	SU2	SU1	SU0
@	1	1	1	0	0	1	1	0
2FF4	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
@	1	1	0	1	0	1	0	0

SU(7:0) : SYNC rising edge position (@ = 57.75µs)

$$SU = \left(\frac{\text{Rise Edge Position}}{2\ \text{pxlck}}\right) - 1$$

SD(7:0) : SYNC falling edge position (@= 53.25µs)

$$SD = \left(\frac{\text{Falling Edge Position}}{2\ \text{pxlck}}\right) - 1$$

Figure 7 : HSYN Register Synchro Pulse Programmation

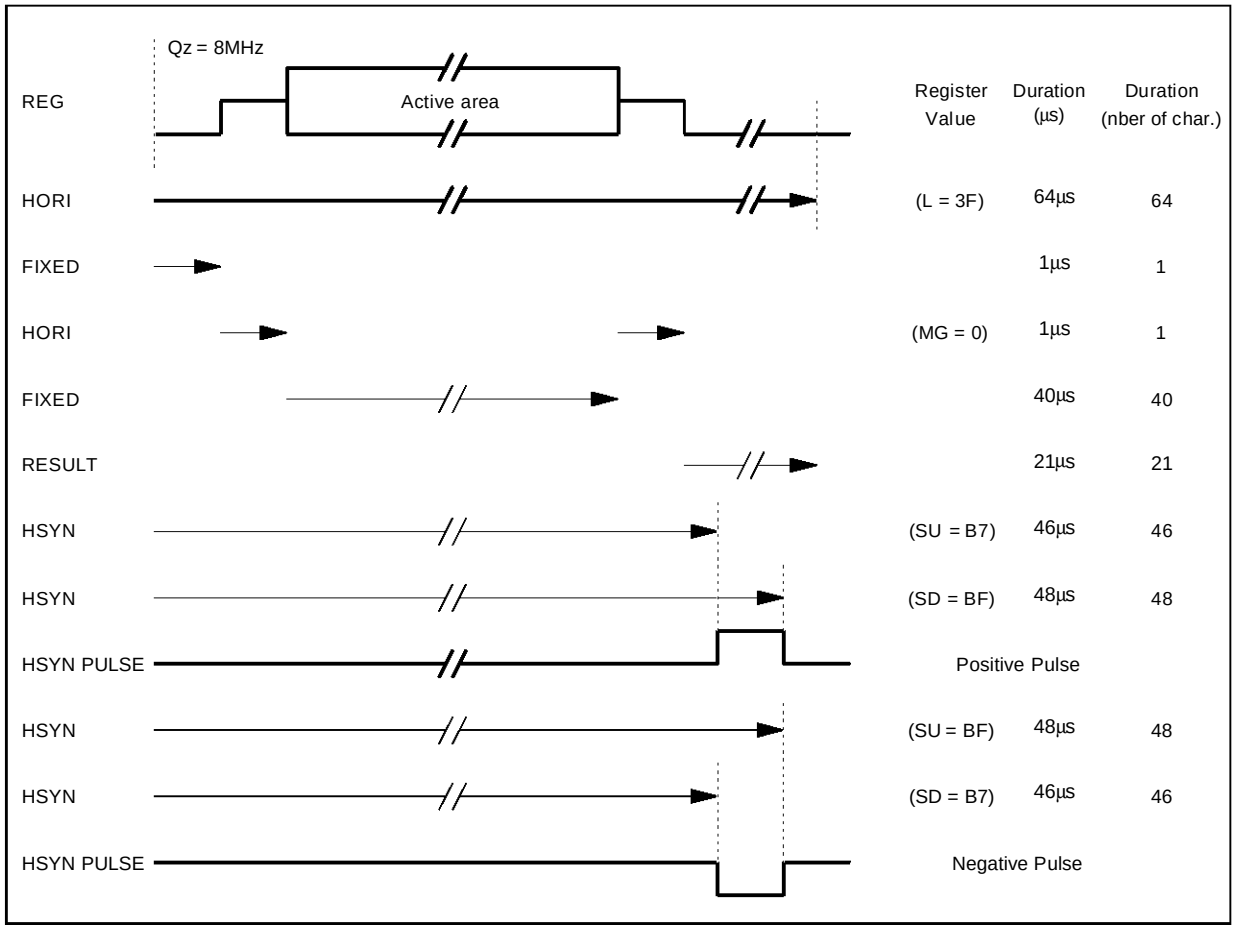
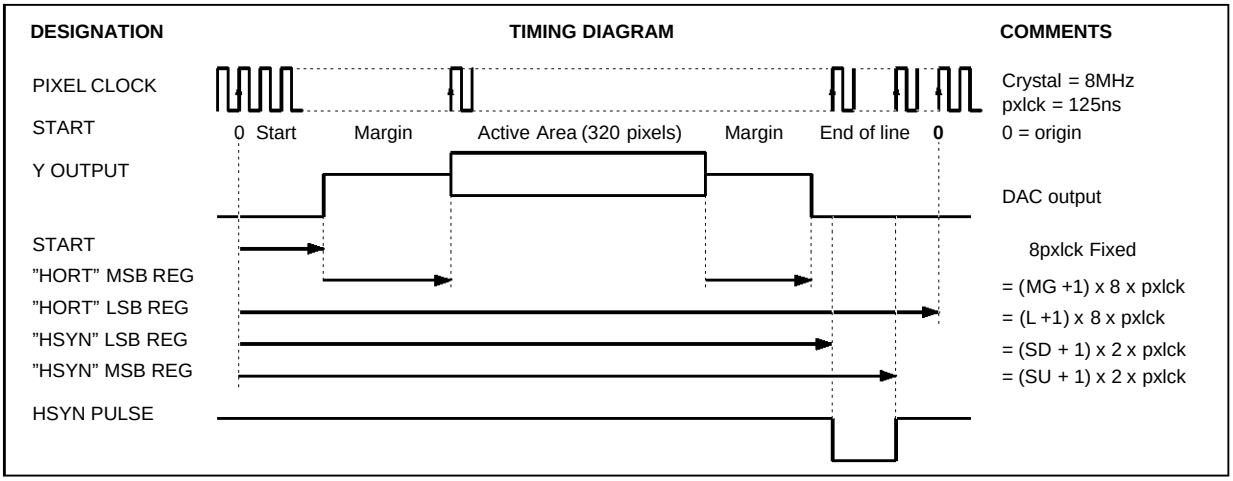


Figure 8 : Horizontal Synchronization Timing



Video Validation and Port Register (PORT)
Internal address : 2FF7-2FF6 h
RESET value :00-00 h
(@ = RESET default configuration)

2FF7	VOE	-	-	-	-	-	TE	PV
@	0	0	0	0	0	0	0	0
2FF6	N7	N6	N5	N4	N3	N2	N1	N0
@	0	0	0	0	0	0	0	0

VOE : Video Output Enable
1 enable synchro & video outputs
0 disable synchro & video outputs @
(@ Output Y, C_{SYNC}, V_{SYNC}, R, G, B, I, POR, and DF are grounded, Input SYNC IN is high impedance)

TE : Timer Enable
1 POR provides a square wave signal with a period of 16 x N(7:0) x pxlck
0 POR output is PV bit @

PV : Port Value
POR output value if TE=0 (@=0)

N(7:0) : Square wave period on POR if TE=1 (@=0)

BEWARE

The programmation of VERT, HORI, HSYN registers must be consistent. To get a proper work of the controller, the following conditions must, in any mode (CRT or LCD), be fulfiled :

- $SU \neq SD$
- $\frac{SU+1}{4} < L$ and $\frac{SD+1}{4} < L$
- $2(MG + 1) + 40 \leq L$

Line period is :

- $P_L = [L(5:0) + 1] \times 8$ pxlck
- In LCD, MG(2:0) can be 0, then minimum Line Period is $P_{L\,(min.)} = 43 \times 8$ pxlck

Frame period is :

- $P_F = [F(8:0) + 2] \times P_L$
- In LCD, using a 240 lines matrix, F(8:0) = 238, then minimum frame is :
  $P_{F\,(min.)} = 240 \times 43 \times 8$ pxclk

Pixel period is :

- $Pxclk = \frac{P_{Frame}}{[F(8:0) + 2][L(5:0) + 1] \times 8}$
- In LCD, using a 240 lines matrix, and MG(2:0) = 0, $Pxclk = \frac{P_{Frame}}{240 \times 43 \times 8}$

Interlaced mode conditions :

- $\frac{SU+1}{4}$ and $\frac{SD+1}{4} < L$
- $\frac{SU+1}{4}$ and $\frac{SD+1}{4} > (MG + 1) + 42$

2.3.2. CRT Mode

In CRT mode, the Vsync signal appears at the first two lines of the first strip of the descriptor list. It is recommended to provide an uniform blanked (with FFB bit) strip as first descriptor. The scan line number of this strip have to be equal or higher than scan line number of the vertical blanking Interval.

Master Mode

This mode is selected by writing VSE and HSE bit of VERT register with logical value "0".

Non-interlaced mode is selected by writing ILC bit of VERT register with logical value "0".

Horizontal or composite synchronization signal is output on C_{SYNC} pin, Vertical synchronization signal is output on V_{SYNC} pin.

Signal waveforms are described in Figure 9.

Interlaced mode is selected by writing ILC bit of VERT register with logical value "1".
Even frame is identical to non-interlaced frame. V_{SYNC} PULSE is low during second half of last line of previous Odd frame and during the two first lines of current Even frame.
Odd frame is one scan line more than Even frame. V_{SYNC} PULSE is low during the two first lines and up to first half of the third line of current Odd frame. Half line corresponds to 17th character position. Signals waveforms are described in Figure 10.

Slave Mode

This mode is activated by writing VSE and/or HSE bit of VERT register with logical value "1". Then SYNC IN input signal is sampled according to procedure described below.

Vertical Synchronization

SYNC IN signal may be either a vertical synchronization or a composite synchronization. It is sampled on first pixel of each scan line active area. As soon as SYNC IN signal low level is detected, vertical time base counter F(8:0) of VERT register is reset without any modification of other time base registers.

Horizontal Synchronization

SYNC IN is sampled one pxlck before and one pxlck after internal horizontal pulse transition. If falling edge is not found, one pixel period is added to internal line duration. Using a line frequency locked clock applied on XTI, internal scan line becomes phase locked after few scan line periods at programmed value (see Figure 11).

2.3.3 LCD Mode

LCD mode only works as a master mode with 320 pixels per line. Internal algorithm allows 8 grey levels on passive LCD matrix. Number of scan line is programmable. In order to get maximum refresh frequency of display, margin and line duration must be reduced to miminum. Interlaced mode and external synchronization are not allowed. The 1st line of the first descriptor in the description list correspond to the first line of the LCD display. Y output provides a programmable voltage usable to adjust contrast of LCD display. To reduce supply current consumption, when Y output is unused, V_{SSA} must not be connected to ground, and V_{REF} pin works as a reset pin. Notice that SYNC IN Pin provides (CKD) data clock signal.

2.4 POR OUTPUT

POR is a standard I/O pin programmable at logical level "1" or "0". It can also provide a programmable square wave signal of period
P = 16 x N(7:0) x pxlck ($0 \leq N \leq 255$).

It can drive a capacitive buzzer (see application diagram at page 22).

RESET value of PORT is "0".

Figure 9 : ODD and EVEN Synchronization Pulses in Non-interlaced Mode

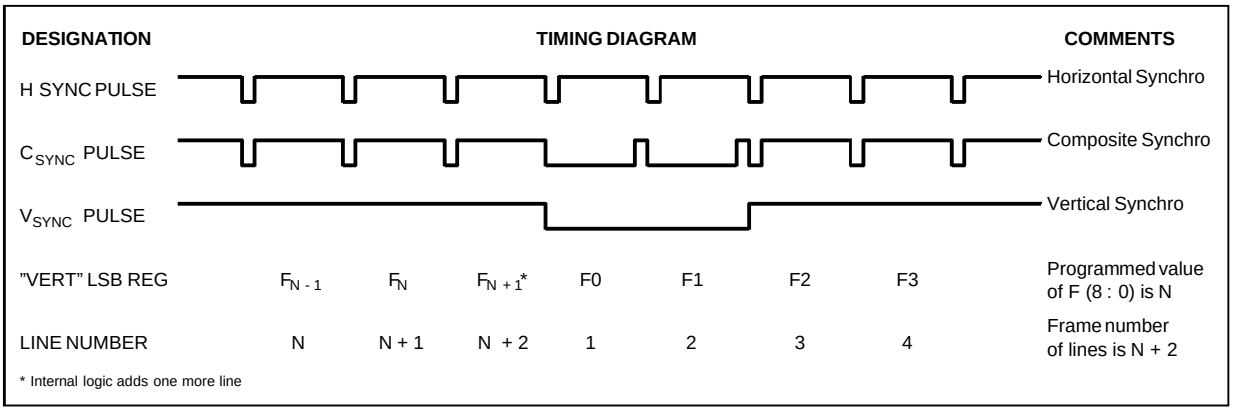


Figure 10 : Interlaced Mode Synchronization Pulses

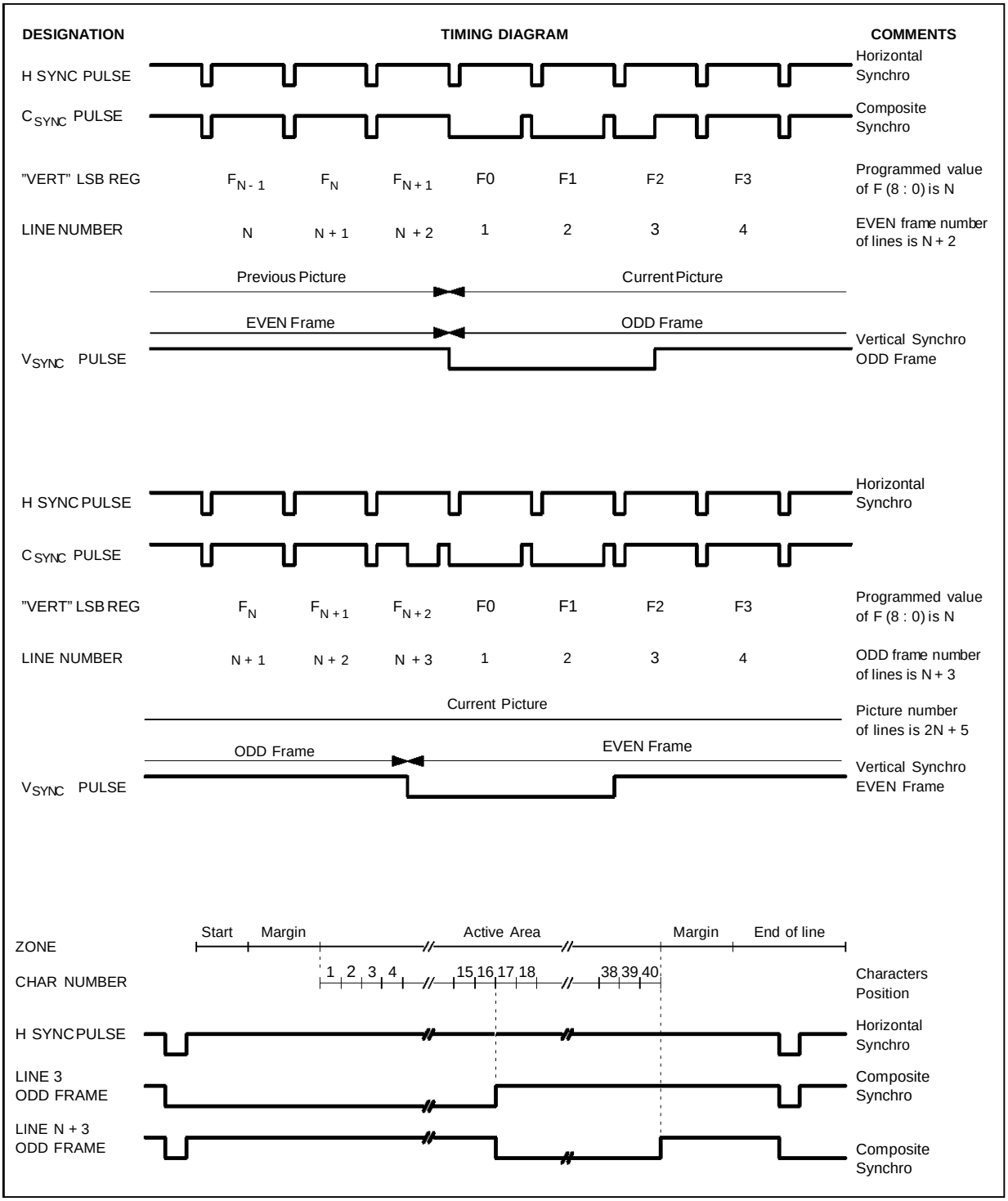
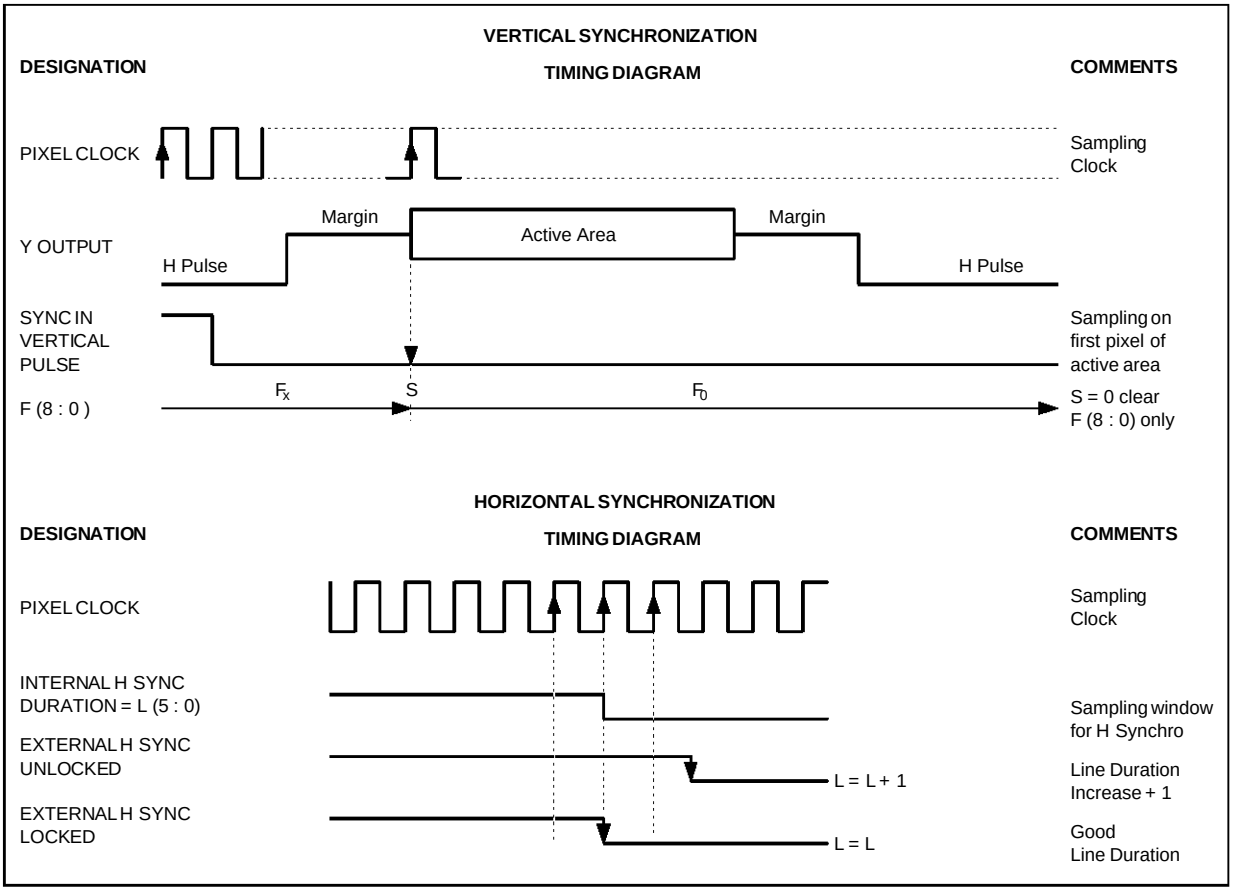


Figure 11 : Synchronization on SYNC IN External Signal



3. INTERNAL REGISTER DESCRIPTION

STV9410 is programmable with 7 registers of 16 bit each. These registers can also be programmed in byte mode. Not significant bit must be cleared in order to be compatible with next generation products.

3.1 TIME BASE REGISTERS

Registers VERT, HORI, HSYN and PORT are described in chapter 2.3

3.2 ADDRESS REGISTER (ADDR)

Internal address : 2FF9-2FF8 h

RESET value :00-00 h
(@ = RESET default configuration)

2FF9 h	-	P12	P11	P10	P9	P8	P7	P6
@	0	0	0	0	0	0	0	0

2FF8 h	-	G12	G11	G10	-	A12	A11	A10
@	0	0	0	0	0	0	0	0

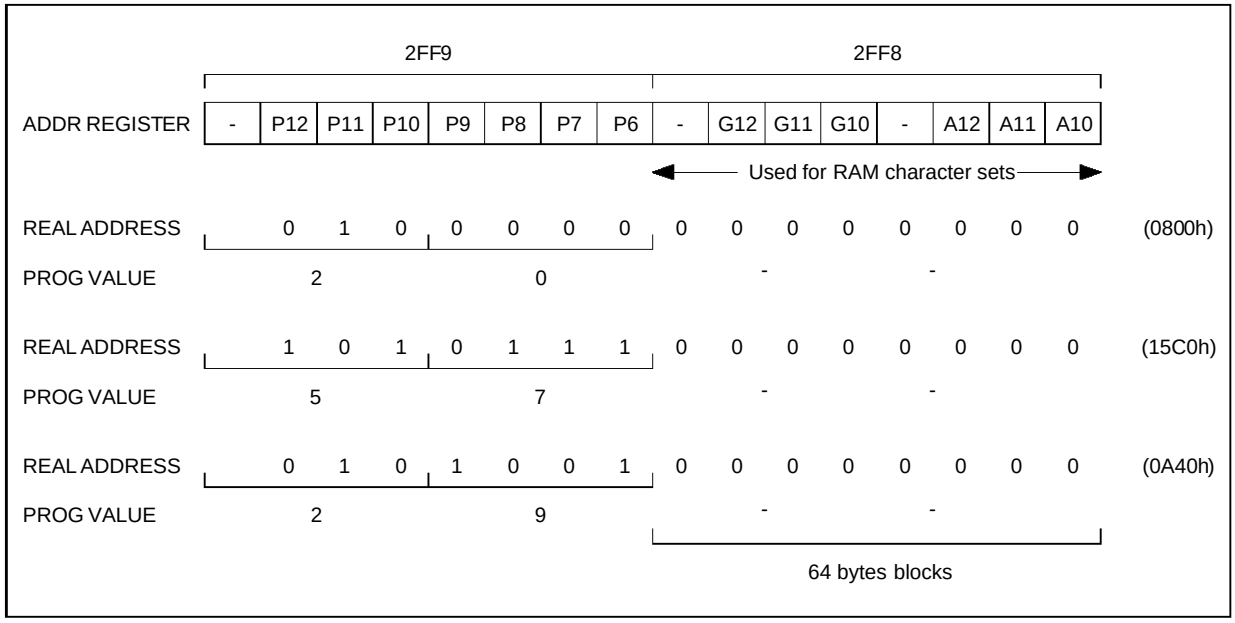
P(12:6) : Page first descriptor address, P(5:0)=0 @

G(12:10) : Graphic character set MSB address, G(9:0)=0 @

A(12:10) : Alphanumeric character set MSB address, A(9:0)=0 @

NB : as addresses are in RAM area, address bit 13 is reset to ”0”

Figure 12 : ADDR Register and Descriptor List Address



3.3 DISPLAY REGISTER (DISP)

Internal address : 2FFB-2FFAh

RESET value :00-00 h
(@ = RESET default configuration)

2FFB	IMG	GMG	RMG	BMG	-	-	-	HIC
@	0	0	0	0	0	0	0	0

2FFA	FLE	CCE	IN1	IN0	BR3	BR2	BR1	BR0
@	0	0	0	0	0	0	0	0

IMG, GMG, RMG, BMG : Margin value of I,G,R,B outputs and background color and insertion default attribute of next alphanumeric character. In case of graphic characters only I is default attribute.

HIC : Forces alphanumeric characters background black (R, G, B = 0), and foreground white (R, G, B = 1) for maximum contrast, 0 = disable @

FLE : Flashing enable, 0 = disable @

CCE : Conceal enable, 0 = disable @

IN1,IN0 : Insertion attribute mode selection. Mode selects value of I output during active area of scan line in CRT mode; I output value (during margin) is programmed with DISP register; during uniform strip I output value is set according to strip descriptor.
During active time slot :

- 0 0 : I output gets value of current code I attribute (margin attribute or control character attribute) @
- 0 1 : I is set (”1”)
- 1 0 : I output gets value of current code I attribute if I=0 R,G,B are reset to ”0”
- 0 1 : Reserved mode

BR(3:0) : This value is combined with pixel value to drive Y DAC in CRT mode :
Y= 4xG + 2xR + B + BR(2:0) + 3x(R or G or B) (logical or)
R, G, B, I, Y, = 0 during line flyback.

Black level is output with R, G, B = ”0”.
White level is output with R, G, B = ”1”.

During frame flyback, R, G, B, I, Y provides signal according to uniform strip descriptor FFB bit state (see chapter 4.2.1)
During LCD mode BR(3:0) drives continuously Y DAC. Notice that only bit 0 to 2 of BR are used in CRT mode.

3.4. CURSOR REGISTER (CURS)

Internal address : 2FFD-2FFC h

RESET value : 00-00 h
(@= RESET default configuration)

2FFD	CEN	CBL	CUL	-	C12	C11	C10	C9
@	0	0	0	0	0	0	0	0

2FFC	C8	C7	C6	C5	C4	C3	C2	C1
@	0	0	0	0	0	0	0	0

CEN : Cursor enable, 0 = disable @

CBL : 0 cursor blinking off, character blinking attribute unchanged @
1 cursor blinking on, blinking is mixed with character blinking attribute. Blinking frequency is around 1Hz and duty cycle 50%

CUL : 0 character underline attribut is complemented on cursor position @
1 character color is complemented on cursor position

C(12:1) : Cursor address (not a screen position)

4. DISPLAY CONTROL

4.1 SCREEN DESCRIPTION

A screen is composed of successive scan lines gathered in one or several strips. Each strip is defined by a descriptor stored in memory. A list of descriptors allows screen composition, different screens can be defined in memory (see application note and Figures 13, 14.).

Two kinds of strip are available :

- **Uniform color strip**

  Applications :
  - vertical front and back porch
  - vertical synchro
  - border lines

  Parameters :
  - number of scan lines
  - color

- **Character strip**

  Characters and attributes are defined by a succession of codes stored in memory; thanks to the character code, a memory address is calculated and used to get the character pattern.

  Parameters :
  - address of the first code
  - size, display enable

Figure 13 : Programmation of Number of Scan Lines - Vertical Register VERT (2FF0/2FF1) and Descriptor List

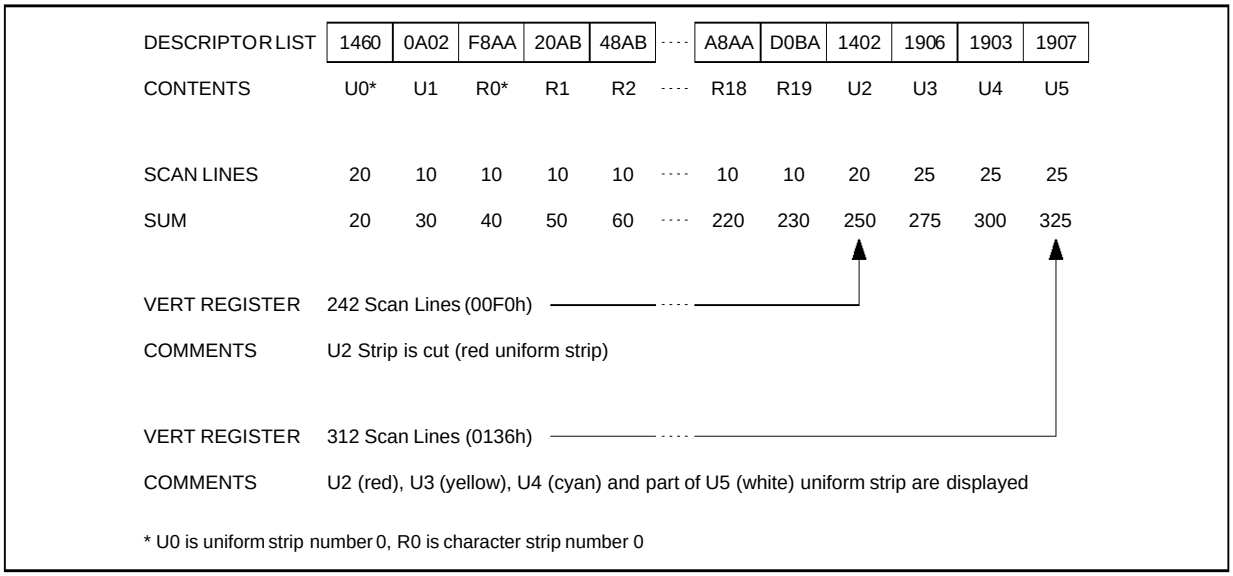
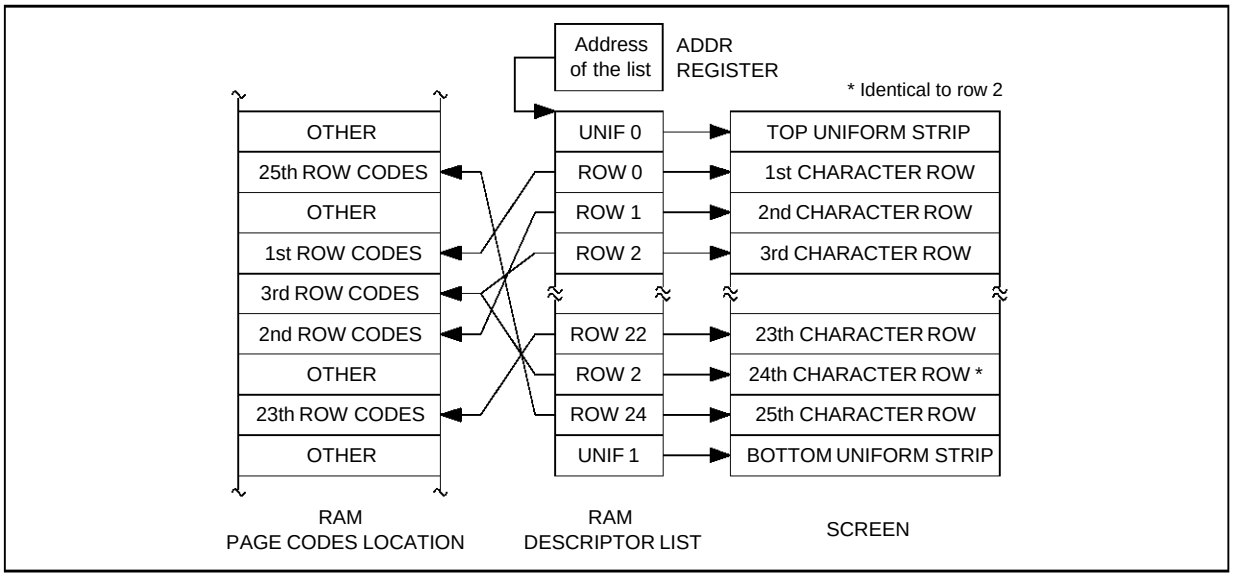


Figure 14 : Relation between Screen Location/Descriptor Pointer/RAM Page Codes



4.2. STRIP DESCRIPTOR

Each strip is defined by 2 bytes.
During the vertical retrace, an internal descriptor address counter is initialised with the value P(12:0) of ADDR register; on the trailing edge of vertical synchro, the first strip descriptor is loaded into the display controller; if it is an uniform strip, selected color is displayed during the corresponding number of scan lines; if it is a character strip, left margin followed by text, followed by right margin are displayed during 10 scan lines ; the next descriptor is then read, and the same process is repeated until the last scan line. This information being given by the vertical timing generator.

4.2.1 Uniform Strip

0	RTP	FFB	-	I	C2	C1	C0
SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0

RTP : Real Time Port
RTP bit value is output on V_{SYNC} when V/P bit of VERT register is "0", along the complete duration of the strip scan line. Not used in LCD mode.

FFB : Field Flyback
0 R, G, B, I and Y outputs are defined by corresponding bit of DISP for margin and C(2:0) and I for active area
1 R, G, B, I and Y outputs are cleared during Field Flyback, whatever other parameters are.

I : 0 Fast Blanking Disable
1 Fast Blanking Enable

C(2:0) : G, R, B, value during the active area of the strip (320 pixels)

SL(7:0) : Number of scan lines of the strip, minimal value is 1.

4.2.2. Character Strip

1	RTP	DE	ZY	C12	C11	C10	C9
C8	C7	C6	C5	C4	C3	C2	C1

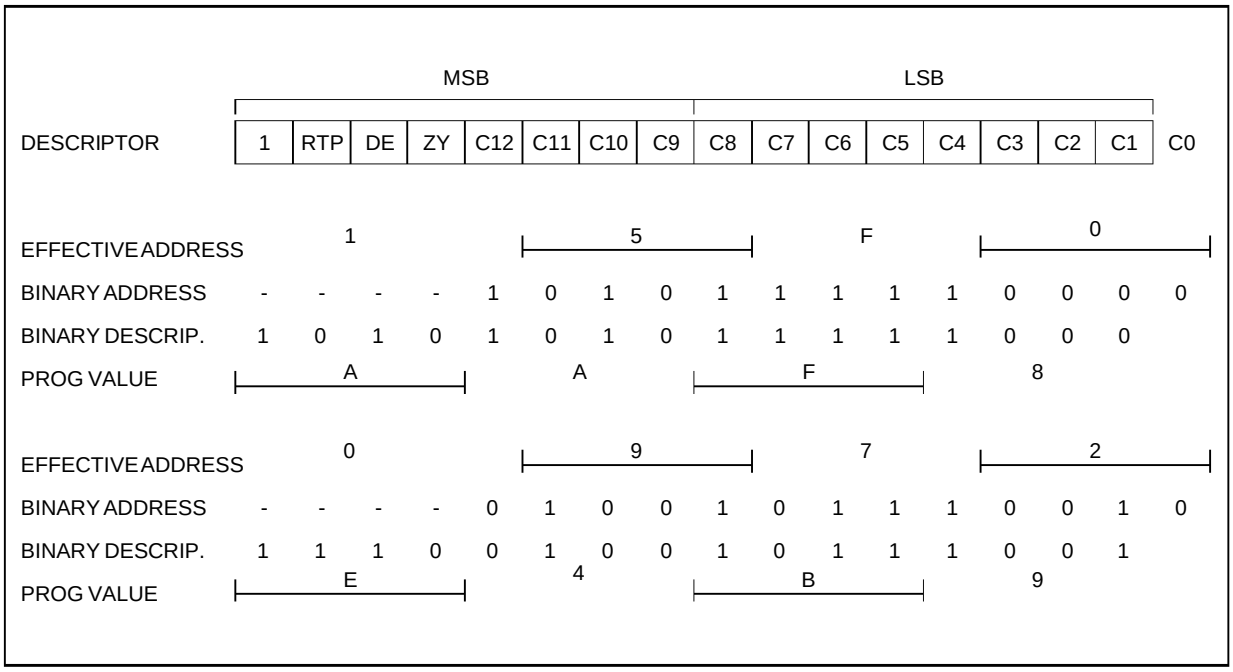
RTP : Real Time Port
RTP bit value is output on V_{SYNC} when V/P bit of VERT register "0", along the complete duration of the strip line, during the whole strip.

DE : Display Enable
0 display off, the strip is displayed with margin attributes IMG, GMG, RMG, BMG bit of DISP register,
1 display on, the strip works as selected.

ZY : Vertical Zoom
0 normal display mode
1 all scan line are doubled, providing a vertical zoom effect

C(12:1) : Address of the first code to display

Figure 15 : Character Strip Descriptor - First Character Address Selection



5. CHARACTER CODE FORMAT

Each character is defined with a two bytes code; the first is at an even address, the second is at the following odd address. Some attributes are parallel, other keep the last explicit value.
STV9410 uses 3 different types of codes.

5.1 ALPHANUMERIC CHARACTERS
(256 patterns)

The background color is not defined by the code; it takes the same value as the previous character or it has the value of the margin color at the beginning of each row.
The character pattern lies in ROM if CHARACTER NUMBER is lower than 80h, (ALPHANUMERIC CHARACTER SET is shown in TABLE 3),else it is User Defined Character in RAM (DRCS).

ODD	CHARACTER NUMBER							
EVEN	0	IV	DW	DH	FL	FC2	FC1	FC0

CHARACTER NUMBER : ROM or RAM character set code
IV : Inverted video if set.
DW : Double character width if set, code must be repeated for the right part of the character.
DH : Double character height if set, code must be repeated for the bottom part of the character. The first DH attribute encountered in a vertical column is always interpreted as a top part.
FL : Flashing, inverted phase if IV is set.
FC(2:0) : Foreground color (Green, Red, Blue).

5.2. GRAPHIC CHARACTERS (224 patterns)

IV, DW, DH, UL take the value ”0”
CHARACTER NUMBER must be lower than E0h.
The character pattern lies in ROM if CHARACTER NUMBER is lower than 80h, (STANDARD MOSAIC character set is shown in Table 4), else it is an User Defined Character in RAM (DRCS).

ODD	CHARACTER NUMBER							
EVEN	1	BC2	BC1	BC0	FL	FC2	FC1	FC0

CHARACTER NUMBER : ROM or RAM character set code
BC(2:0) : Background color (Green, Red, Blue).
FL : Flashing.
FC(2:0) : Foreground color (Green, Red, Blue).

5.3. CONTROL CHARACTERS (32 codes)

These characters are displayed as foreground color spaces if HG bit is clear. They can change some attributes applying to themselves and to the following string.

ODD	1	1	1	EOL	IF	IB	UL	CC
EVEN	1	BC2	BC1	BC0	HG	FC2	FC1	FC0

EOL : End Of Line
0 normal control code
1 space are displayed until the end of the row, allowing memory space saving
IF,IB : Insert foreground, Insert background attribute.
0 fast blanking disable
1 fast blanking enable
UL : Underlined
0 disable
1 enable
CC : Conceal Character
0 disable
1 enable, character is diplayed as a space.
BC(2:0) : Default background color of next character(s)
HG : Hold Graphics
0 disable, the control character is displayed as a uniform space character with foreground color fixed by FC(2:0)
1 enable, the control character pattern takes the last mosaic value encountered in the row, if any, or is a space.
FC(2:0) : G, R, B foreground value of the control character

At the beginning of each row, those attributes take default values :
- EOL, UL, CC, HG = 0
- IF = 1
- IB = IMG (Margin insert attribute)
- BC(2:0) = GMG, RMG, BMG (Margin color).

Notice that following characters code is reserved for futur use.

ODD	1	1	1	1	X	X	X	1
EVEN	1	X	X	X	X	X	X	X

6. CHARACTER GENERATORS

Each pixel is defined with one bit, 1 refers to foreground color, and 0 to background color.

PX7	PX6	PX5	PX4	PX3	PX2	PX1	PX0

PX7 is the leftmost pixel.
Character slice address :
Each character generator contains a succession of patterns arranged as a number of horizontal slices :
- Slice addr = (Set addr) + Char Number x 10 + (slice number)
- Char Number is the number of the character in the set; using DRCS in RAM, the calling code of the character is the number of the character in the set plus 80h.
- Set addr is defined in ADDR register, in RAM for DRCS (see section 3.2), and is 2000h for ALPHANUMERIC ROM, and 2800h for STANDARD MOSAIC ROM.

Table 3 : Go Alphanumeric Character Set 40 Character/Row STV9410

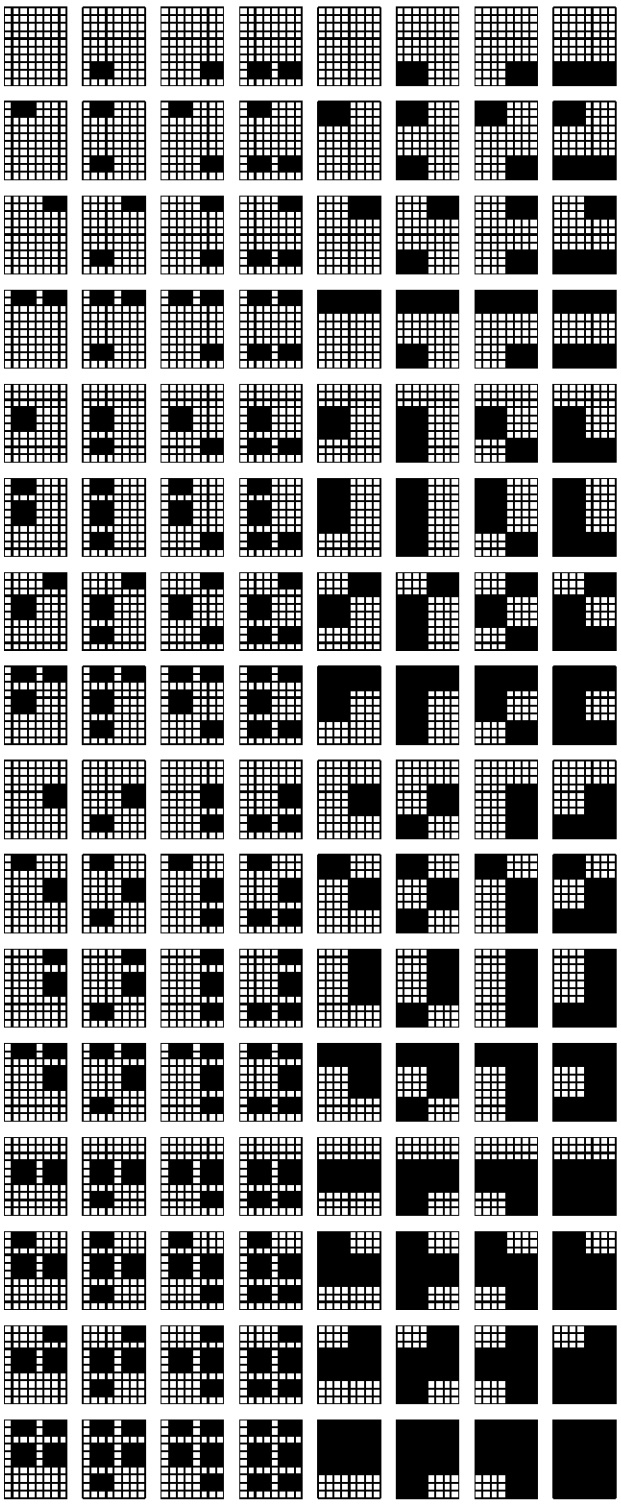
C3	C2	C1	C0	C6=0 C5=0 C4=0	C6=0 C5=0 C4=1	C6=0 C5=1 C4=0	C6=0 C5=1 C4=1	C6=1 C5=0 C4=0	C6=1 C5=0 C4=1	C6=1 C5=1 C4=0	C6=1 C5=1 C4=1
0	0	0	0								
0	0	0	1								
0	0	1	0								
0	0	1	1								
0	1	0	0								
0	1	0	1								
0	1	1	0								
0	1	1	1								
1	0	0	0								
1	0	0	1								
1	0	1	0								
1	0	1	1								
1	1	0	0								
1	1	0	1								
1	1	1	0								
1	1	1	1								

9410-20.EPS

Table 4 : G_1 Semigraphic Character Set

		SEPARATED SEMI-GRAPHIC				MOSAIC SEMI-GRAPHIC			
C6	0	0	0	0	1	1	1	1
C5	0	0	1	1	0	0	1	1
C4	0	1	0	1	0	1	0	1

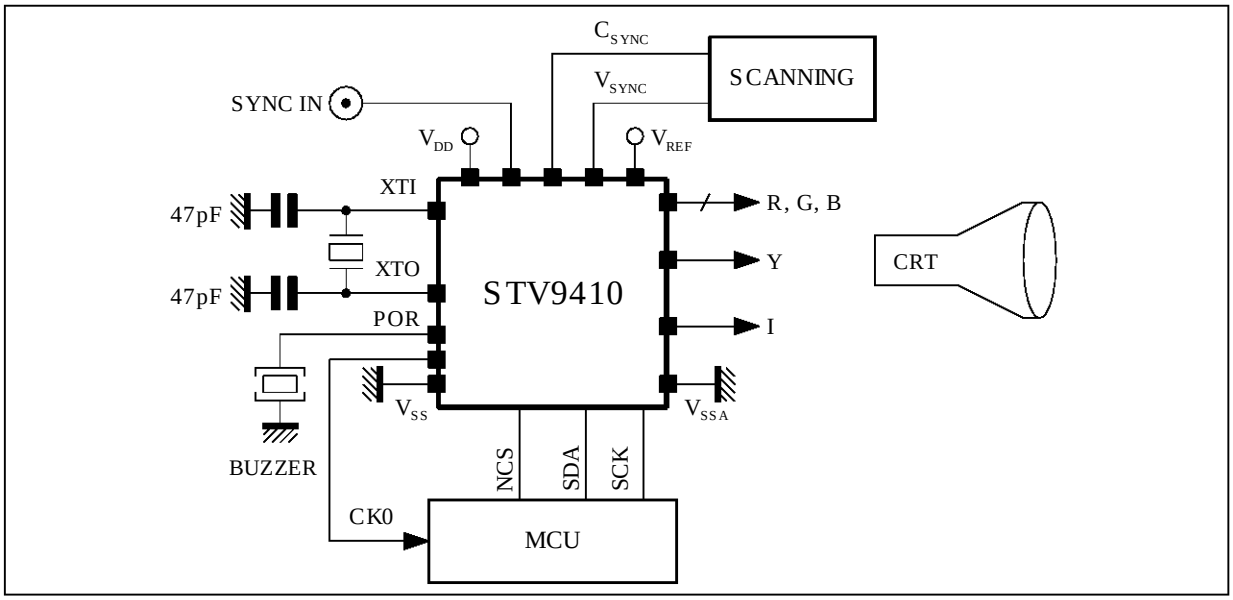
C3	C2	C1	C0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1



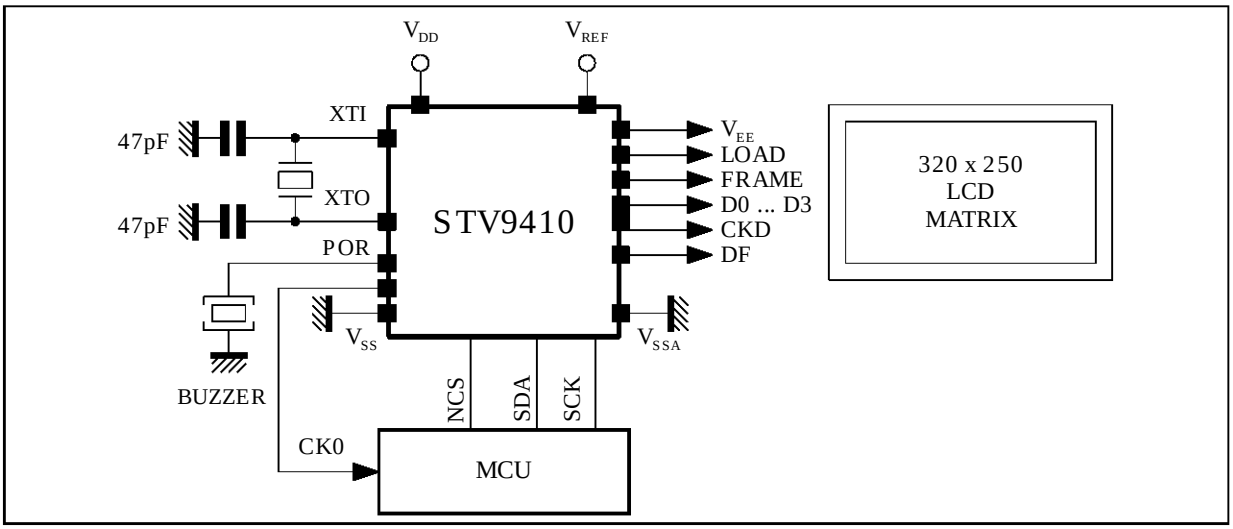
9410-21.EPS

TYPICAL APPLICATIONS

CRT APPLICATION DIAGRAM

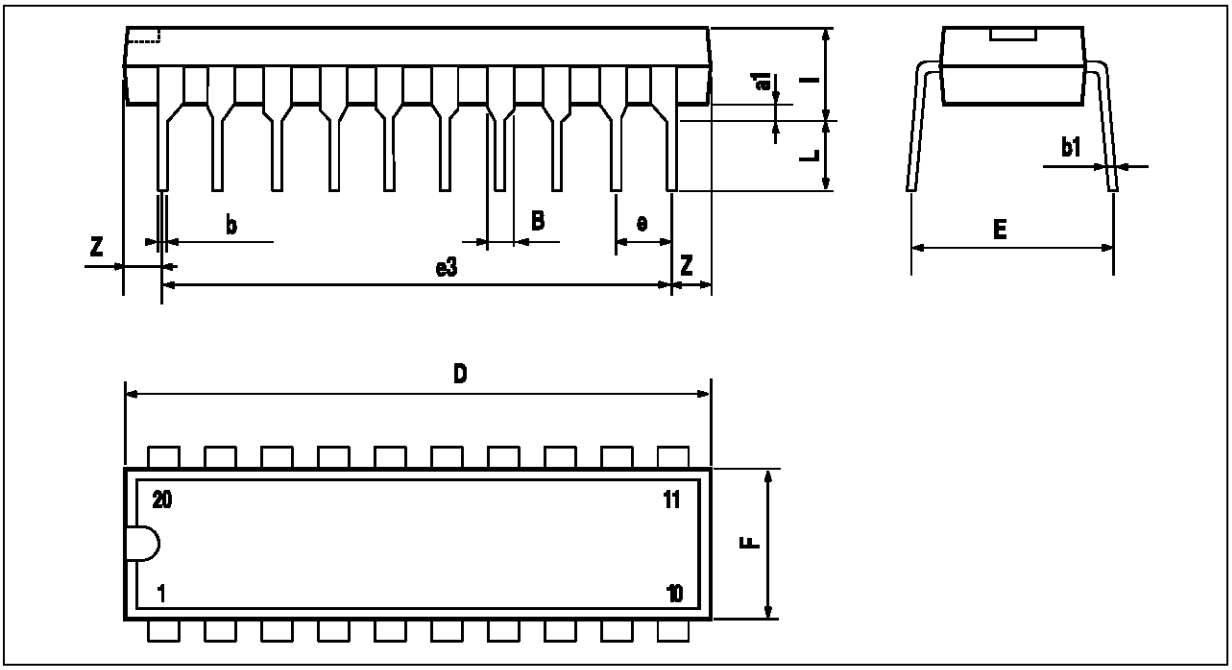


LCD APPLICATION DIAGRAM



PACKAGE MECHANICAL DATA

20 PINS - PLASTIC DIP



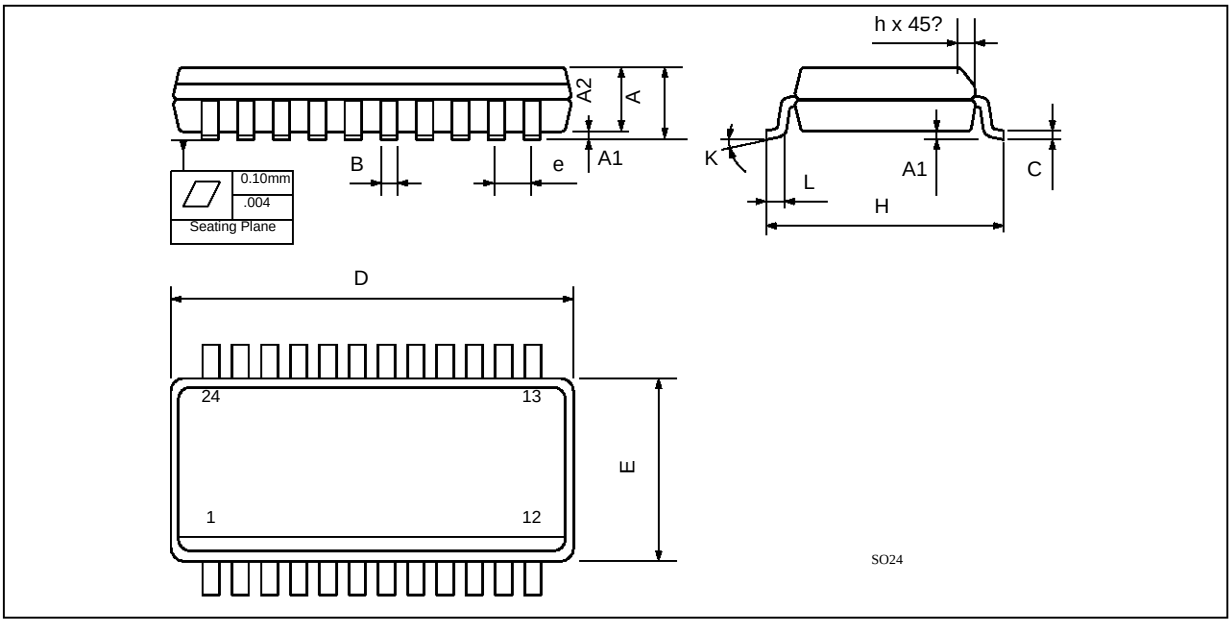
PM-DIP20.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053

DIP20.TBL

PACKAGE MECHANICAL DATA

24 PINS - PLASTIC MICROPACKAGE



PM-SO24.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.35		2.65	0.093		0.104
A1	0.1		0.30	0.004		0.012
A2			2.55			0.100
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	15.20		15.60	0.598		0614
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
K	0^o (Min.), 8^o (Max.)					
L	0.40		1.27	0.016		0.050

SO24.TBL