



# SY2128

## 2048 x 8 Static Random Access Memory

MEMORIES

### Features

- 100 nsec Maximum Access Time
- Fully Static Operation:  
No Clocks or Strokes Required
- Automatic  $\overline{CE}$  Power Down
- Identical Cycle and Access Times
- Single +5V Supply ( $\pm 10\%$ )
- Pin Compatible with 16K ROMs, EPROMs, and EEPROMs
- Totally TTL Compatible:  
All Inputs and Outputs
- Common Data Input and Output
- Three-State Output
- JEDEC Approved Pinout

### Description

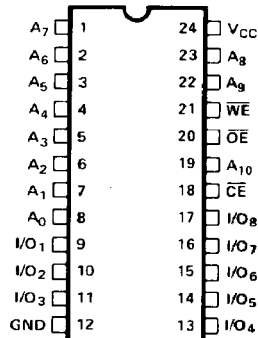
The Synertek SY2128 is a 16,384 bit static Random Access Memory organized 2048 words by eight bits and is fabricated using Synertek's new scaled n-channel silicon gate technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. The common data input and three-state output pins optimize compatibility with systems utilizing a bidirectional data bus.

The SY2128 offers an automatic power down feature under the control of the chip enable ( $\overline{CE}$ ) input. When  $\overline{CE}$  goes high, deselecting the

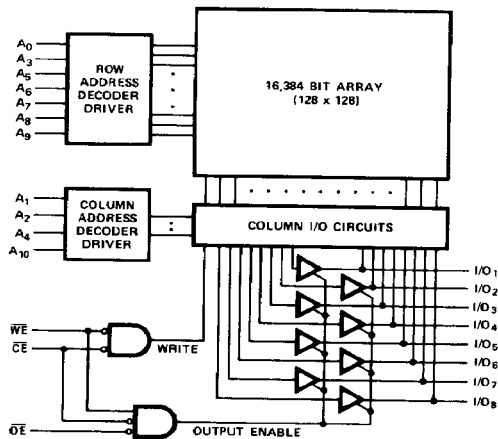
chip, the device will automatically power down and remain in a standby power mode as long as  $\overline{CE}$  remains high. This feature provides significant system level power savings.

The SY2128 is configured in the JEDEC approved pinout for 24 pin byte organized memories and is pin compatible with 16K ROMs, EPROMs and EEPROMs. This offers the user the flexibility of being able to switch between RAM, ROM, EPROM, or EEPROM as his needs dictate with a minimum of board changes.

### Pin Configuration



### Block Diagram



**Absolute Maximum Ratings\***

Temperature Under Bias	-10°C to 85°C
Storage Temperature	65°C to 150°C
Voltage on Any Pin with Respect to Ground	-3.5V to +7V
Power Dissipation	1.0W
Electrostatic Discharge Rating (ESD)**	
Inputs to Ground	±2000V

**Comment\***

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

\*\*Test Condition: MIL-STD-883B Method 3015.1

**D.C. Characteristics**  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 10\%$  (Unless otherwise specified)

Symbol	Parameter	2128-1/-2/-3/-4		2128L-1/L-2/L-3/L-4		Unit	Conditions
		Min.	Max.	Min.	Max.		
I <sub>LI</sub>	Input Load Current (All input pins)		10		10	μA	V <sub>CC</sub> = Max, V <sub>IN</sub> = Gnd to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10		10	μA	C <sub>E</sub> = V <sub>IH</sub> , V <sub>CC</sub> = Max V <sub>OUT</sub> = Gnd to 4.5V
I <sub>CC</sub>	Power Supply Current		95		75	mA	T <sub>A</sub> = 25°C, V <sub>CC</sub> = Max, C <sub>E</sub> = V <sub>IL</sub>
			100		80	mA	T <sub>A</sub> = 0°C, Outputs Open
I <sub>SB</sub>	Standby Current		20		15	mA	V <sub>CC</sub> = Min to Max, C <sub>E</sub> = V <sub>IH</sub>
I <sub>PO</sub>	Peak Power-on Current (Note 6)		40		30	mA	V <sub>CC</sub> = Gnd to V <sub>CC</sub> Min C <sub>E</sub> = Lower of V <sub>CC</sub> or V <sub>IH</sub> Min.
V <sub>IL</sub>	Input Low Voltage	-3.0	0.8	-3.0	0.8	V	
V <sub>IH</sub>	Input High Voltage	2.0	6.0	2.0	6.0	V	
V <sub>OL</sub>	Output Low Voltage		0.4		0.4	V	I <sub>OL</sub> = 3.2mA
V <sub>OH</sub>	Output High Voltage	2.4		2.4		V	I <sub>OH</sub> = -1.0mA

**Capacitance**  $T_A = 25^\circ\text{C}$ , f = 1.0 MHz

Symbol	Test	Typ.	Max.	Unit
C <sub>OUT</sub>	Output Capacitance		5	pF
C <sub>IN</sub>	Input Capacitance		5	pF

NOTE: This parameter is periodically sampled and not 100% tested.

**A.C. Characteristics**  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 10\%$  (Note 7)

**READ CYCLE**

Symbol	Parameter	2128-1/L-1		2128-2/L-2		2128-3/L-3		2128-4/L-4		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>RC</sub>	Read Cycle Time	100		120		150		200		ns	
t <sub>AA</sub>	Address Access Time		100		120		150		200	ns	
t <sub>ACE</sub>	Chip Enable Access Time		100		120		150		200	ns	
t <sub>AOE</sub>	Output Enable Access Time		35		50		60		70	ns	
t <sub>OH</sub>	Output Hold from Address Change	10		10		10		10		ns	
t <sub>LZ</sub>	Output Low Z Time	10		10		10		10		ns	Note 5
t <sub>HZ</sub>	Output High Z Time	0	35	0	40	0	50	0	60	ns	Note 5
t <sub>PU</sub>	Chip Enable to Power Up Time	0		0		0		0		ns	
t <sub>PD</sub>	Chip Disable to Power Down Time		50		60		80		100	ns	

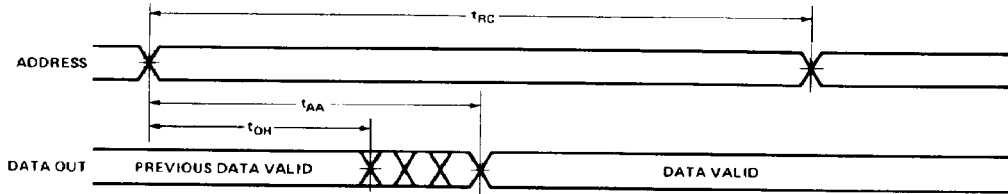
**WRITE CYCLE**

t <sub>WC</sub>	Write Cycle Time	100		120		150		200		ns	
t <sub>CW</sub>	Chip Enable to End of Write	80		90		120		150		ns	
t <sub>AW</sub>	Address Valid to End of Write	80		90		120		150		ns	
t <sub>AS</sub>	Address Setup Time	0		0		0		0		ns	
t <sub>WP</sub>	Write Pulse Width	60		70		90		120		ns	
t <sub>WR</sub>	Write Recovery Time	0		0		0		0		ns	
t <sub>DW</sub>	Data Valid to End of Write	40		50		70		90		ns	
t <sub>DH</sub>	Data Hold Time	0		0		0		0		ns	
t <sub>WZ</sub>	Write Enabled to Output in High Z	0	35	0	40	0	50	0	60	ns	Note 5
t <sub>OW</sub>	Output Active from End of Write	0		0		0		0		ns	Note 5

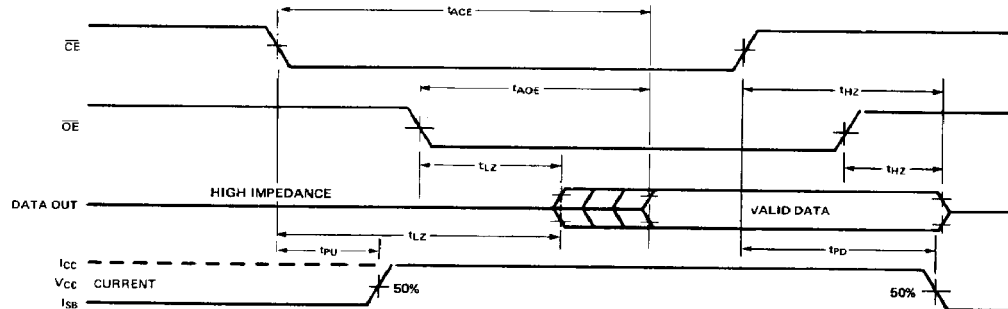
(See following page for notes)

Timing Diagrams

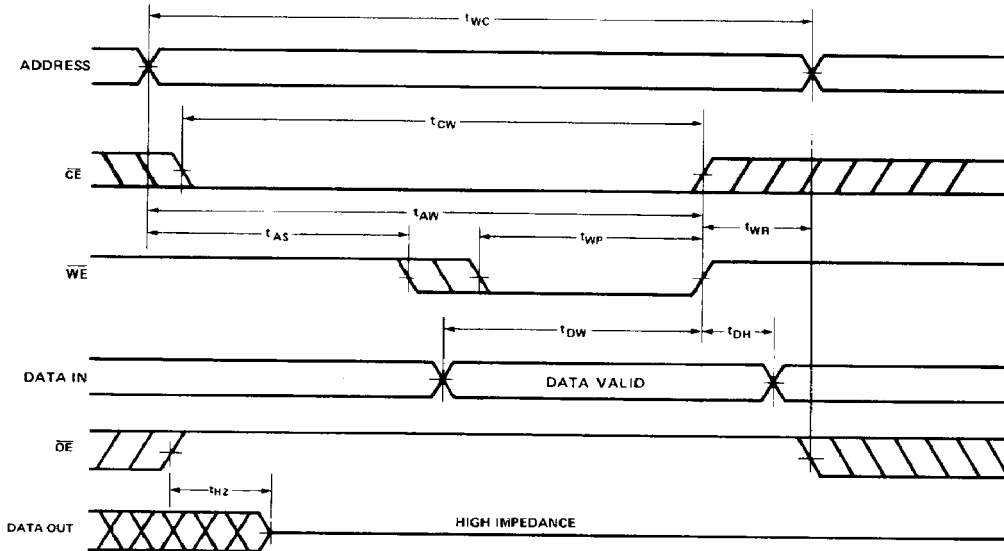
READ CYCLE NO. 1 (NOTES 1 and 2)



READ CYCLE NO. 2 (NOTES 1 and 3)



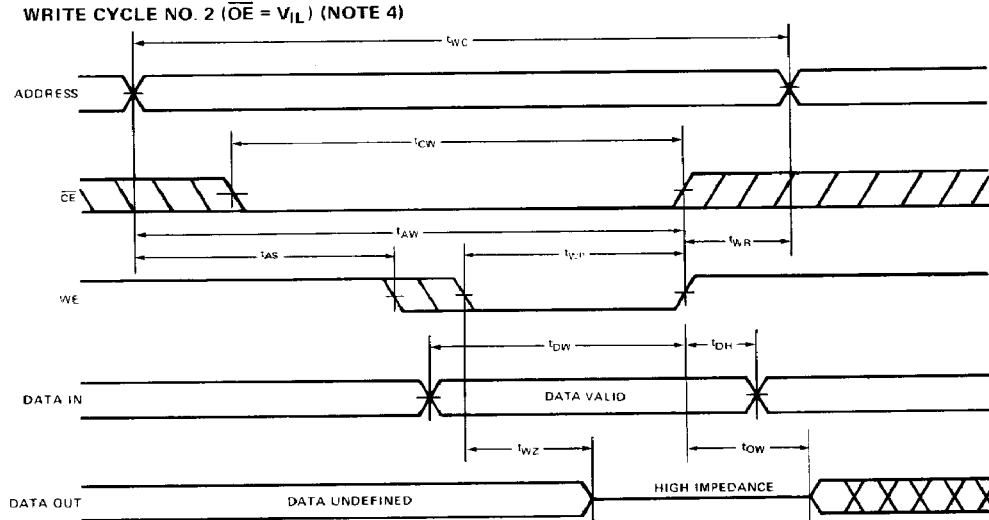
WRITE CYCLE NO. 1 (NOTE 4)



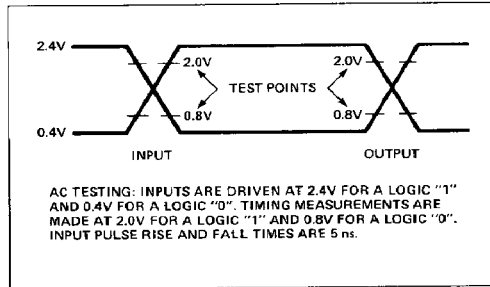
Notes:

1.  $\overline{WE}$  is high for Read Cycles.
2. Device is continuously selected,  $\overline{CE} = \overline{OE} = V_{IL}$ .
3. Addresses valid prior to or coincident with  $\overline{CE}$  transition low.
4. If  $\overline{CE}$  goes high simultaneously with  $\overline{WE}$  high, the outputs remain in the high impedance state.
5. Transition is measured  $\pm 500\text{mV}$  from low or high impedance voltage with load B. This parameter is sampled and not 100% tested.
6. A pullup resistor to  $V_{CC}$  on the  $\overline{CE}$  input is required to keep the device deselected; otherwise, power-on current approaches  $I_{CC}$  active.
7. A minimum 0.5 ms time delay is required after application of  $V_{CC}$  (+5V) before proper operation is achieved.

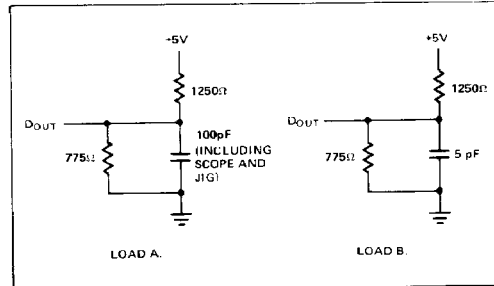
MEMORIES



**A.C. Testing Input, Output Waveform**



**A.C. Testing Load Circuit**



**Package Availability** 24 Pin Cerdip  
24 Pin Plastic

**Ordering Information**

Order Number	Access Time (Max)	Operating Current (Max)	Standby Current (Max)	Package Type
SYD2128-1	100ns	100mA	20mA	Cerdip
SYP2128-1	100ns	100mA	20mA	Plastic
SYD2128-2	120ns	100mA	20mA	Cerdip
SYP2128-2	120ns	100mA	20mA	Plastic
SYD2128-3	150ns	100mA	20mA	Cerdip
SYP2128-3	150ns	100mA	20mA	Plastic
SYD2128-4	200ns	100mA	20mA	Cerdip
SYP2128-4	200ns	100mA	20mA	Plastic
SYD2128L-1	100ns	80mA	15mA	Cerdip
SYP2128L-1	100ns	80mA	15mA	Plastic
SYD2128L-2	120ns	80mA	15mA	Cerdip
SYP2128L-2	120ns	80mA	15mA	Plastic
SYD2128L-3	150ns	80mA	15mA	Cerdip
SYP2128L-3	150ns	80mA	15mA	Plastic
SYD2128L-4	200ns	80mA	15mA	Cerdip
SYP2128L-4	200ns	80mA	15mA	Plastic