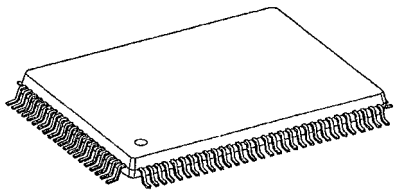
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T6B23

COLUMN DRIVER LSI FOR A DOT MATRIX LCD

The T6B23 is a column driver with 80 output channels for a dot matrix LCD.
The T6B23 realizes low power consumption using the CMOS Si-Gate process. The T6B23 has two types of data flow:
(1) $O_1 \rightarrow O_{80}$, (2) $O_{80} \rightarrow O_1$.



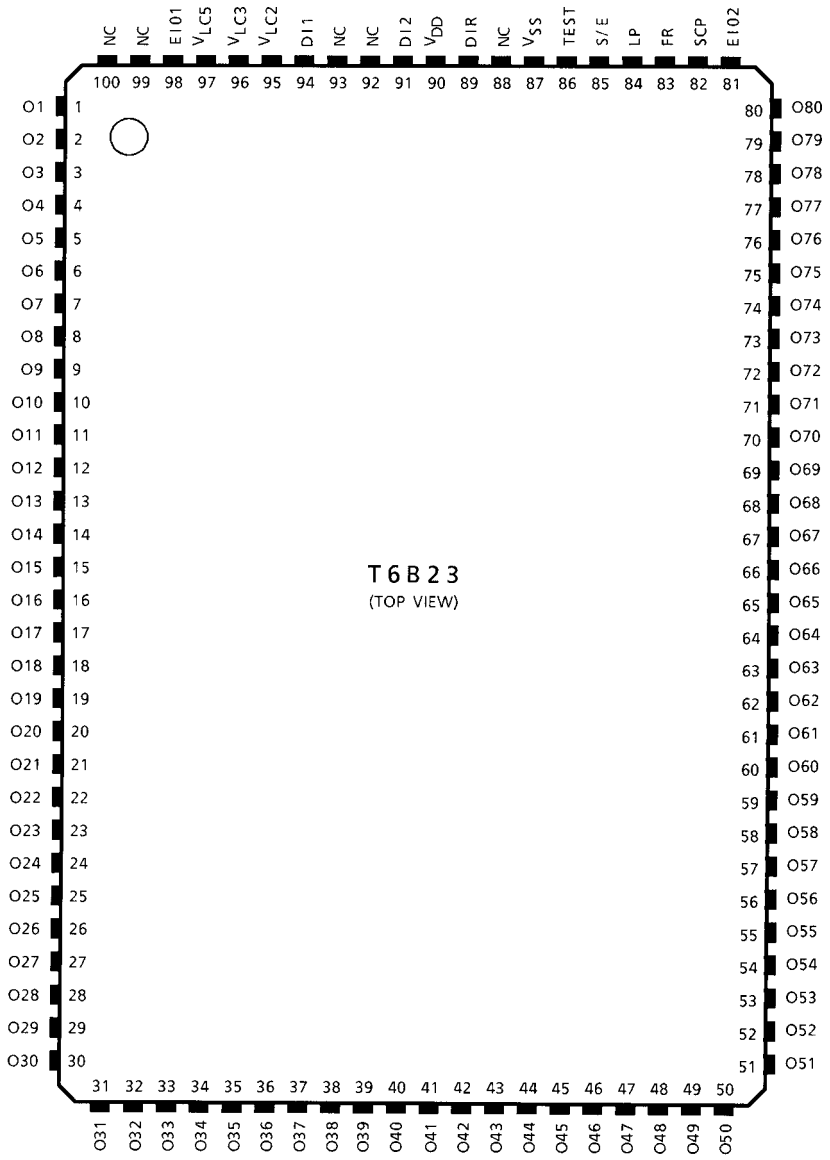
QFP100-P-1420-0.65J

Weight : 1.6 g (typ.)

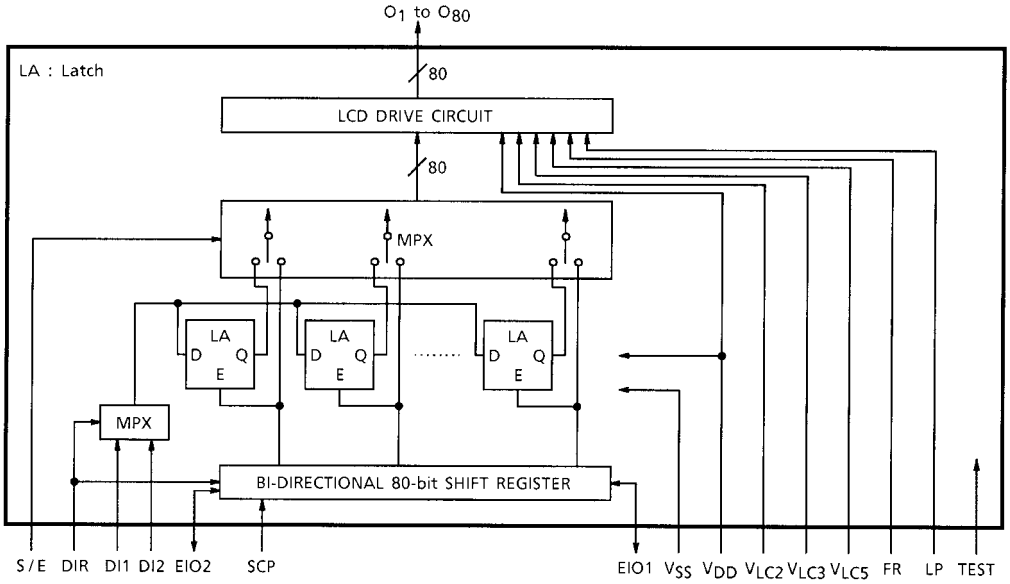
FEATURES

- 80-output column driver
- Data input format : ENABLE mode
  : SHIFT mode
- Two types of data flow:
  (1) $O_1 \rightarrow O_{80}$
  (2) $O_{80} \rightarrow O_1$
- Low power consumption
- Logic voltage : 5.0V ± 10%
- LCD drive voltage : V_{DD} − 3.0V to V_{DD} − 11.0V
- 100-pin plastic flat package

PIN ASSIGNMENT



BLOCK DIAGRAM



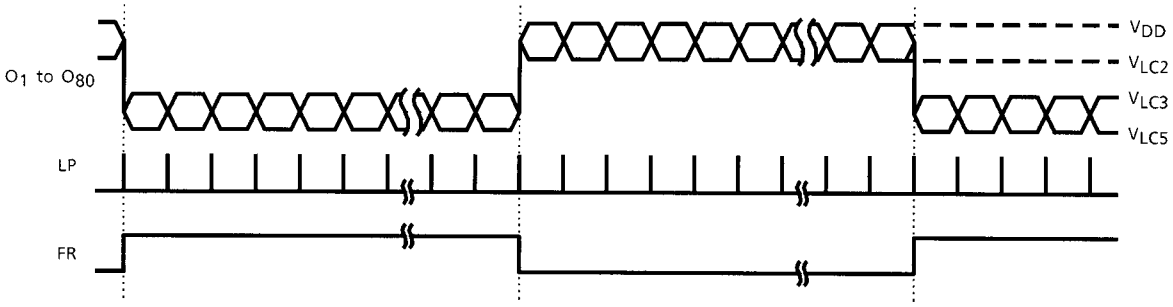
PIN FUNCTIONS

PIN NAME	I / O	FUNCTIONS	LEVEL
O1 to O80	Output	LCD drive output	V_{DD} to V_{LC5}
DI1, DI2	Input	Data signal input	V_{DD} to V_{SS}
EIO1, EIO2	I / O	ENABLE I / O When S / E = H, this pin is for input.	
SCP	Input	(Shift Clock Pulse) Shift clock pulse input	
FR	Input	(Frame) Frame signal input	
LP	Input	(Latch Pulse) Latch pulse signal input	
S / E	Input	Extension driver select input	
DIR	Input	Input data flow direction select input	
TEST	Input	Test pin: usually connected to V_{SS}.	
$V_{LC2, 3, 5}$	—	Power supply for LCD drive	—
V_{DD}	—	Power supply (5V)	
V_{SS}	—	Power supply (0V)	

FUNCTION OF DATA AND ENABLE PINS

S / E DIR		DI1	DI2	EIO1	EIO2	DATA FLOW	FIRST DATA	LAST DATA	MODE
L	L	Open	DATA INPUT	ENABLE signal input	ENABLE signal output	$O_{80} \rightarrow O_1$	O_1	O_{80}	ENABLE
L	H	DATA INPUT	Open	ENABLE signal output	ENABLE signal input	$O_1 \rightarrow O_{80}$	O_{80}	O_1	
H	L	Open	Open	DATA INPUT	DATA OUTPUT	$O_1 \rightarrow O_{80}$	O_{80}	O_1	SHIFT
H	H	Open	Open	DATA OUTPUT	DATA INPUT	$O_{80} \rightarrow O_1$	O_1	O_{80}	

TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

ITEM	SYMBOL	RATING	UNIT
Supply Voltage (1)	V_{DD} (Note 1)	− 0.3 to 7.0	V
Supply Voltage (2)	V_{LC2}, V_{LC3}, V_{LC5} (Note1, 2)	V_{DD} − 12.0 to V_{DD} + 0.3	V
Input Voltage	V_{IN} (Note 1)	− 0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opr}	− 20 to 75	°C
Storage Temperature	T_{stg}	− 55 to 125	°C

Note 1: Referenced to V_{SS} = 0 V

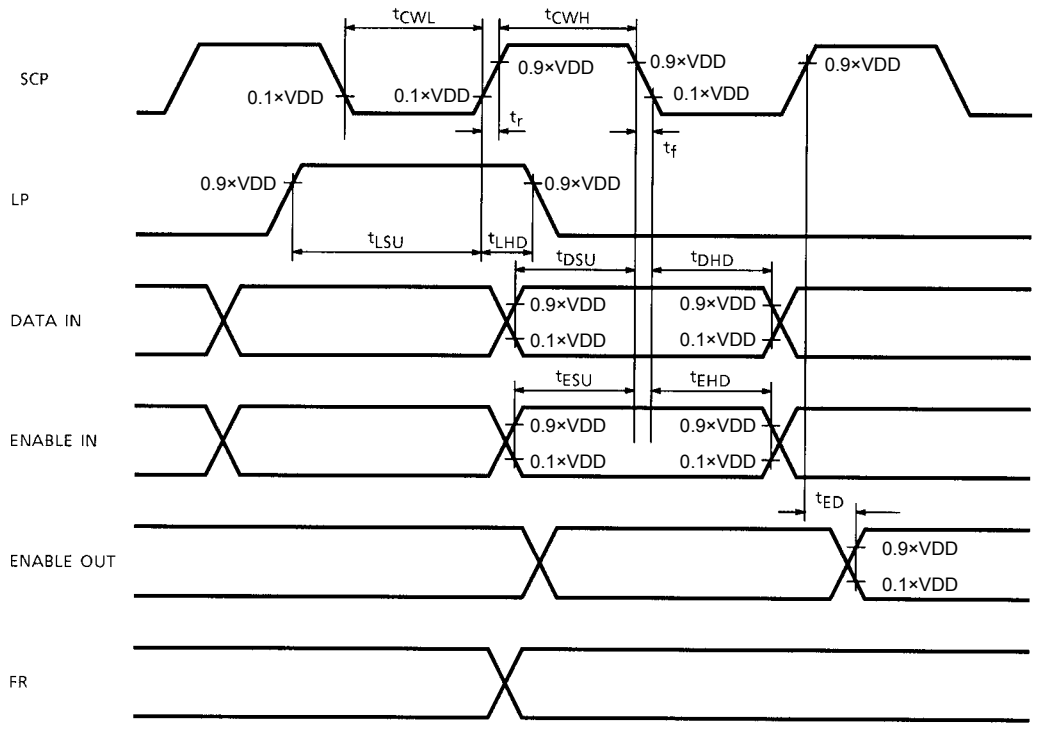
Note 2: Ensure that the following condition is always maintained.
$V_{DD} \geq V_{LC2} \geq V_{LC3} \geq V_{LC5}$.

ELECTRICAL CHARACTERISTICS
DC CHARACTERISTICS
TEST CONDITIONS (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, V_{LC5} = 0V, Ta = −20 to 75°C)

ITEM		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN	TYP.	MAX	UNIT	PIN NAME
Operating Voltage (1)		V_{DD}	—	—		4.5	5.0	5.5	V	V_{DD}
Operating Voltage (2)		VLC5	—	—		V_{DD} − 11.0	—	V_{DD} − 3.0	V	VLC5
Input Voltage	H Level	V_{IH}	—	—		V_{DD} − 1.0	—	V_{DD}	V	(*)
	L Level	V_{IL}		—		0	—	1.0	V	(*)
Output Voltage	H Level	V_{OH}	—	I_{OH} = −0.4 mA		V_{DD} − 0.4	—	V_{DD}	V	EIO1, EIO2
	L Level	V_{OL}		I_{Oh} = 0.4 mA		0	—	0.4	V	EIO1, EIO2
Output Resistance		R_{COL}	—	I_d = ±50μA		—	—	30	kΩ	O_1 to O_{80}
Operating Frequency		f_{scp}	—	Ta = −20to 75°C		—	—	400	kHz	SCP
Current Consumption		I_{SS}	—	V_{DD} = 5.0 V V_{LC2} = 3.0 V V_{LC3} = 2.0 V V_{LC5} = 0.0 V f_{FR} = 39 Hz f_{SCP} = 250 kHz 0_1 to 0_{80} :No Load	Binary Data Input	—	—	1.0	mA	V_{SS}
					Input Data : LOW Constant	—	—	0.4	mA	

*: SCP, LP, FR, EIO1, EIO2, DI1, DI2, DIR, S / E, TEST

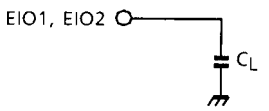
AC CHARACTERISTICS



TEST CONDITIONS (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 5 V ± 10%, V_{LC5} = 0 V, Ta = −20 to 75°C)

ITEM	SYMBOL		MIN	MAX	UNIT
Operating Frequency	f_{SCP}		—	400	KHz
SCP Pulse Width	t_{CWH}, t_{CWL}		800	—	ns
SCP Rise / Fall Time	t_r, t_f		—	200	ns
LP Set-up Time	t_{LSU}		500	—	ns
LP Hold Time	t_{LHD}		—	10	ns
Data Set-up Time	t_{DSU}	(Note 1)	300	—	ns
Data Hold Time	t_{DHD}	(Note 1)	300	—	ns
Enable Set-up Time	tESU	(Note 2)	300	—	ns
Enable Hold Time	t_{EHD}	(Note 2)	300	—	ns
Enable Delay Time	t_{ED}	(Note 3)	—	500	ns

LOAD CIRCUIT



C_L = 50pF
(including wiring capacitance)

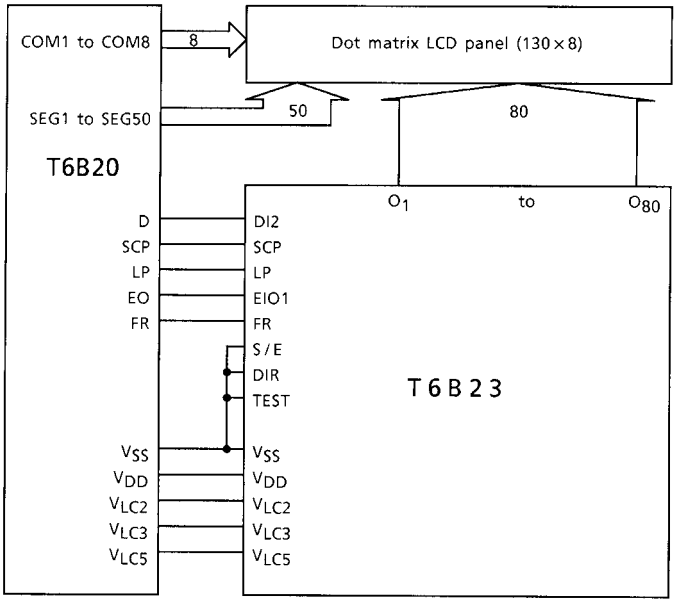
Note 1: Applies to DI1 and DI2.

Note 2: Applies to EIO1 and EIO2.

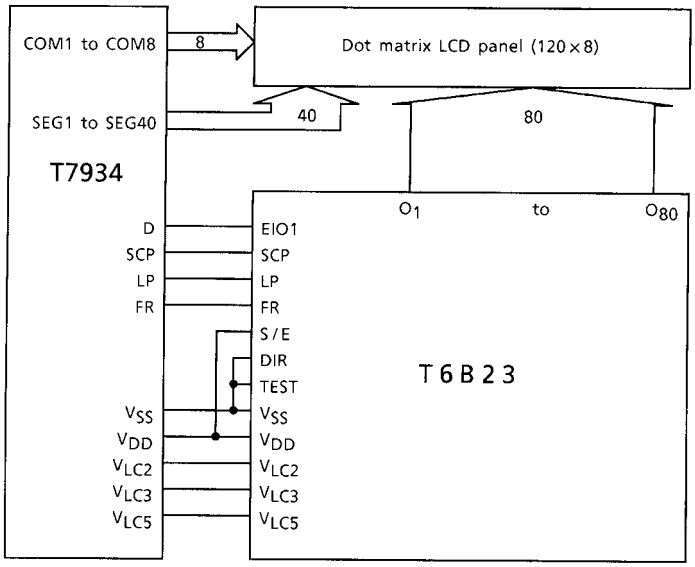
Note 3: With load circuit connected

APPLICATION CIRCUIT

(a) S / E = L (ENABLE mode)

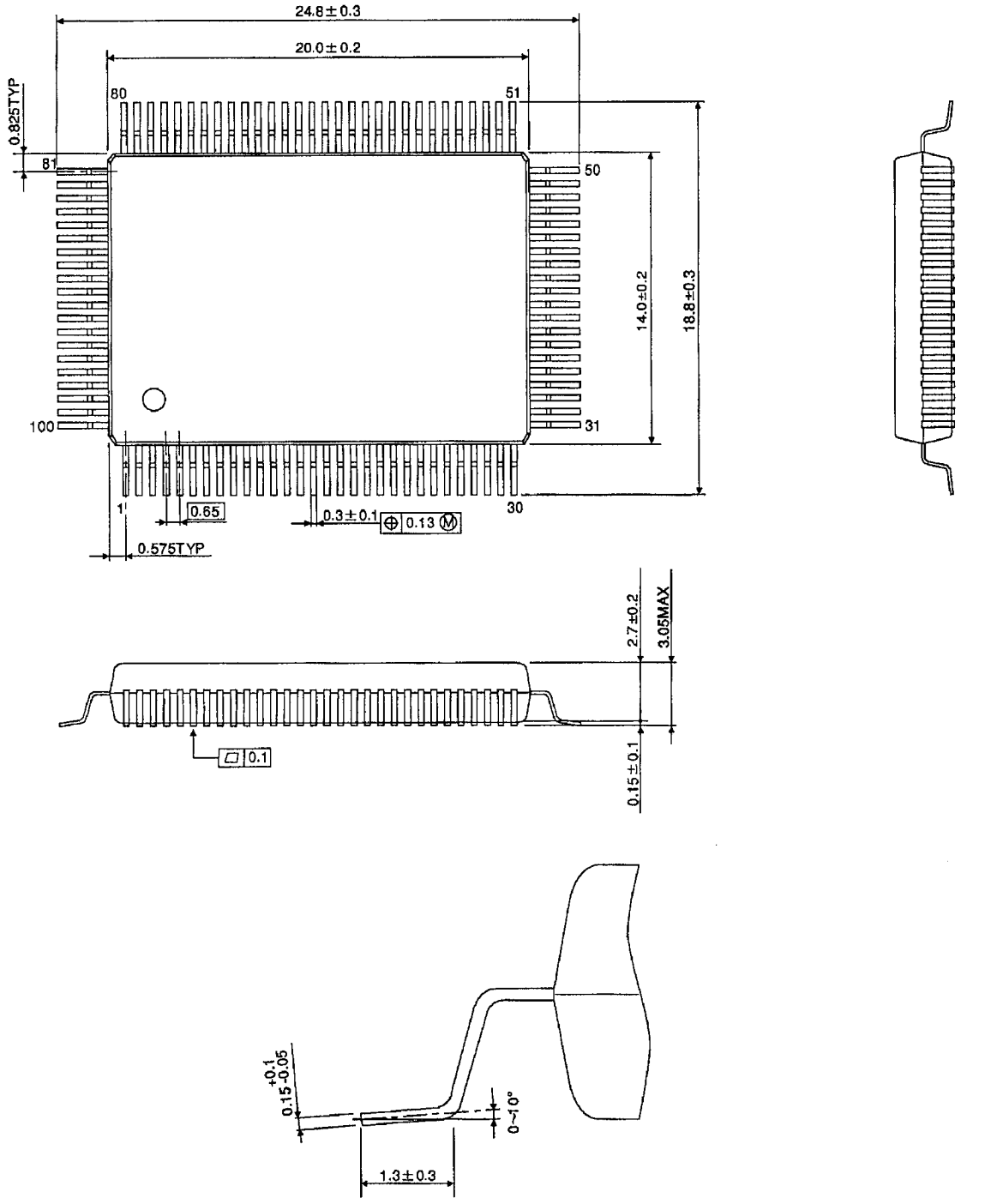


(b)S / E = H (SHIFT mode)



Package Dimensions

QFP100-P-1420-0.65J Unit: mm



Weight : 1.6 g (Typ.)

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