TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T6C23

COLUMN DRIVER LSI FOR A DOT MATRIX GRAPHIC LCD

The T6C23 is a column (segment) driver for a dot matrix graphic LCD. The T6C23 realizes low power consumption, due to the CMOS Si-Gate process. It is designed to directly with a microprocessor unit (MPU). A program running on the MPU can drive the T6C23 asynchronously. The T6C23 stores data transferred from the MPU in its built-in RAM. The data stored in the built-in display RAM corresponds to the image on the LCD screen; the data is converted into the LCD drive signal. A configuration of two T6C23s and one T6C24 can be used to drive a 320 × 240-dot LCD.

Unit: mm

T6C23	LEAD PITCH	
	IN	OUT
(UAM)	0.8	0.21
(UBM)	0.8	0.21
(UCM, 6NS)	0.8	0.21
(UEM, 6FS)	0.8	0.21
(UFM, 6FS)	0.8	0.21

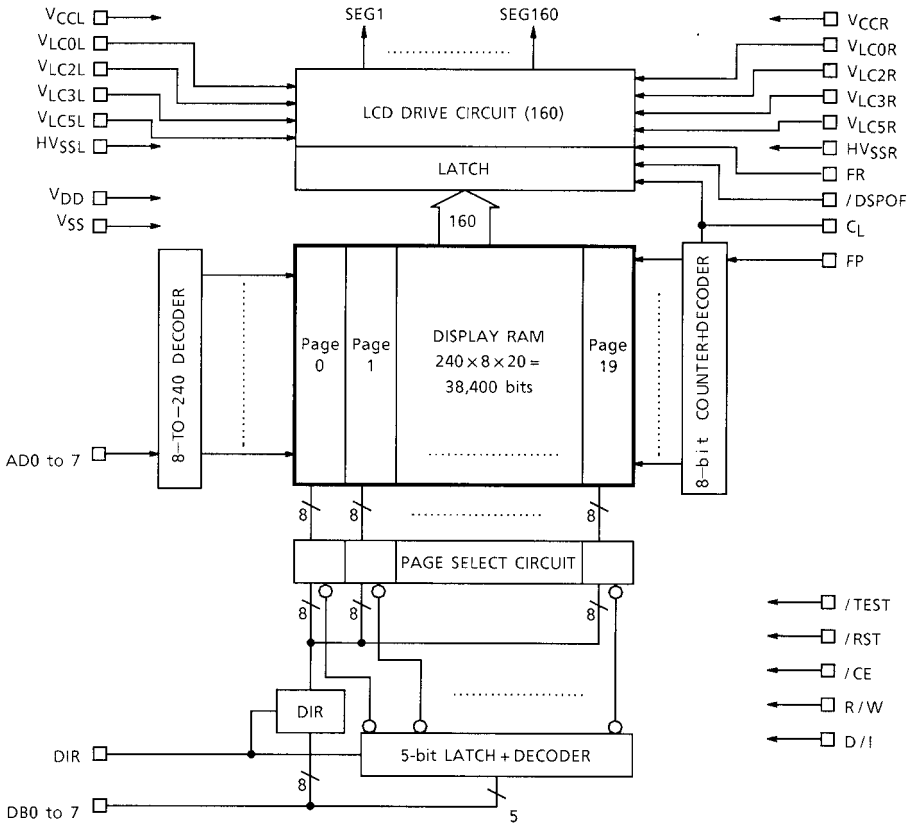
Please contact Toshiba or an authorized Toshiba dealer for information on package dimensions.

TCP (Tape Carrier Package)

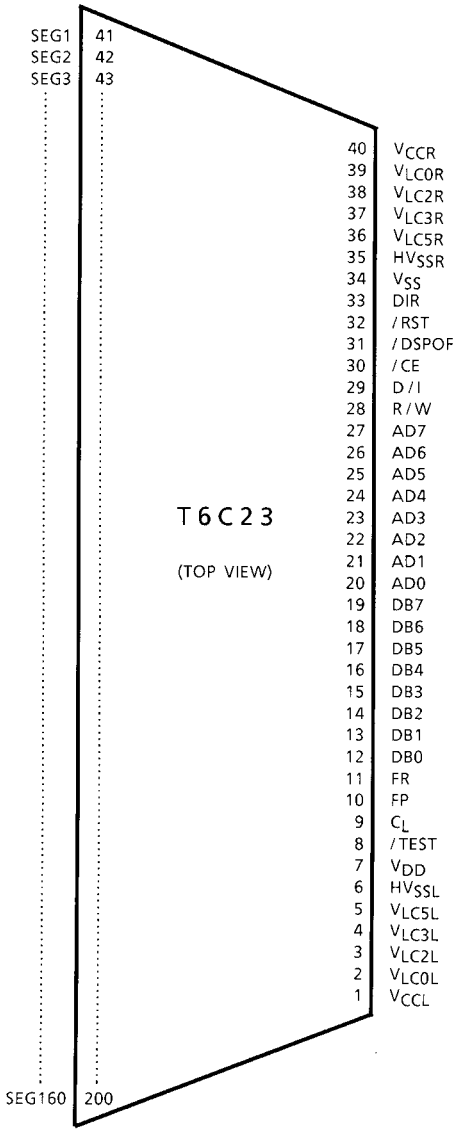
Features

- Dot matrix graphic LCD column driver with display RAM
- Display RAM capacity: 240 lines × 20 pages × 8 bits = 38400 bits
- LCD drive output: 160
- Interface: 8-bit MPU
- Relation between RAM data and display
  RAM bit data = 1 → display ON
  RAM bit data = 0 → display OFF
- Duty: Can be controlled by a T6C24 (row driver)
- Display OFF function
- Low power consumption
- Logic power supply: 2.7 to 5.5 V
- LCD power supply: 8.0 to 30.0 V
- Package: TCP (Tape Carrier Package)

Block Diagram



Pin Assignment



Note: The above diagram shows the pin configuration of the LSI chip; it does not show the configuration of the tape carrier package.

Pin Functions

Pin Name	Pin No.	I / O	Functions
SEG1 to SEG160	41 to 200	Output	Column driver outputs
C_L	9	Input	Shift clock pulse
FP	10	Input	Display synchronous signal
FR	11	Input	Frame signal
DB0 to DB7	12 to 19	I / O	Data bus
AD0 to AD7	20 to 27	Input	Address bus
R / W	28	Input	Read / write select R / W = H → Read selected R / W = L → Write selected
D / I	29	Input	Data / instruction select D / I = L → Page data D / I = H → Display data
/ CE	30	Input	Chip enable Data write: Data write enabled on rising edge of / CE Data read: Data read out while / CE is at L level
/ DSPOF	31	Input	Display off. Usually connected to V_{DD} / DSPOF = H: Display−on mode (SEG1 to SEG160) are operational / DSPOF = L: Display−off mode (SEG1 to SEG160) are at the V_{SS} level
/ RST	32	Input	Reset signal: / RST = L → Reset state
DIR	33	Input	Data direction select
/ TEST	8	Input	Test terminal. Usually connected to V_{DD}
V_{DD}, V_{SS}	7, 34	—	Power supply
V_{CCL}, V_{CCR} V_{LC0L}, V_{LC0R} V_{LC2L}, V_{LC2R} V_{LC3L}, V_{LC3R} V_{LC5L}, V_{LC5R} HV_{SSL}, HV_{SSR}	1, 40 2, 39 3, 38 4, 37 5, 36 6, 35	—	Power supply for LCD drive

D / I	DB0 to DB7	AD0 to AD7
L	Page data (00H to 13H)	Do not select.
H	Display data	Address (00H to EFH)

Function of Each Block

- **RAM cell**

  The RAM capacity is 240 bytes × 20 pages.

- **5-bit latch + decoder**

  This register holds the page data. The decoder selects one of the RAM cell pages.

- **DIR**

  This circuit changes the data flow direction and page selection sequence.

- **8-to-240 decoder**

  This decoder selects one of the 240 address line of RAM cells for read / write operation.

- **8-bit counter + decoder**

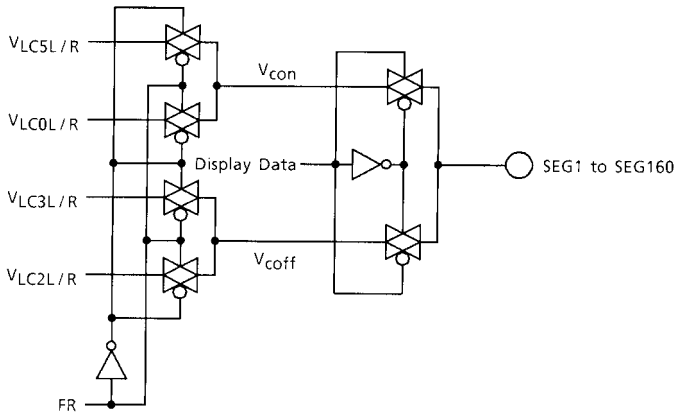
  The decoder selects one RAM cell from the 240 address lines for display operation.

- **Latch**

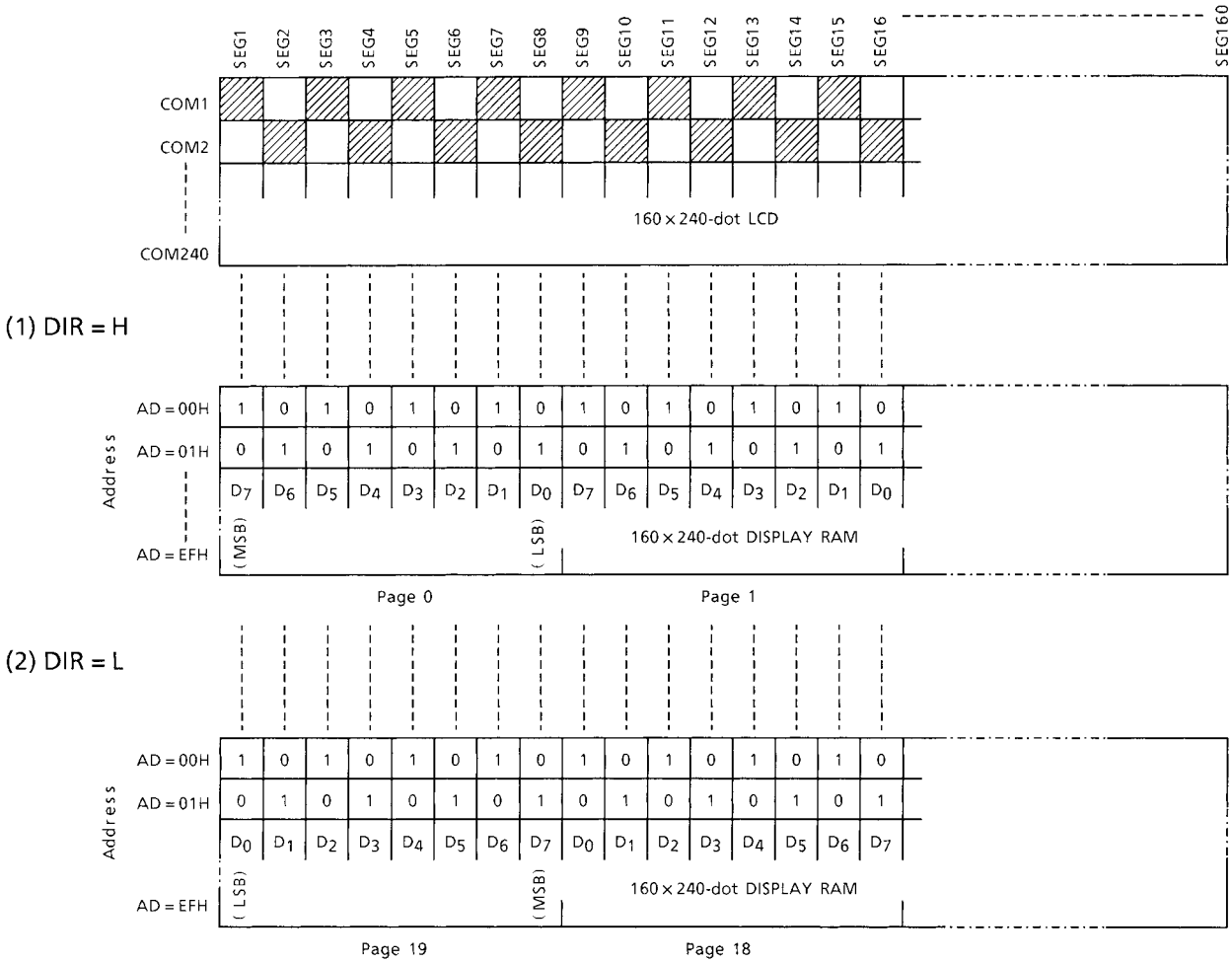
  The data is latched from the display RAM on the rising edge of C_L.

- **Column driver circuit and LCD voltage generation circuit**

  The T6C23 has 160 column drivers and four different LCD drive output voltage levels. The display data from the latch circuit and the M signal determine which of the four LCD drive voltages is selected. This circuit is shown in the following diagram.



- **The relation between DIR and the memory map**



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage (1)	V_{DD} (Note 2)	−0.3 to 7.0	V
Supply Voltage (2)	(Note 1, 2)	−0.3 to 32.0	V
Input Voltage	V_{In} (Note 2, 3)	−0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opr}	−20 to 75	°C
Storage Temperature	T_{stg}	−55 to 125	°C

Note 1: V_{CCL}, V_{CCR}, V_{LC0L}, V_{LC0R}, V_{LC2L}, V_{LC2R}, V_{LC3L}, V_{LC3R}, V_{LC5L} and V_{LC5R}
Note 2: Referenced to V_{SS}, HV_{SSL} and HV_{SSR}
Note 3: Applies to all data bus and I / O pins.
Note 4: Ensure that the following condition is always maintained.
$V_{CCL / R} \geq V_{LC0L / R} \geq V_{LC2L / R} \geq V_{LC3L / R} \geq V_{LC5L / R} \geq HV_{SSL / R}$

Electrical Characteristics
DC Characteristics
Test Conditions (1) (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 3.0 V ± 10%, $V_{CCL\,/\,R}$ = 23.0 V ± 10%, Ta = −20 to 75°C)

Item		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Pin Name
Operating Supply (1)		V_{DD}	—	—	2.7	—	3.3	V	V_{DD}
Operating Supply (2)		V_{CC}	—	—	8.0	—	30.0	V	V_{CCL}, V_{CCR}
Input Voltage	H Level	V_{IH}	—	—	0.7 V_{DD}	—	V_{DD}	V	DB0 to DB7 AD0 to AD7, / RST / DSPOF, / CE, R / W, D / I, C_L, FP FR, DIR, / TEST
	L Level	V_{IL}	—	—	0	—	0.3 V_{DD}	V	
Output Voltage	H Level	V_{OH}	—	I_{OH} = −400 μA	V_{DD} − 0.4	—	—	V	DB0 to DB7
	L Level	V_{OL}	—	I_{OL} = 400 μA	—	—	0.4	V	
Column Driver Output Resistance		R_{col}	—	(Note 4) Load current = ±100 μA	—	—	3.0	kΩ	SEG1 to SEG160
Input Leakage		I_{IL}	—	V_{IN} = V_{DD} to V_{ss}	−1	—	1	μA	DB0 to DB7 AD0 to AD7, / RST / DSPOF, / CE, R / W, D / I, C_L, FP FR, DIR, / TEST
Operating Freq.		f_{CL}	—	—	10	—	50	kHz	C_L
Current Consumption (1)		I_{SS1}	—	(Note 1)	—	2.4	3.3	mA	V_{SS}, HV_{SSL}, HV_{SSR} V_{LC5L}, V_{LC5R}
Current Consumption (2)		I_{SS2}	—	(Note 2)	—	57	70	μA	
Current Consumption (3)		I_{SS3}	—	(Note 3)	−1	—	1	μA	

Note 1: Current consumption while internal data receiver is operating
V_{DD} = 3.0 V ± 10%, $V_{CCL\,/\,R}$ = 23.0 V, Ta = 25°C, 1/13 bias, 1/240 duty, no load, f_{FP} = 70Hz, f / $_{CE}$ = 5 MHz

Note 2: Current consumption while internal data receiver is sleeping
V_{DD} = 3.0 V ± 10%, $V_{CCL\,/\,R}$ = 23.0 V, Ta = 25°C, 1/13 bias, 1/240 duty, no load, f_{FP} = 70 Hz, f / $_{CE}$ = 0 Hz

Note 3: Standby current: V_{DD} = 3.0 V ± 10%, $V_{CCL\,/\,R}$ = 23.0 V, Ta = 25°C, no load, f_{FP} = 0 Hz, f / $_{CE}$ = 0 Hz

Note 4: $V_{CCL\,/\,R}$ = $V_{LC0L\,/\,R}$ = 23.0 V, $V_{LC2L\,/\,R}$ = V_{CC} × 11 / 13, $V_{LC3L\,/\,R}$ = V_{CC} × 2 / 13, $HV_{SSL\,/\,R}$ = $V_{LC5L\,/\,R}$ = 0 V

Test Conditions (2) (**Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, $V_{CCL\ /\ R}$ = 23.0 V ± 10%, Ta =−20 to 75°C**)

Item		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Pin Name
Operating Supply (1)		V_{DD}	—	—	4.5	—	5.5	V	V_{DD}
Operating Supply (2)		V_{CC}	—	—	8.0	—	30.0	V	V_{CCL}, V_{CCR}
Input Voltage	H Level	V_{IH}	—	—	0.7 V_{DD}	—	V_{DD}	V	DB0 to DB7 AD0 to AD7, / RST / DSPOF, / CE, R / W, D / I, C_L, FP FR, DIR, / TEST
	L Level	V_{IL}	—	—	0	—	0.3 V_{DD}	V	
Output Voltage	H Level	V_{OH}	—	I_{OH} = −400 μA	V_{DD} − 0.4	—	—	V	DB0 to DB7
	L Level	V_{OL}	—	I_{OL} = 400 μA	—	—	0.4	V	
Column Driver Output Resistance		R_{col}	—	(Note 4) Load current = ±100 μA	—	—	3.0	kΩ	SEG1 to SEG160
Input Leakage		I_{IL}	—	V_{IN} = V_{DD} to V_{ss}	−1	—	1	μA	DB0 to DB7 AD0 to AD7, / RST / DSPOF, / CE, R / W, D / I, C_L, FP FR, DIR, / TEST
Operating Freq.		f_{CL}	—	—	10	—	50	kHz	C_L
Current Consumption (1)		I_{SS1}	—	(Note 1)	—	5.4	6.5	mA	V_{SS}, HV_{SSL}, HV_{SSR} V_{LC5L}, V_{LC5R}
Current Consumption (2)		I_{SS2}	—	(Note 2)	—	57	70	μA	
Current Consumption (3)		I_{SS3}	—	(Note 3)	−1	—	1	μA	

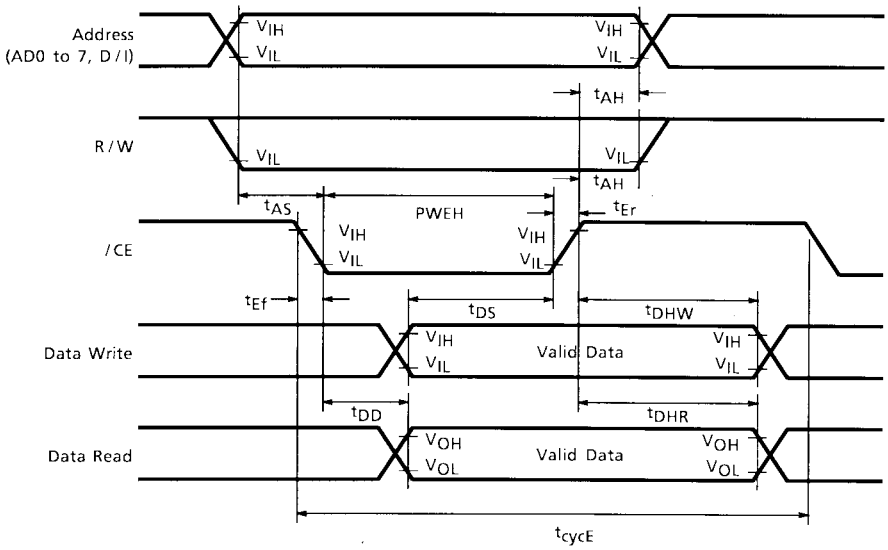
Note 1: Current consumption while internal data receiver is operating
V_{DD} = 5.0 V ± 10%, $V_{CCL\ /\ R}$ = 23.0 V, Ta = 25°C, 1/13 bias, 1/240 duty, no load, f_{FP} = 70 Hz, $f_{/\ CE}$ = 5 MHz

Note 2: Current consumption while internal data receiver is sleeping
V_{DD} = 5.0 V ± 10%, $V_{CCL\ /\ R}$ = 23.0 V, Ta = 25°C, 1/13 bias, 1/240 duty, no load, f_{FP} = 70 Hz, $f_{/\ CE}$ = 0 Hz

Note 3: Standby current: V_{DD} = 5.0 V ± 10%, $V_{CCL\ /\ R}$ = 23.0 V, Ta = 25°C, no load, f_{FP} = 0 Hz, $f_{/\ CE}$ = 0 Hz

Note 4: $V_{CCL\ /\ R}$ = $V_{LC0L\ /\ R}$ = 23.0 V, $V_{LC2L\ /\ R}$ = V_{CC} × 11 / 13, $V_{LC3L\ /\ R}$ = V_{CC} × 2 / 13, $HV_{SSL\ /\ R}$ = $V_{LC5L\ /\ R}$ = 0 V

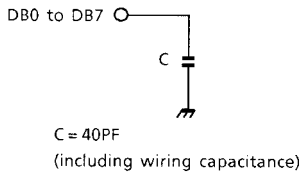
AC Characteristics



Test Conditions (1)
(Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 3.0 V ± 10%, Ta = −20 to 75°C)

Item	Symbol	Min	Max	Unit
Enable Cycle Time	t_{cycE}	500	—	ns
Enable Pulse Width	PWEH	400	—	ns
Enable Rise / Fall Time	t_{Er}, t_{Ef}	—	15	ns
Address Set-up Time	t_{AS}	0	—	ns
Address Hold Time	t_{AH}	10	—	ns
Data Set-up Time	t_{DS}	60	—	ns
Data Hold Time	t_{DHW}	5	—	ns
Data Delay Time	t_{DD} (Note)	—	240	ns
Data Hold Time	t_{DHR} (Note)	5	—	ns

Load Circuit

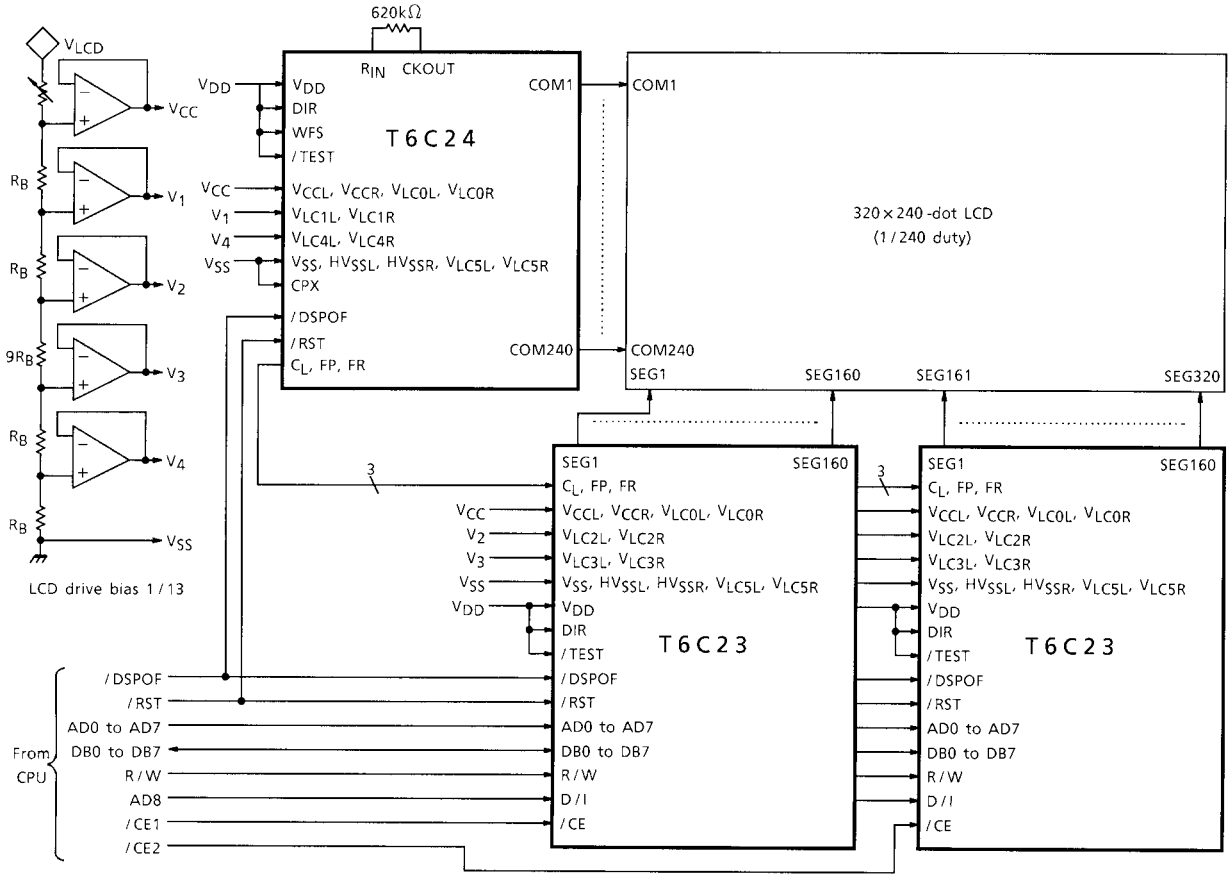


Test Conditions (2)
(Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, Ta = −20 to 75°C)

Item	Symbol	Min	Max	Unit
Enable Cycle Time	t_{cycE}	200	—	ns
Enable Pulse Width	PWEH	160	—	ns
Enable Rise / Fall Time	t_{Er}, t_{Ef}	—	10	ns
Address Set-up Time	t_{AS}	0	—	ns
Address Hold Time	t_{AH}	10	—	ns
Data Set-up Time	t_{DS}	60	—	ns
Data Hold Time	t_{DHW}	5	—	ns
Data Delay Time	t_{DD} (Note)	—	180	ns
Data Hold Time	t_{DHR} (Note)	5	—	ns

Note: With load circuit connected

T6C23, T6C24 Application Circuit



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