TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T6K18

COLUMN AND ROW DRIVER LSI FOR A DOT MATRIX GRAPHIC LCD

The T6K18 is a driver for small−to−medium−sized dot matrix Liquid Crystal Display (LCD). This driver combines the functions of the T9841B (column driver) and T9842B (row driver) into a more functionally advanced single−chip device.
The T6K18 can be interfaced with 8−bit general MPU; it operates asynchronously with the MPU. The T6K18 contains an RC oscillator circuit to generate the timing signal required for display and has a built−in RAM to store the display data. Each cell in this RAM corresponds to each dot on the dot matrix LCD. Therefore, the display data written to the RAM is corresponded one to one to the LCD as the LCD drive signal output. The T6K18 has 80 outputs for LCD drive signals (columns) that are equivalent to display data and 26 outputs for LCD drive signals (rows) that are equivalent to scan signals. Consequently, this single chip can drive up to 80 × 26 dots of LCD display with minimal power.

Unit: mm

T6K18	User Area Pitch	
	IN	OUT
(UAM, 5NS)	0.7	0.26

Please contact Toshiba or its distributor for information about the latest TCP specification and product lineup.

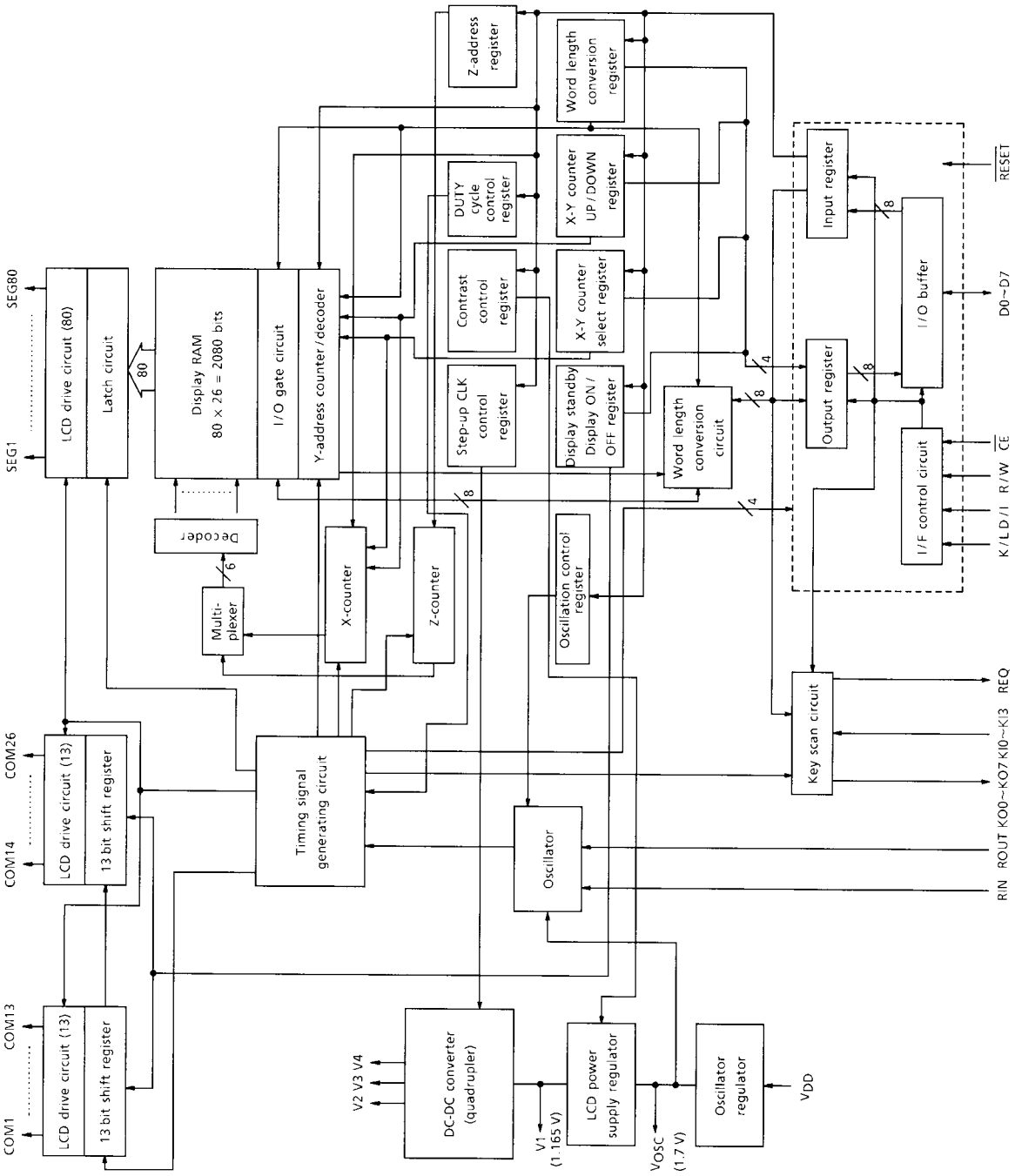
TCP (Tape Carrier Package)

In addition, the T6K18 has the LCD power supply regulator, a voltage quadrupler, and a contrast control circuit enabling the LCD to be driven by a single power supply. To minimize current consumption in the oscillator, the T6K18 has an oscillator regulator. The T6K18 has key scan circuit which can construct (max.) 32 (4 × 8) key matrix.

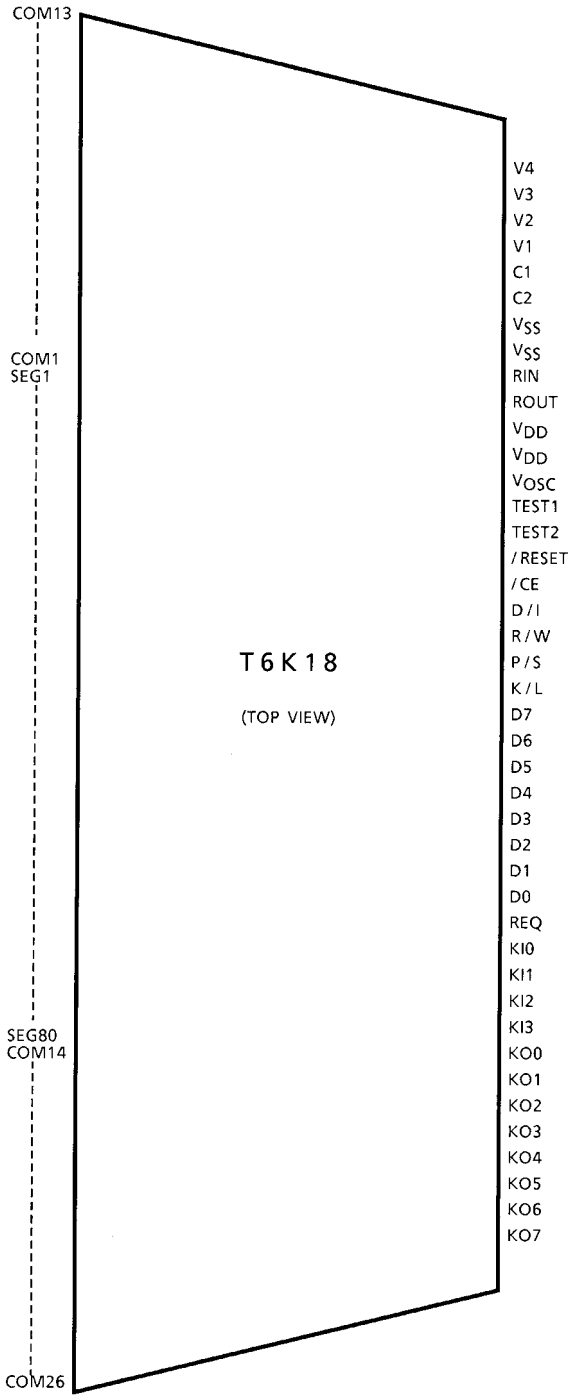
Features

- Built−in display RAM with 80 × 26 = 2080 bits of capacity.
- Direct RAM data display
  Dots are turned on when bit data in RAM = 1.
  Dots are not turned on when bit data in RAM = 0.
- Display duty cycle : 1/26 or 1/18 duty (switchable)
- Display data word length can be switched between 8 bits and 6 bits according to character font.
- LCD display drive circuit
  Segment output : 80 lines
  Common output : 26 or 18 lines (switchable)
- Can be interfaced with 8−bit general MPU (operated asynchronously).
- Data interface : Parallel data interface.
- Built−in oscillator circuit regulator (oscillator unit only is operated with 1.7 V).
- Key scan circuit : Able to construct max. 32 (4 × 8) key matrix.
- Built−in RC oscillator (capacitor internal and resistor external to the chip)
  T6K18 is able to switch to external clock input by software.
- Built−in LCD power supply regulator, voltage quadrupler, and contrast control circuits (16−gradation). (4.1 to 5.3 V, 0.08 V / step)
- Low power consumption (10 μA during display without data access when operating at 3.0 V).
- CMOS process.
- Low−voltage operation : 1.8 to 5.5 V
- Operating voltage of LCD drive signal
  : (1) V4 = 4 times the LCD power supply regulator output V1.
  (2) 1 / 4 bias
- Package : Bump chip and 148 pins TCP

Block Diagram



Pin Assignment



Note: The above TCP pin assignment is shown for reference purposes only.

Pin Function

Name	I / O	Function
SEG1 to SEG80	Output	Column drive output
COM1 to COM26	Output	Row driver output
D0 to D7	I / O	Data bus
P / S	Input	LSI test pin ● Leave this pin connect to V_{DD}
K / L	Input	KEY / LCD data output select pin
D / I	Input	Data / instruction select signal input pin ● When D / I = High → The data on D0 to D7 is assumed to be display data. ● When D / I = Low → The data on D0 to D7 is assumed to be instruction data.
R / W	Input	Write select signal ● When R / W = High → The device is readied to read data. ● When R / W = Low → The device is readied to write data.
/ CE	Input	Chip enable signal input pin ● When writing the D0 to D7 data, drive /CE from low to high when R / W = low. ● When reading the D0 to D7 data, the data is output while /CE is held low when R / W = high.
REQ	Output	Key request output pin
KI0 to KI3	Input	Key scan data input pins
KO0 to KO7	Output	Key scan data output pins
/ RESET	Input	Reset signal input pin
RIN, ROUT	—	Connect an external resistor between these pins to use the built−in RC oscillator. If you want an external clock input, use RIN for clock input and leave ROUT open.
V_{OSC}	—	Oscillator circuit regulator output pin
C1, C2	—	External capacitor connecting pins
V1	—	LCD power supply regulator output pin
V2	—	×2 step−up voltage output pin
V3	—	×3 step−up voltage output pin
V4	—	×4 step−up voltage output pin
V_{DD}, V_{SS}	—	Power supply pins
TEST1, TEST2	Input	LSI test pin ● Leave this pin open or connect to V_{SS}.

Functional Specification and Device Operation

● Interface logic

The T6K18 can be interfaced with 8−bit general MPU.
Fig. 1 shows an example of how the device is interfaced with the MPU.

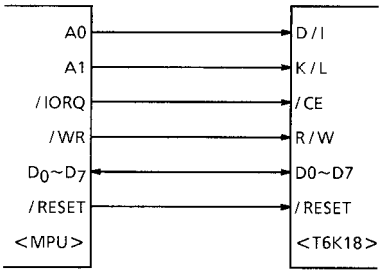


Fig. 1

● Input register

This register holds the 8−bit data from the MPU.
The data held in this register is discriminated between instruction and display data by the D / I signal.

● Output register

This register holds the 8−bit data to the MPU.
The data in this register came from the display RAM or STRD register is discriminated between display data and instruction by D / I signal.

● X−address counter

This counter is a 26−up / down−counter used to hold the address in the column direction of the display RAM. When X−counter is selected by a command, the counter is automatically incremented or decremented by 1 each time the MPU reads or writes to the display RAM.

● Y (Page) −address counter

This counter has its count values changed depending on the word length of display data.
If the display data word length is 8 bits, the Y (page) −address counter is a 10−up / down−counter. If the word length is 6 bits, the Y (page) −address counter is a 14−up / down−counter. In either case, the counter holds the address in the row direction of the display RAM. When a Y (page) −counter is selected by a command, the counter is automatically incremented or decremented by 1 each time the MPU reads or writes to the display RAM.

● Z−address counter

This counter is a 26−up counter used to supply display data stored in RAM to the LCD driver circuit. The data held in the Z−address register are loaded to the counter as Z−address data.
For example, setting the Z−address to 13 starts the counter counting 13, 14, 15 to 24, 25, 0, 1, 2 then to 10, 11, and 12. The start line on the LCD screen is line 13 of display RAM.

- **X and Y−counter UP / DOWN register**

  This register holds data to determine whether the X−and Y−counters function as an up−or down−counter.

- **X and Y−counter select register**

  This register holds data to determine which counter is enabled, X−or Y−counter.

- **Display standby and display ON / OFF registers**

  The display standby register (1 bit) holds the standby status of display. When display is in standby state, the LCD drive signal is disabled (V_{SS}). In active state, the LCD drive signal is enabled for output.
  The display ON / OFF register (1 bit) holds the ON / OFF status of display. When display is in OFF state, the output from the display RAM is reset. In ON state, the display data is output from the display RAM. The data in the display RAM is not affected by the ON / OFF status of display.

- **Word length change register**

  This register holds data to determine whether the display data is read and written in 8 bits per word or 6 bits per word.

- **Word length change circuit**

  This circuit is controlled by the data held in the word length conversion register.
  If the word length is 8 bits, the 8−bit data is read and written directly as is. If the word length is 6 bits, the 8−bit display data held in the input register has had its two MSB bits nullified as the data is written to the display RAM as shown in Fig. 2. When reading data, the 6−bit data from the display RAM has had 0 s added in its two MSB bits so that it is stored in the output register as 8−bit data.

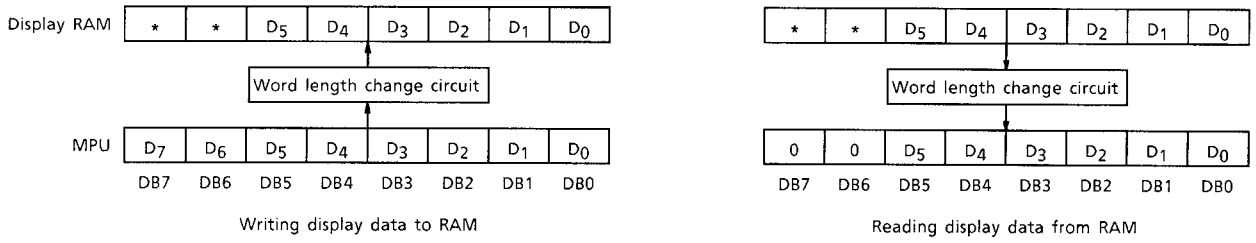


Fig. 2

- **Oscillator**

The oscillator in the T6K18 can be an RC oscillator. This case, connect an external resistor between the RIN and ROUT pins. When using external clock for the device, use RIN to supply the clock.

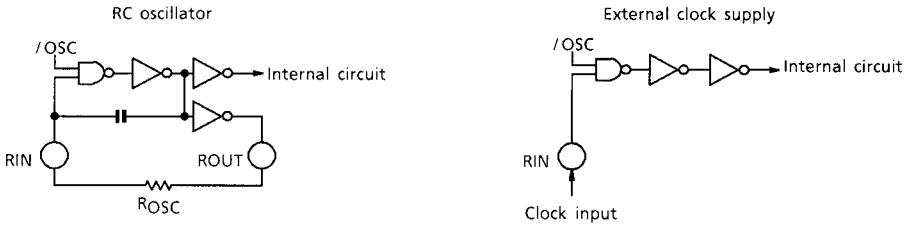


Fig. 3

- **Oscillation control register**

This register holds the active / inactive status of the oscillator.
When the oscillator is in inactive state, the internal logic of the device is stopped entirely because the oscillator is disabled. In active state, the oscillator is enabled supplying clock to the device. The oscillator circuit can be selected according to the type of oscillator (RC or external clock as described above).

- **Oscillator regulator**

This regulator generates V_{OSC} to drive the oscillator.
Connect a capacitor to V_{OSC} in order to stabilize the regulator voltage.

- **Timing signal generation circuit**

This circuit generates the necessary display timing signals and operating clock by dividing the source clock from the oscillator.

- **Shift register**

The T6K18 has two channels of 13 bit shift registers to shift the turn−on data that is required for common signals to drive the LCD.

- **Display latch circuit**

This circuit latches display data as it is fed from the display RAM.

- **Column driver circuit**

The column driver circuit consists of 80 driver circuits. Each driver circuit outputs one of the three LCD drive voltages that derive from a combination of the display data from the latch circuit and the M signal as shown in Fig. 4.
The diagram below depicts the column driver circuit.

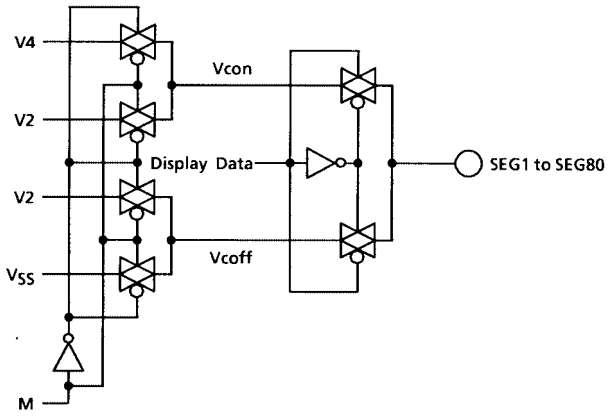


Fig. 4

- **Row driver circuit**

The row driver circuit consists of 26 driver circuits. each driver circuit outputs one of the four LCD drive voltages that derive from a combination of the shift register data and the M signal as shown in Fig. 5.
The diagram below depicts the row driver circuit.

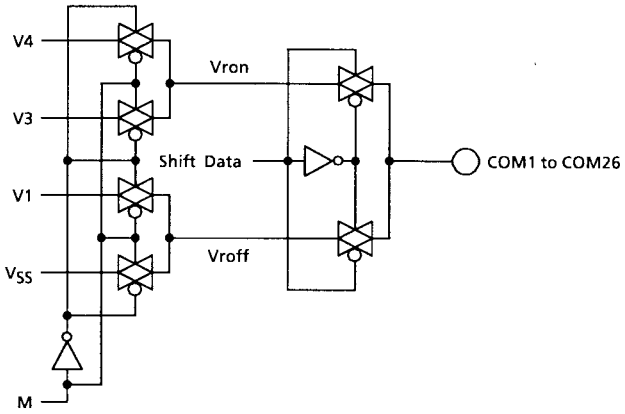


Fig. 5

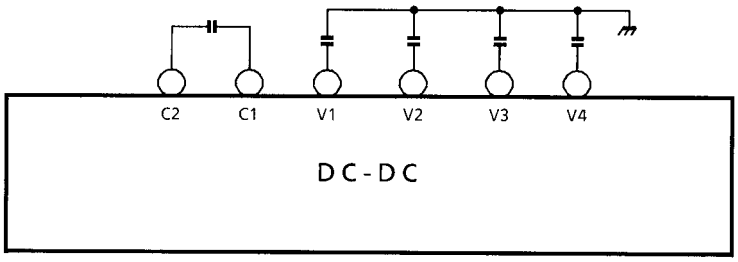
- **LCD power supply regulator**

This regulator generates the reference voltage V1 for the voltage quadrupler circuit that generates the power to LCD.
Connect a capacitor to V1 in order to stabilize the regulator output.

- **DC−DC converter (Voltage quadrupler)**

  This circuit boosts the V1 voltage generated by the LCD power supply regulator four−fold by using a step−up capacitor. Insert a step−up capacitor between C1 and C2 and connect smoothing capacitors to V2, V3 and V4. Normally use capacitors of about 0.1μF here.

Connecting Capacitors to the Voltage Quadrupler Circuit



- **Contrast control circuit**

  The T6K18 contains a contrast control circuit in their LCD power supply regulator.
  Contrast is varied in 16 steps by data from the contrast control register. This is done by changing the output voltage V1 of the LCD power supply regulator by using data from the contrast control register. The voltage quadrupler circuit generates the V4 voltages listed in the table below from the V1 reference voltage. (Refer to command definitions for details about CONT3 to CONT0.)

Table 1

CONT3	CONT2	CONT1	CONT0	V4 Output Voltage
1	1	1	1	5.24 V ± 0.2 V
1	1	1	0	5.17 V ± 0.2 V
1	1	0	1	5.10 V ± 0.2 V
1	1	0	0	5.02 V ± 0.2 V
1	0	1	1	4.95 V ± 0.2 V
1	0	1	0	4.88 V ± 0.2 V
1	0	0	1	4.81 V ± 0.2 V
1	0	0	0	4.73 V ± 0.2 V
0	1	1	1	4.66 V ± 0.2 V
0	1	1	0	4.59 V ± 0.2 V
0	1	0	1	4.51 V ± 0.2 V
0	1	0	0	4.44 V ± 0.2 V
0	0	1	1	4.36 V ± 0.2 V
0	0	1	0	4.29 V ± 0.2 V
0	0	0	1	4.21 V ± 0.2 V
0	0	0	0	4.13 V ± 0.2 V

- **Duty cycle control register**

This 1−bit register holds the selected status of the duty cycle.
The display duty cycle can be selected from 1/26 duty and 1/18 duty.

- **Display RAM**

The display RAM consists of an array of 80 cells in the segment (column) direction and 26 cells in the common (row) direction providing a total of 2080 bits of storage capacity. The dot matrix LCD (i.e., the display screen) and the display RAM have a relationship that each dot on the display screen corresponds to one bit in the display RAM as shown in Fig. 8. If the data written to RAM = 1, the dot on the display screen corresponding to that RAM cell is turned on (black). If the data written to RAM = 0, the corresponding dot on the display screen is turned off (white).

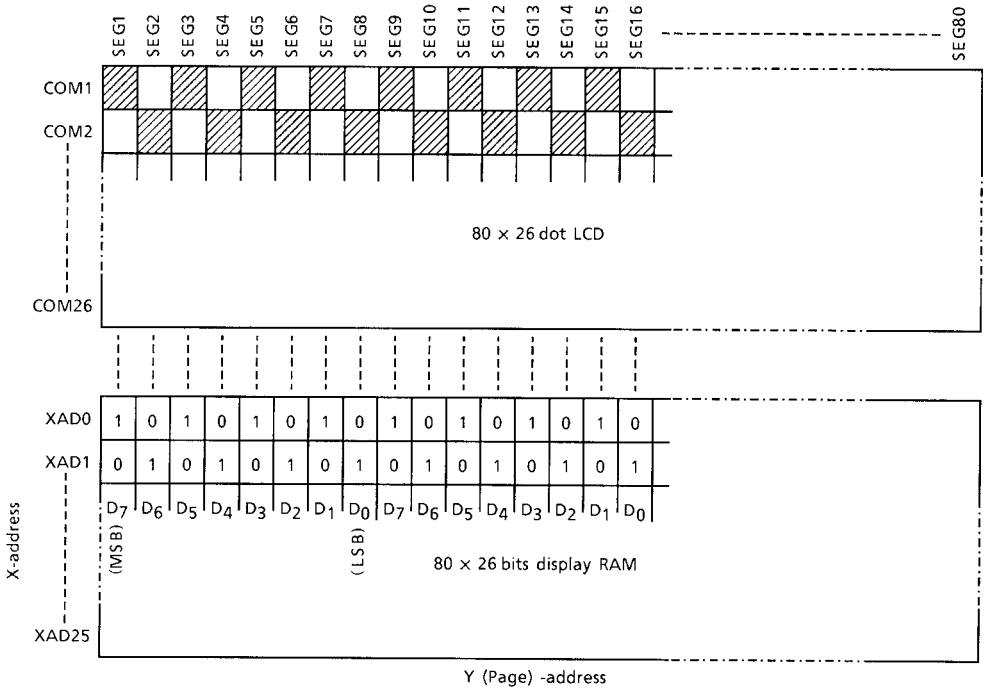
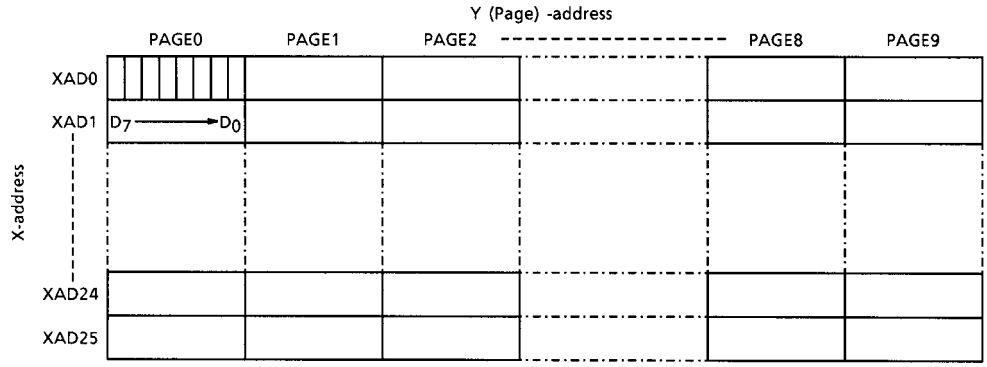


Fig. 8

Furthermore, the display RAM addresses change with the word length setting. If the word length is set to 8 bits / WORD by executing command 86BS, the Y (page) −address is assigned YAD0 to YAD9, with one page configured with 8 bits. If the word length is set to 6 bits / WORD, the Y (page) −address is assigned YAD0 to YAD13, with one page configured with 6 bits.

8 bits per word Mode



6 bits per word Mode

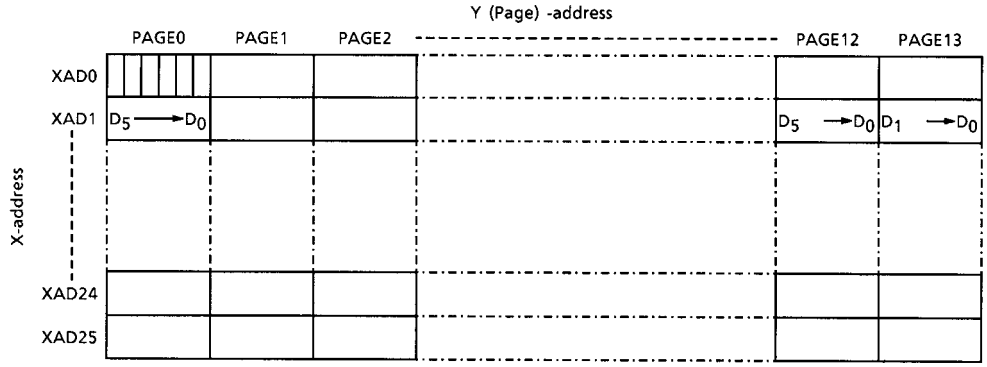


Fig. 9

- **Command definitions**

Command Name	K / L	R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0	Function
DISP	0	0	0	0	0	0	0	0	0	1 / 0	1 / 0	• Display ON / OFF (DISPON): D1 Display ON (1) / Display OFF (0) • Display standby (DISPST): D0 Active (1) / Standby (0)
BSDT	0	0	0	0	0	0	0	1	0	1 / 0	1 / 0	• Word length (86BS): D1 8 bits (1) / 6 bits (0) • Duty cycle (DUTY): D0 1/26 duty (1) / 1/18 duty (0)
OSC	0	0	0	0	0	0	1	0	0	0	1 / 0	• Oscillator enable (OSC) : Oscillation enabled (1) : Oscillation disabled (0)
OSCM	0	0	0	0	0	1	0	0	0	0	1 / 0	• Oscillation mode select
PUMP	0	0	0	0	1	0	0	0	0	1 / 0	1 / 0	• Voltage quadrupler clock select
CONT	0	0	0	0	1	1	1 / 0	Contrast (0 to 15)				• Voltage quadrupler enable (4BION): D4 Enabled (1) / Disabled (0) • Contrast set (CONT0 to CONT3) : D0 to D3
UDE	0	0	0	1	0	0	0	0	0	1 / 0	1 / 0	• Count select (Y / X): D1 Y (1) / X (0) • Mode select (U / D): D0 UP (1) / DOWN (0)
SZE	0	0	0	1	0	1	Z−address (0 to 25)					• Z−address set
SXE	0	0	0	1	1	0	X−address (0 to 25)					• X−address set
SYE	0	0	0	1	1	1	0	Y−address (0 to 13)				• Y (Page) −address set
STRD	0	1	0	0	86BS	DISP ON	R	0	0	Y / X	U / D	• Status read
DAWR	0	0	1	Write Data								• Display data write
DARD	0	1	1	Read Data								• Display data read
KEYRD1	1	1	0	0	0	BUSY	REQ	KEY DATA (K13 to 0)				• Key data read 1
KEYRD2	1	1	1	KEY DATA (KO7 to 0)								• Key data read 2
KEYCOM	1	0	0	*	*	*	*	*	*	*	1 / 0	• Software reset: D0 Reset ON (1) / Reset OFF (0)

- **Display standby select (DISP: DISPST)**

K / L	R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	0	*	1	Display active (03H, 01H)
0	0	0	0	0	0	0	0	0	0	0	Display standby (00H)

The DISPST bit of command DISP controls display by making it active and standby. When "Display active" is selected, the DISPON bit is enabled, turning display ON or OFF.

Note: If "Display standby" is selected, the LCD drive signal is fixed to V_{SS}.

Note: When using "Display standby", make sure that display is turned OFF (D1 = 0).
When the device is reset, the display is placed in standby state by default.
Before setting to display active, ensure that the booster circuit is enabled.

- **Display ON / OFF select (DISP: DISPON)**

K / L	R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	0	1	1	Display ON (03H)
0	0	0	0	0	0	0	0	0	0	1	Display OFF (01H)

The DISPON bit of command DISP controls display by turning it ON and OFF. Since the display data in RAM is not affected by the DISP command, the display data in RAM is not cleared to 0 s even when display is turned OFF by this command.

Note: Display is turned OFF when the device is reset (by pulling / RESET low).

Display state (DISPON, DISPST)

D1	D0	Display State
0	0	COM / SEG: Fixed to V_{SS}
0	1	Outputs a display OFF level waveform.
1	1	Outputs a display ON level waveform.

- **Word length 8 bits / 6 bits select (BSDT: 86BS)**

K / L	R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	1	0	1	*	Word length 8 bit / Word mode
0	0	0	0	0	0	0	1	0	0	*	Word length 6 bit / Word mode

The 86BS bit of command BSDT sets the word length of the display data stored in display RAM to 8 bits or 6 bits.

Note: When the device is reset, the word length is set to 8 bit / Word mode by default.

- **Duty select (BSDT: DUTY)**

K / L	R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	1	0	*	1	1/26 duty
0	0	0	0	0	0	0	1	0	*	0	1/18 duty

The DUTY bit of command BSDT sets the display duty cycle to 1/26 or 1/18.

Note: When the device is reset, the display duty cycle is set to 1/18 by default.

- **X / Y counter and UP / DOWN mode select (UDE: X / Y and U / D)**

K / L	R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	1	0	0	0	0	0	0	0	X−counter DOWN mode (80H)
0	0	0	1	0	0	0	0	0	0	1	X−counter UP mode (81H)
0	0	0	1	0	0	0	0	0	1	0	Y−counter DOWN mode (82H)
0	0	0	1	0	0	0	0	0	1	1	Y−counter UP mode (83H)

The UDE command selects the display RAM address counter from X−counter or Y−counter when reading and writing display data and specifies whether the selected counter counts the address up or down. Therefore, if you select X−counter UP mode, for example, the X−address is incremented each time the MPU reads or writes to the RAM. On the other hand, the Y−counter is disabled, so the Y (page) −address is set by executing the command SYE.

Note: When the device is reset, the Y−counter UP mode is selected by default.

- **Y (Page) −address set (SYE)**

K / L	R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	1	0	A	A	A	A

Set up range 8 bit / WORD: E0H to E9H (Page 0 to Page 9)
6 bit / WORD: E0H to EDH (Page 0 to Page 13)

The SYE command selects one page from 0 to 9 page display RAM when the word length of display data is set to 8 bit / WORD by the BSDT command or from 0 to 13 page display RAM when the word length is set to 6 bit / WORD. When the selected word length is 8−bit / WORD, make sure that address is always set within 9 pages. When the selected word length is 6−bit / WORD, make sure that address is always set within 13 pages.

Note: When the device is reset, the Y (page) −address is set to page 0 by default.

- **Z−address set (SZE)**

K / L	R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	A	A	A	A	A

Set up range: A0H to B9H (ZAD0 to ZAD25)

The SZE command sets any arbitrary address in the display RAM row as the start line on the LCD screen. For example, setting the Z−address to 13 using the SZE command, the start line on the LCD screen corresponds to Z−address 13 in display RAM and the last line corresponds to Z−address 12.

Note: When the device is reset, the Z−address is set to 0 by default.

- **X−address set (SXE)**

K / L	R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	0	A	A	A	A	A

Set up range: C0H to D9H (XAD0 to XAD25)
The SXE command sets an X−address.

Note: When the device is reset, the X−address is set to 0 by default.

- **Contrast set (CONT: CONT0 to CONT3)**

K / L	R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	*	A	A	A	A

Set up range: 60H to 6FH or 70H to 7FH
The CONT0 to CONT3 bits of command CONT set the display density of the LCD screen. The display density is set in 16 steps, with 60H / 70H the lightest, and 6FH / 7FH the darkest.

Note: When the device is reset, the display density is set to the lightest level of 60H by default.

- **Voltage quadrupler circuit enable (CONT: 4BION)**

K / L	R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	1	1	0	*	*	*	*	Voltage quadrupler circuit disabled
0	0	0	0	1	1	1	*	*	*	*	Voltage quadrupler circuit enabled

The 4BION bit of command CONT controls the voltage quadrupler circuit. When the voltage quadrupler circuit is enabled by this command, its operation is activated, outputting boosted voltage to V1 through V4.

Note: When the device is reset, the voltage quadrupler circuit is disabled by default.

- **Oscillator enable (OSC)**

K / L	R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	1	0	0	0	1	Oscillation enabled (11H)
0	0	0	0	0	0	1	0	0	0	0	Oscillation disabled (10H)

The OSC command controls the operation of the oscillator circuit by enabling or disabling it.
When the oscillator circuit is disabled, the oscillator stops oscillating, so it stops clocking the internal logic of the device.

Note: When the device is reset, the oscillator circuit is enabled by default.

- **Oscillation mode select (OSCM)**

K / L	R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	1	0	0	0	0	0	RC oscillator mode using external resistor (20H)
0	0	0	0	0	1	0	0	0	0	1	External clock supply mode (21H)

The OSCM command determines the operating mode of the oscillator circuit.
Choose the appropriate mode of operation depending on the type of oscillator (RC oscillator with external resistor or external clock).

Note: When the device is reset, the oscillator mode is set to “RC oscillator mode using external resistor” by default.

- **Voltage quadrupler clock select (PUMP)**

K / L	R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	1	0	0	0	0	0	0	Voltage quadrupler clock 1/2 f_{OSC} (40H)
0	0	0	0	1	0	0	0	0	0	1	Voltage quadrupler clock 1/4 f_{OSC} (41H)
0	0	0	0	1	0	0	0	0	1	0	Voltage quadrupler clock 1/8 f_{OSC} (42H)
0	0	0	0	1	0	0	0	0	1	1	Voltage quadrupler clock f_{OSC} (43H)

The PUMP command selects the operating clock for the voltage quadrupler circuit.

Note: When the device is reset, the 1/2 f_{OSC} clock is selected for the voltage quadrupler circuit by default.

- **Status read (STRD)**

K / L	R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	86BS	DISPON	R	0	0	Y / X	U / D

The STRD command lets you know the status of the T6K18.

86BS (word length) : The word length is 8 bit / WORD when 86BS = 1.
The word length is 6 bit / WORD when 86BS = 0.
DISPON (Display) : Display is turned ON when DISPON = 1.
Display is turned OFF when DISPON = 0.
R (Reset) : The device is reset when R = 1.
The device is active (reset deasserted) when R = 0.
Y / X (Counter) : Y (page) −counter is selected when Y / X = 1.
X−counter is selected when Y / X = 0.
U / D (UP / DOWN) : The X / Y counter functions as an up−counter when U / D = 1
The X / Y counter functions as a down−counter when U / D = 0.

- **Write / Read display data**

K / L	R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	1	D	D	D	D	D	D	D	D	DAWR: display data write
0	1	1	D	D	D	D	D	D	D	D	DARD : display data read

The DAWR command writes display data to the predefined address in RAM. The DARD command reads display data from the specified address in RAM.

- **Key input data read (KEYRD1)**

K / L	R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	0	BUSY	REQ	KI3	KI2	KI1	KI0

The KEYRD1 command lets you know the key input data (KI0 to KI3) for the key scan circuit as well as the BUSY status (during key scan) and REQ status (key input).

BUSY (during key scan) : "1" indicates that the key scan circuit is operating.
"0" indicates that the key scan circuit is not operating.

REQ (with key input) : "1" indicates key input. When this key is pressed and the "0" level is input for KI0 to KI3, the key scan circuit automatically determines the key input status. "0" indicates no key input. The REQ flag is output as external signal, allowing confirmation of both hardware and software.

KI0 to KI3 : The key resistor is set to "1" for KI0 to KI3pins with key input after scanned by the key scan circuit. If the KI0 to KI3 pins read with the KEYRD1 command are set to "1", this indicates that there was key input for that pin.

- **Key input data read (KEYRD2)**

K / L	R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	KO7	KO6	KO5	KO4	KO3	KO2	KO1	KO0

The KEYRD2 command lets you know the key output data (KO0 to KO7) for the key scan circuit.
If the KO0 to KO7 pins read with the KEYRD2 command are set to "1", this indicates that the key was pushed for that pin output.
The key scan circuit can be used to automatically scan a key matrix with a maximum of 32 keys. The KEYRD2 command also activates the key scan circuit. The use of this command engages the key scan. For further details, refer to the section on the key scan circuit in the Detailed Description of Functions.

- **Key scan circuit setting (KEYCOM)**

K / L	R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0	
1	0	0	*	*	*	*	*	*	*	1	Reset the software to ON
1	0	0	*	*	*	*	*	*	*	0	Reset the software to OFF

The KEYCOM command resets the software for a key scan circuit. Set D0 to "1" to reset the software. After engaging the reset function, set D0 back to "0".

Detailed Description of Functions

- **X−address counter and Y (page) −address counter**

The following explains how the X−address counter and Y (page) −address counter operate when each specific command is issued. Fig. 11 shows a typical operation of the X−address counter.
After a reset on the device is deasserted, the X−address (XAD) is initialized to XAD = 0. Use the UDE command to select the X−counter UP mode. Next, issue the SXE command to set the X−address to 24. Then read or write data, at which time the X−address counter will be automatically incremented as it counts up. When data is read or written at XAD = 25, the X−address recycles to XAD = 0. Use the UDE command again to select the X−counter DOWN mode this time. Then read or write data, at which time the X−address will be decremented as the counter counts down. When data is read or written at XAD = 0, the X−address recycles to XAD = 25.
At this time, the Y (page) −address counter does not operate.

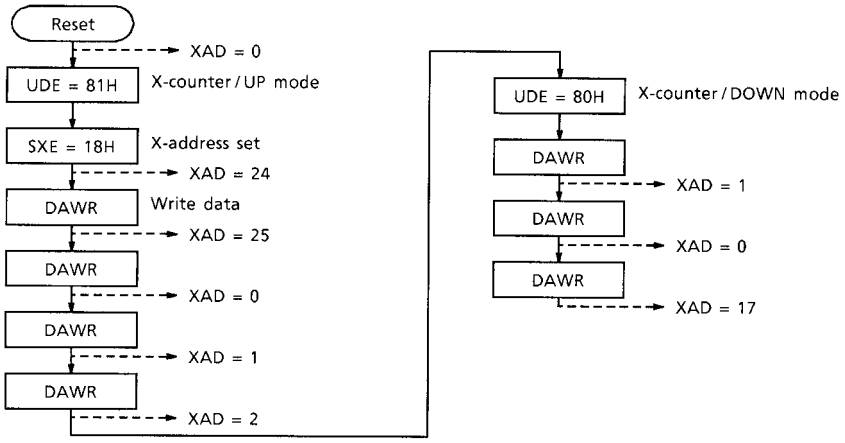


Fig. 11

Fig. 12 shows a typical operation of the Y (page) −address counter when the word length is 8 bit / WORD. After a reset on the device is deasserted, the Y (page) −address (PAGE) is initialized to Page = 0. Use the UDE command to select the Y−counter UP mode and the BSDT command to select the 8 bit / WORD mode. Then read or write data, at which time the Y (page) −address counter will be incremented. When data is read or written at Page = 9, the Y (page) −address recycles to Page = 0. Conversely, if data is read or written when the Y−counter DOWN mode is selected by the UDE command, the Y (page) −address is automatically decremented as the Y (page) −address counter counts down. Then when data is read or written at Page = 0, the Y (page) −address recycles to Page = 9.
At this time, the X−address counter does not operate.

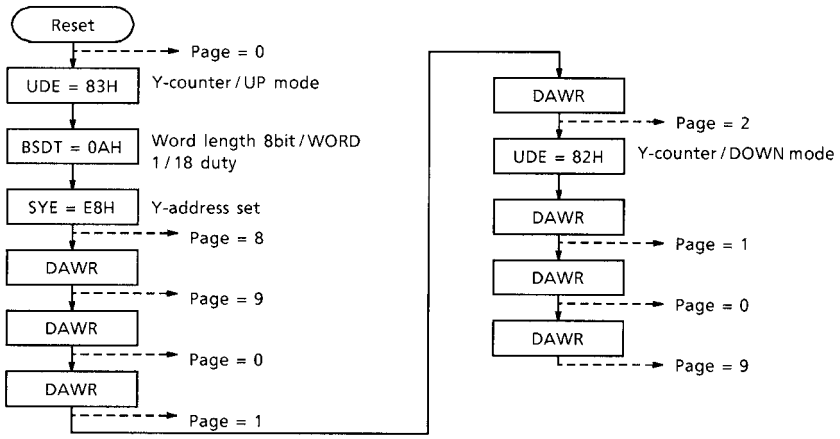


Fig. 12

If the word length is 6 bit / WORD, the Y (page) −address counter is tetra decimal Up / Down counter. Therefore, when data is read or written at Page = 13 in UP mode, the Y (page) −address recycles to Page = 0. When data is read or written at Page = 0 in DOWN mode, the Y (page) −address recycles to Page = 13.

- **Data read**

T6K18 can read display data directly from the display RAM after executing the SYE and SXE commands to set addresses. See Fig. 13.

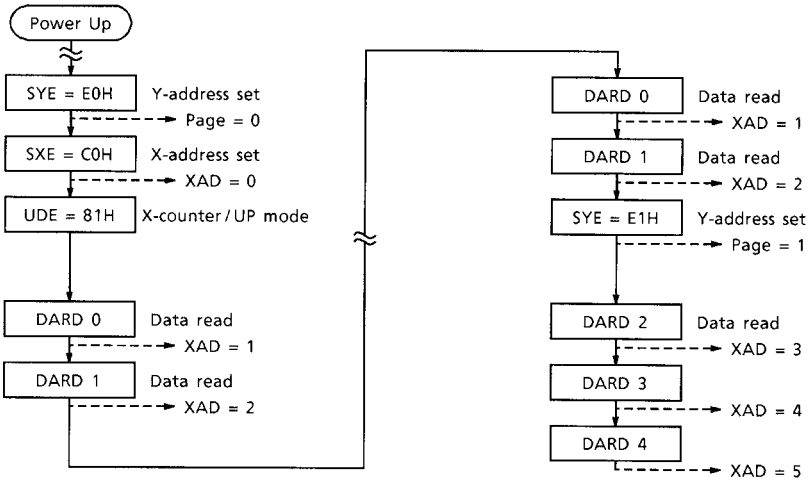


Fig. 13

- **Key scan circuit**

The key scan circuit is comprised of key scan input (KI0 to KI3), key scan output (KO0 to KO7), key scan resistor, key request output (REQ), and key scan display (BUSY). The basic clock in the key scan circuit is input in clock divisions oscillated with the oscillator.
When keys are input for the key scan input (KI0 to KI3), a transition of the internal 1 kHz key check signal occurs. After detecting a key pressed three continuous times, H is output from the key request (REQ), and lets you know that key input occurred for the external MPU.
To activate the key scan circuit, use the key input data read command (KEYRD2). This command activates the key scan circuit, automatically outputs the scan signal from the key scan output (KO0 to KO7), and incorporates the key data. The key scan status is stored in the key scan output resistor (8−bit) and key scan input resistor (4−bit).
During key scan, "1" is set for the BUSY flag of the 8 bit data read with the KEYRD1 command. The key data is not at correct values when BUSY flag is set to "1", so read the correct key data after confirming that BUSY flag is set to "0". When using the key input data read command (KEYRD2) to activate the key scan circuit, note that the key data read with the initial KEYRD2 command will be invalid (Dummy read). The key data will also be invalid when BUSY flag is set to "1".

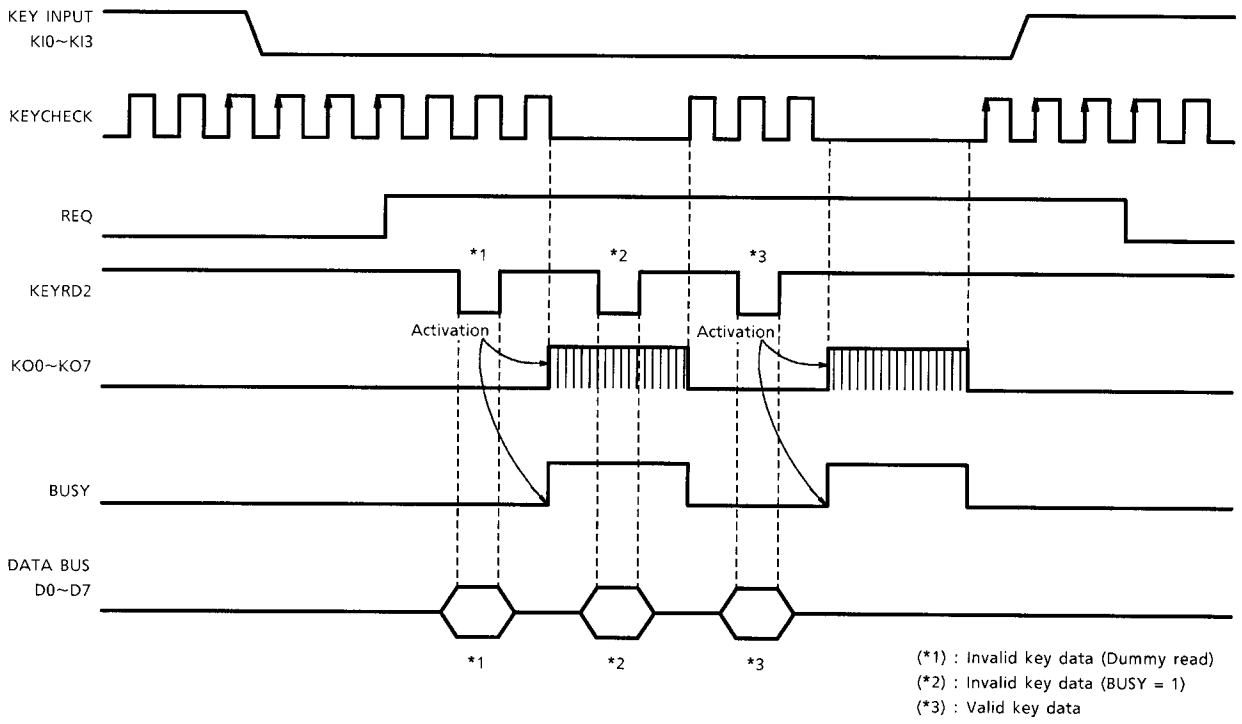


Fig. 14 Key scan operation (1)

Note: The above diagram is constructed to display the various signals in an easy−to−understand format. It does not reflect the exact timing.

- **Key scan timing**

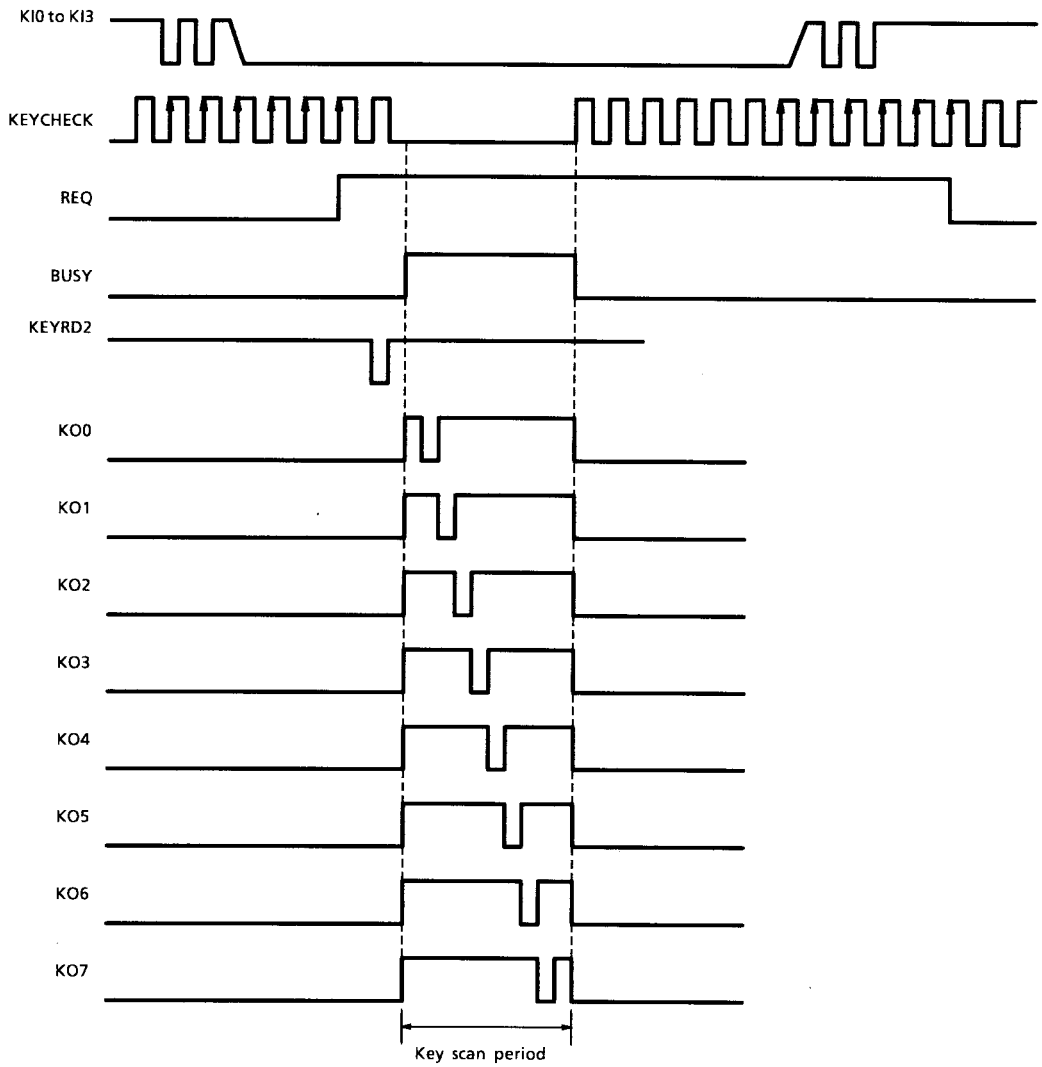
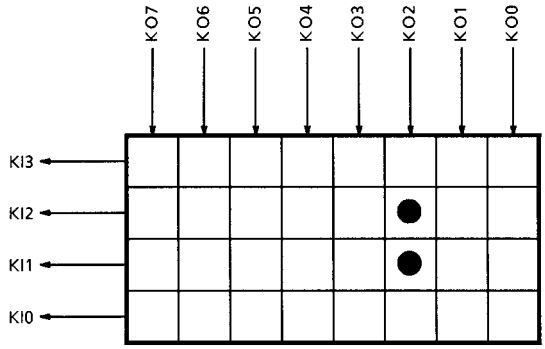


Fig. 15 Key scan operation (2)

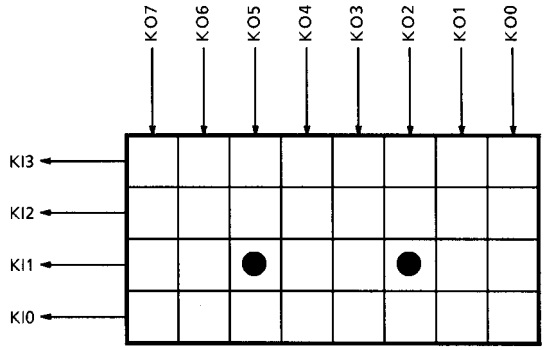
The relationship of the key check frequency and key scan period with T6K18 oscillation frequency (f_{osc}) is represented with the following equation:

$$\text{Key check frequency } f_{(KEYCHECK)\ [Hz]} = fosc \times \frac{1}{32}$$

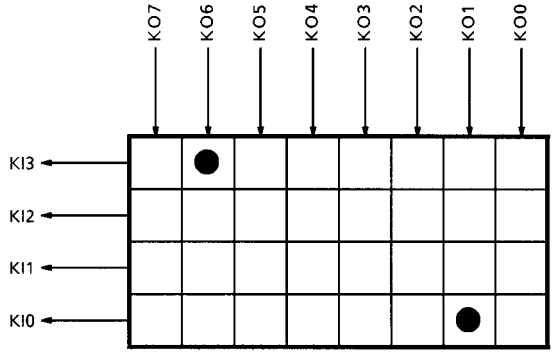
- **Examples of key data read (● mark denotes pressed key.)**



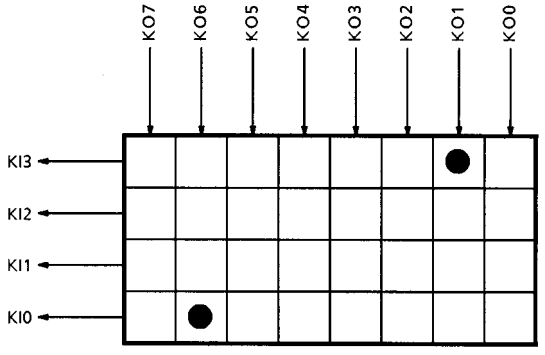
COMMAND	D7	D6	D5	D4	D3	D2	D1	D0
KEYRD1	0	0	*	1	0	1	1	0
KEYRD2	0	0	0	0	0	1	0	0



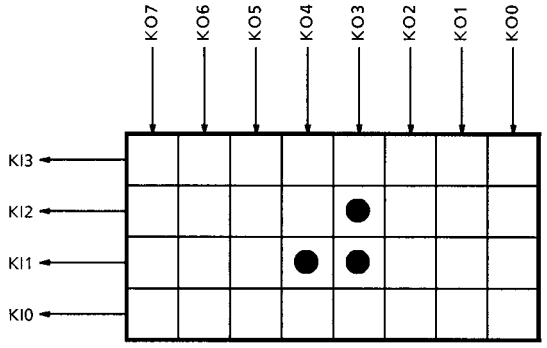
COMMAND	D7	D6	D5	D4	D3	D2	D1	D0
KEYRD1	0	0	*	1	0	0	1	0
KEYRD2	0	0	1	0	0	1	0	0



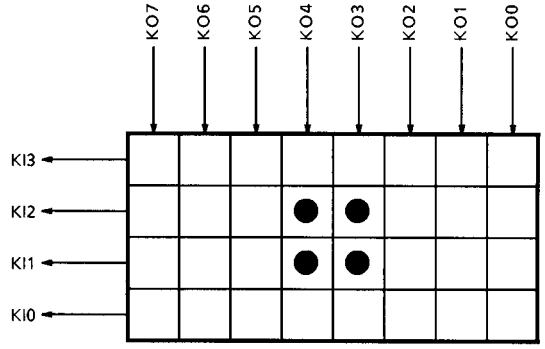
COMMAND	D7	D6	D5	D4	D3	D2	D1	D0
KEYRD1	0	0	*	1	1	0	0	1
KEYRD2	0	1	0	0	0	0	1	0



COMMAND	D7	D6	D5	D4	D3	D2	D1	D0
KEYRD1	0	0	*	1	1	0	0	1
KEYRD2	0	1	0	0	0	0	1	0

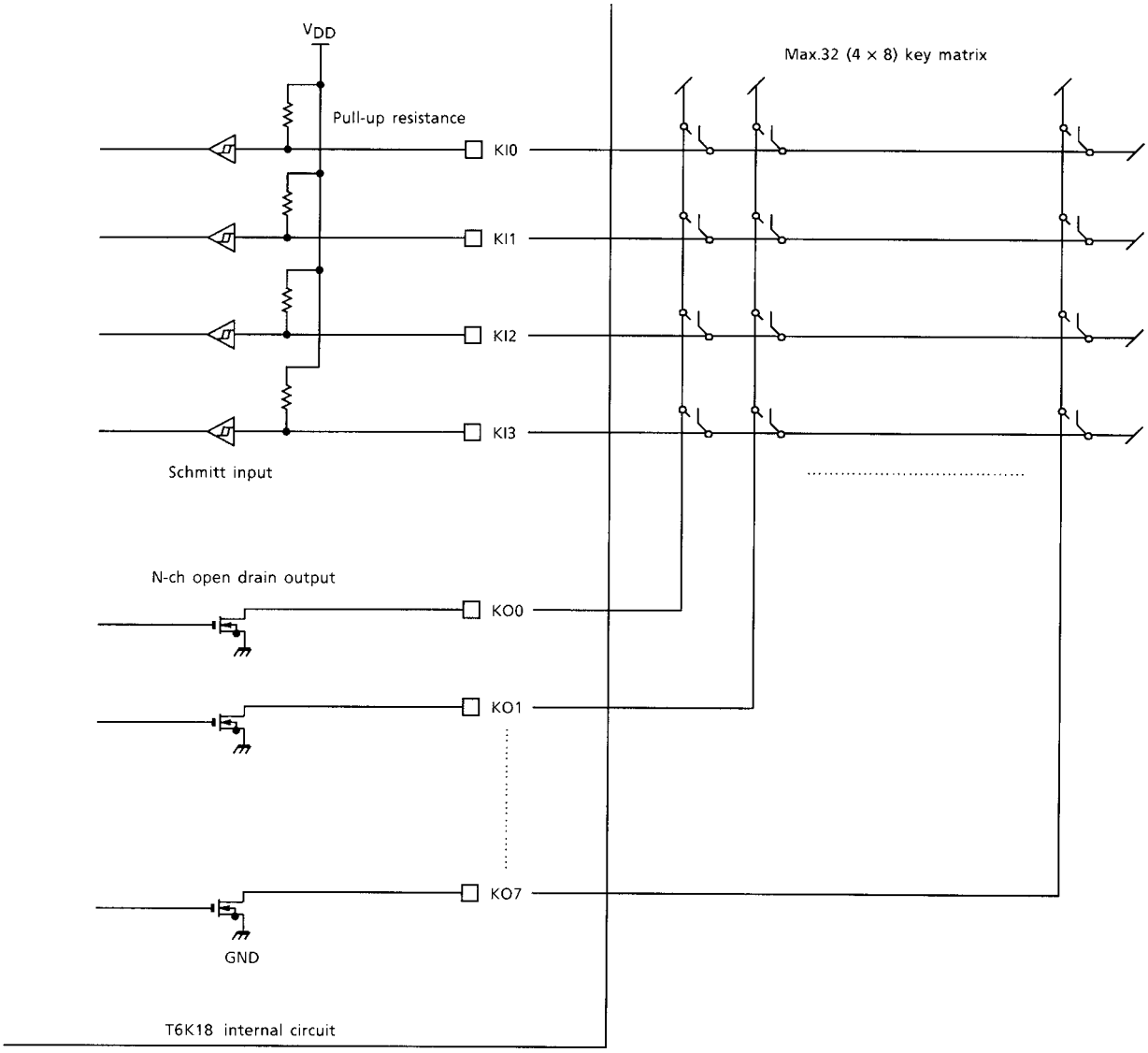


COMMAND	D7	D6	D5	D4	D3	D2	D1	D0
KEYRD1	0	0	*	1	0	1	1	0
KEYRD2	0	0	0	1	1	0	0	0



COMMAND	D7	D6	D5	D4	D3	D2	D1	D0
KEYRD1	0	0	*	1	0	1	1	0
KEYRD2	0	0	0	1	1	0	0	0

- **Key scan circuit input / output configuration**



- When there is no key input (key is not pressed), KO0 to KO7 will output at "0" level (N−ch open drain output). KI0 to KI3 input at "1" level with pull−up resistance.
- If any keys are pressed, KI0 to KI3 will input at "0" level, and detect if the key on the key scan circuit is pressed.
- The key scan circuit does not eliminate key−on chatter or key−off chatter. Nor does the circuit detect multiple pressings of buttons. After reading the key scan input or output registers from the control MPU, determine the status by the MPU.

● Reset function

The T6K18 has a reset input pin designated as / RESET. A low on this input resets the T6K18 and its internal circuits are initialized as follows

- Display ..... Standby
- Duty cycle..... 1/18 duty
- Word length..... 8 bit / WORD
- Counter..... Y−counter / UP mode
- Y (Page) −address counter..... Page = 0
- X−address counter ..... Xad = 0
- Z−address counter..... Zad = 0
- Key scan input register..... 0 h
- Key scan output register ..... 00 h
- Voltage step−up circuit ..... Disabled; step−up clock = 1/2 f_{OSC}
- Contrast..... Minimum
- Oscillation ..... External clock is fed to the device.

*: Please be sure to execute Reset Function at the time of a power−supply.

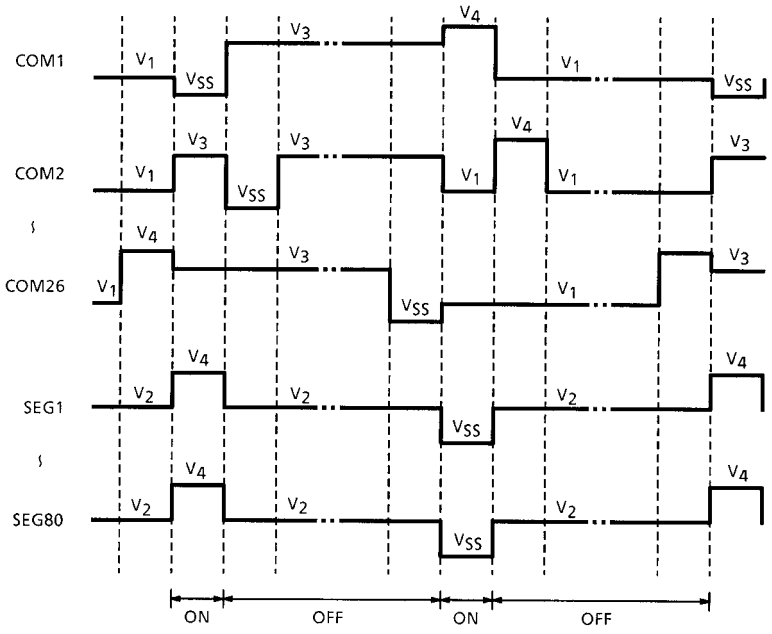
● About oscillation frequency

The T6K18 have a command named OSCM that allows you to choose the operating clock for the device from the built−in RC oscillator (using an external resistor) or an external clock source.
The equations below show the relationship between the oscillation frequency (f_{OSC}) and frame frequency (f_F):

$$f_F\ [Hz] = f_{OSC} \times \frac{1}{416}$$ (when operating with 1/26 duty)

$$f_F\ [Hz] = f_{OSC} \times \frac{1}{432}$$ (when operating with 1/18 duty)

- **LCD driver waveform**



LCD drive timing chart (1/26 duty)

Maximum Ratings

Item	Symbol	Rating	Unit
Power Supply Voltage	V_{DD} (Note)	−0.3 to 6.0	V
Input Voltage	V_{IN} (Note)	−0.3 to V_{DD} + 0.3	V
Operating Temperature	Topr	−20 to 75	°C
Storage Temperature	T_{stg}	−40 to 125	°C

Note: Referred to V_{SS} = 0 V.

Electrical Characteristics (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 1.8~5.5 V, Ta = 25°C)

Characteristic		Symbol	Test Circuit	Condition	Min	Typ.	Max	Unit	Pin Name
Operating Voltage		V_{DD}	—	—	1.8	3.0	5.5	V	V_{DD}
Input Voltage 1	H Level	V_{IH1}	—	—	V_{DD} × 0.80	—	V_{DD}	V	D0 to D7,/ CE, R / W, K / L, D / I
	L Level	V_{IL1}	—	—	V_{SS}	—	V_{DD} × 0.20		
Input Voltage 2	H Level	V_{IH2}	—	—	V_{DD} × 0.80	—	V_{DD}	V	KI0 to KI3 / RESET
	L Level	V_{IL2}	—	—	V_{SS}	—	V_{DD} × 0.20		
Output Current		I_{OH}	—	V_{OUT} = V_{DD} − 0.5 V	—	—	−0.8	mA	D0 to D7, REQ
		I_{OL}	—	V_{OUT} = 0.5 V	0.8	—	—		D0 to D7, REQ KO0 to KO7
Input Leakage Current		I_{IH}	—	V_{IN} = V_{DD} to V_{SS}	−5	—	5	μA	D0 to D7, / CE, R / W, P / S, K / L, D / I KI0 to KI3 TEST1, TEST2
		I_{IL}	—	V_{IN} = V_{DD} to V_{SS}	−5	—	5		
Operating Frequency		f_{OSC}	—	—	30	33	66	kHz	RIN
External Clock Frequency		f_{ex}	—	—	30	33	66	kHz	RIN
External Clock Duty		f_{duty}	—	—	45	50	55	%	RIN
External Clock Uptime		f_{tr}	—	—	—	—	50	ns	RIN
External Clock Downtime		f_{tf}	—	—	—	—	50	ns	RIN
Current Consumption (1)		I_{rst} I_{hlt1}	—	Display OFF, V_{DD} = 3.0 V f_{osc} = 33 kHz	—	6	12	μA	V_{DD}
Current Consumption (2)		I_{dsp} I_{hlt2}	—	Display ON, V_{DD} = 3.0 V f_{OSC} = 33 kHz, V−quad clock = 1/2 f_{OSC} Contrast 7	—	20	32	μA	V_{DD}

Note: V−quad: Voltage quadrupler

Characteristic	Symbol	Test Circuit	Condition	Min	Typ.	Max	Unit	Pin Name
Current Consumption (3)	I_{stp}	—	V_{DD} = 3.0 V	—	1.0	3.0	μA	V_{DD}
Current Consumption (4)	I_{run}	—	V_{DD} = 3.0 V Tcyc = 100 kHz During data access	—	40	80	μA	V_{DD}
Pull−up Resistance (1)	R_{pu1}	—	V_{OUT} = V_{SS}	30	60	90	kΩ	/ RESET
Pull−up Resistance (2)	R_{pu2}	—	V_{OUT} = V_{SS}	30	60	90	kΩ	KI0 to KI3
Pull−down Resistance	R_{pd}	—	V_{OUT} = V_{DD}	50	100	150	kΩ	TEST1, TEST2
Common Output Current	IOM1	—	V_{OUT} = V3 − 0.5 V	—	—	−250	μA	COM1 to COM26
	IOM2	—	V_{OUT} = V1 + 0.5 V	250	—	—		
	IOH	—	V_{OUT} = V4 − 0.5 V	—	—	−250		
	IOL	—	V_{OUT} = 0.5 V	250	—	—		
Segment Output Current	IOM3	—	V_{OUT} = V2 + 0.5 V	150	—	—	μA	SEG1 to SEG80
	IOM3	—	V_{OUT} = V2 − 0.5 V	—	—	−150		
	IOH	—	V_{OUT} = V4 − 0.5 V	—	—	−150		
	IOL	—	V_{OUT} = 0.5 V	150	—	—		
Step−up Output Voltage	V_O	—	Select Contrast 7 CONT [3: 0] = 0111	1.115	1.165	1.215	V	V1
		—	Select Contrast 7 CONT [3: 0] = 0111	2.23	2.33	2.43		V2
		—	Select Contrast 7 CONT [3: 0] = 0111	3.35	3.50	3.65		V3
		—	Select Contrast 7 CONT [3: 0] = 0111	4.46	4.66	4.86		V4
CR Oscillating Exterior Resistance	R_{OSC}	—	When V_{DD} = 3.0 and f_{OSC} = 33 kHz	—	560	—	kΩ	RIN

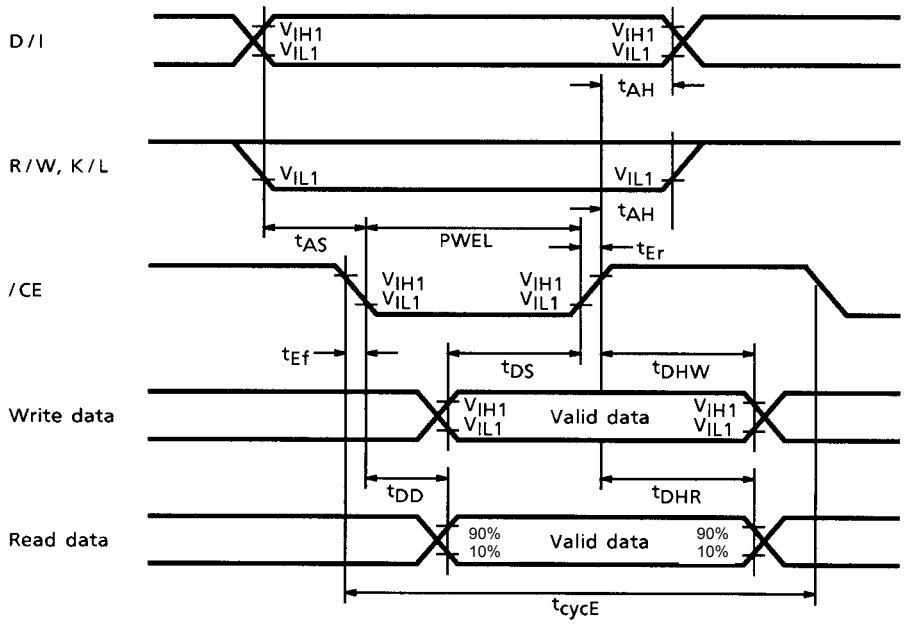
Contrast Level 4V Characteristic

Characteristic	Symbol	Test Circuit	Condition	Min	Typ.	Max	Unit	Pin Used
Set−up Output Voltage	V_O	—	Select contrast 15 CONT [3: 0] = 1111	5.04	5.24	5.44	V	V4
		—	Select contrast 14 CONT [3: 0] = 1110	4.97	5.17	5.37		
		—	Select contrast 13 CONT [3: 0] = 1101	4.90	5.10	5.30		
		—	Select contrast 12 CONT [3: 0] = 1100	4.82	5.02	5.22		
		—	Select contrast 11 CONT [3: 0] = 1011	4.75	4.95	5.15		
		—	Select contrast 10 CONT [3: 0] = 1010	4.68	4.88	5.08		
		—	Select contrast 9 CONT [3: 0] = 1001	4.61	4.81	5.01		
		—	Select contrast 8 CONT [3: 0] = 1000	4.53	4.73	4.93		
		—	Select contrast 7 CONT [3: 0] = 0111	4.46	4.66	4.86		
		—	Select contrast 6 CONT [3: 0] = 0110	4.39	4.59	4.79		
		—	Select contrast 5 CONT [3: 0] = 0101	4.31	4.51	4.71		
		—	Select contrast 4 CONT [3: 0] = 0100	4.24	4.44	4.64		
		—	Select contrast 3 CONT [3: 0] = 0011	4.16	4.36	4.56		
		—	Select contrast 2 CONT [3: 0] = 0010	4.09	4.29	4.49		
		—	Select contrast 1 CONT [3: 0] = 0001	4.01	4.21	4.41		
		—	Select contrast 0 CONT [3: 0] = 0000	3.93	4.13	4.33		

Reference Materials

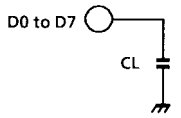
Characteristic	Symbol	Test Circuit	Condition	Voltage Quadrupler Clock			Unit
				1/8 f_{OSC} Typ.	1/4 f_{OSC} Typ.	f_{OSC} Typ.	
Current consumption (2)	I_{HALT} (2)	—	With display on: V_{DD} = 3.0 (V) f_{osc} = 33 kHz Select contrast 7 CONT [3: 0] = 0111	10	12	25	μA

AC Characteristics (V_{SS} = 0 V, V_{DD} = 3.0 V ± 10%, V4 = 4.66 V, Ta = 25°C)



Characteristic	Symbol	Min	Max	Unit
Enable Cycle Time	t_{cycE}	550	—	ns
Read Enable Pulse Width	PWEL (RD)	330	—	ns
Write Enable Pulse Width	PWEL (WR)	180	—	ns
Enable Rise / Fall Times	t_{Er}, t_{Ef}	—	25	ns
Address Set Up Time	t_{AS}	40	—	ns
Address Hold Time	t_{AH}	20	—	ns
Data Set Up Time	t_{DS}	100	—	ns
Write Data Hold Time	t_{DHW}	20	—	ns
Data Delay Time	t_{DD} (Note)	—	250	ns
Read Data Hold Time	t_{DHR} (Note)	20	—	ns

Load Circuit



CL = 100 pF (including jig capacitance)

Note: Values for t_{DD} and t_{DHR} are measured after adding a load circuit like the one shown on the right.

● Precautions for designing

When designing your system, please take the following precautions.

(1) Operation of this product is guaranteed when supply voltage V_{DD} = 1.8 to 5.5 V. If V_{DD} is set to the V_{SS} level or open (cut off), operation is not guaranteed.

(2) Operation of the product is guaranteed with supply voltage V_{DD} on. Power must not be set to off.

(3) After power is cut off, completely discharging the capacitors takes time. The capacitors retain middle voltage levels V1 to V4 used to drive the display. Thus, occasionally, voltage may be instantaneously output to the segment pins (SEG1 to 80) or common pins (COM1 to 26), lighting the display.

(4) To cut power off (0 V or open), set T6K18 as follows:

1: Set all data in display RAM to 0.

2: Set to PUMP OFF.

3: Allow enough discharging time. (1 sec or more)

4: Cut power off.

Even if the above steps are taken, the phenomenon described in (3) may occur. Please configure an adequate system and evaluate it carefully.

● Precautions when used in combination with LCD panel

When using the device in combination with an LCD panel, please take the following precautions.
In general, the lit voltage Vop of the LCD panel and the lit voltage V4 of the device are subject to variations in manufacture. When the worst possible voltages are combined, the display may be lighter or darker. TOSHIBA recommends you check the display quality of actual displays as well as comparing Vop and V4 with standards. The worst possible combinations are as follows:

Vop (mix) −V4 (max): Display may be dark.

Vop (max) −V4 (min): Display may be light.

For V4 reference variation values, see the contrast values (CONT15 to CONT0) in Table 1.

● Precautions on data bus termination

The data bus of the device is CMOS input. If the data are floating, overlap current may be generated at input. Terminate (eg, pull−up resistor, pull−down resistor, bus holder) in order to satisfy the VIH and VIL specifications of the device.

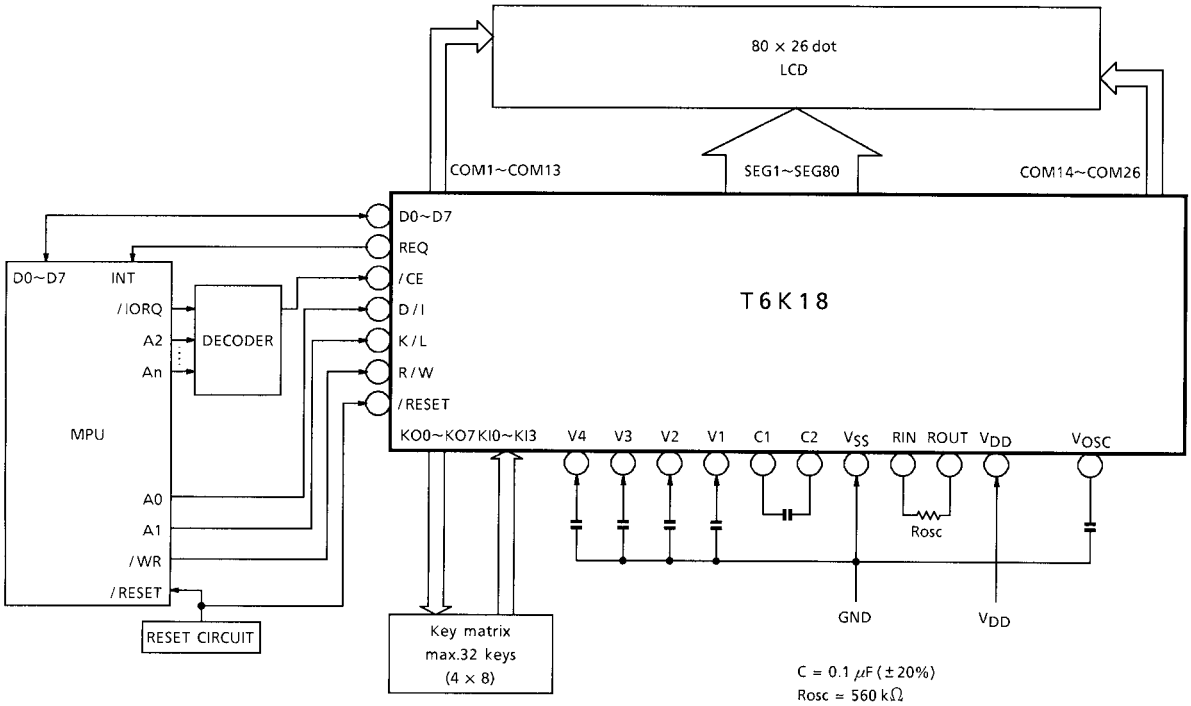
● Instruction for operating circumstances

If light is given to semiconductor devices, electromotive force is generated due to photoelectric effect, and they may malfunction.
Especially, devices whose dies are seen from outside are easily influenced. Please make sure with your design that external light does not come inside.
Please note semiconductors other than optical devices and EPROM may also be influenced.

● Example of application circuit

This application circuit for the T6K18 uses

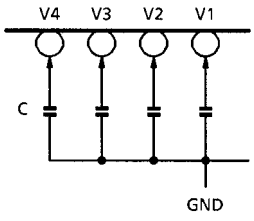
- RC oscillator using an external resistor
- Using DC−DC converter (Quadrupler)



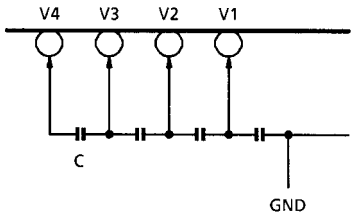
● How to connect booster capacitor

With T6K18, an external booster capacitor (for V1 to V4) can be connected in parallel or series. Shown below are connection examples. Compared with the in−parallel connection, the in−series connection has a total charge amount (Q) of 2/5; however, the current capacity of the pins is about the same.
If power may be cut to T6K18 in an application system, Toshiba recommends in−series connection.

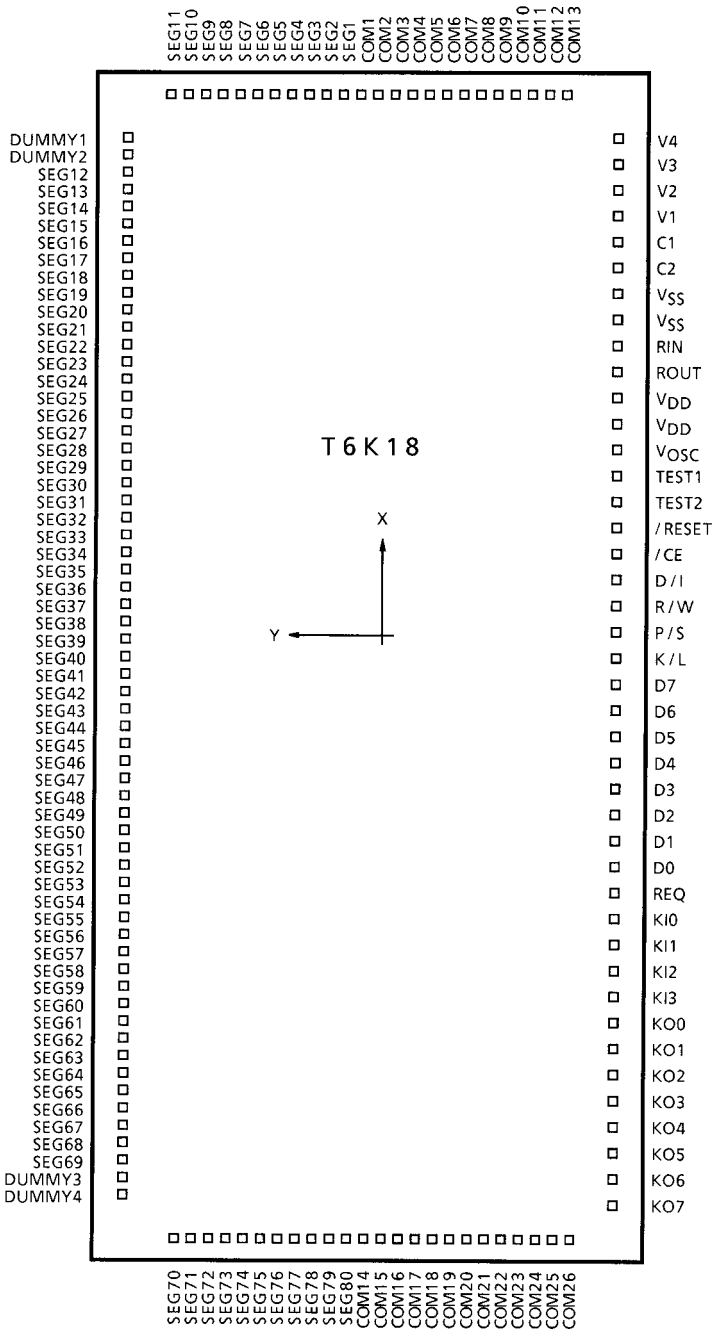
[In−parallel connection]



[In−series connection]



- **PAD layout**


SEG11 SEG10 SEG9 SEG8 SEG7 SEG6 SEG5 SEG4 SEG3 SEG2 SEG1 COM1 COM2 COM3 COM4 COM5 COM6 COM7 COM8 COM9 COM10 COM11 COM12 COM13
DUMMY1 DUMMY2 SEG12 SEG13 SEG14 SEG15 SEG16 SEG17 SEG18 SEG19 SEG20 SEG21 SEG22 SEG23 SEG24 SEG25 SEG26 SEG27 SEG28 SEG29 SEG30 SEG31 SEG32 SEG33 SEG34 SEG35 SEG36 SEG37 SEG38 SEG39 SEG40 SEG41 SEG42 SEG43 SEG44 SEG45 SEG46 SEG47 SEG48 SEG49 SEG50 SEG51 SEG52 SEG53 SEG54 SEG55 SEG56 SEG57 SEG58 SEG59 SEG60 SEG61 SEG62 SEG63 SEG64 SEG65 SEG66 SEG67 SEG68 SEG69 DUMMY3 DUMMY4
V4 V3 V2 V1 C1 C2 VSS VSS RIN ROUT VDD VDD VOSC TEST1 TEST2 /RESET /CE D/I R/W P/S K/L D7 D6 D5 D4 D3 D2 D1 D0 REQ KI0 KI1 KI2 KI3 KO0 KO1 KO2 KO3 KO4 KO5 KO6 KO7
T6K18
X
Y
SEG70 SEG71 SEG72 SEG73 SEG74 SEG75 SEG76 SEG77 SEG78 SEG79 SEG80 COM14 COM15 COM16 COM17 COM18 COM19 COM20 COM21 COM22 COM23 COM24 COM25 COM26

PAD Arrangement Diagram

Scribe width : (80 140) μm
Chip size : 6110 × 2720 μm
Chip thickness : 450 ± 50 μm

Unit: (μm)

No.	PAD Name	X Point	Y Point
1	KO7	−2670	−1207
2	KO6	−2535	−1207
3	KO5	−2405	−1207
4	KO4	−2275	−1207
5	KO3	−2145	−1207
6	KO2	−2015	−1207
7	KO1	−1885	−1207
8	KO0	−1755	−1207
9	KI3	−1625	−1207
10	KI2	−1495	−1207
11	KI1	−1365	−1207
12	KI0	−1235	−1207
13	REQ	−1105	−1207
14	D0	−975	−1207
15	D1	−845	−1207
16	D2	−715	−1207
17	D3	−585	−1207
18	D4	−455	−1207
19	D5	−325	−1207
20	D6	−195	−1207
21	D7	−65	−1207
22	K / L	65	−1207
23	P / S	195	−1207
24	R / W	325	−1207
25	D / I	455	−1207
26	/ CE	585	−1207
27	/ RESET	715	−1207
28	TEST2	845	−1207
29	TEST1	975	−1207
30	VOSC	1105	−1207
31	VDD	1235	−1207
32	VDD	1365	−1207
33	ROUT	1495	−1207
34	RIN	1625	−1207
35	VSS	1755	−1207
36	VSS	1885	−1207
37	C2	2015	−1207
38	C1	2145	−1207

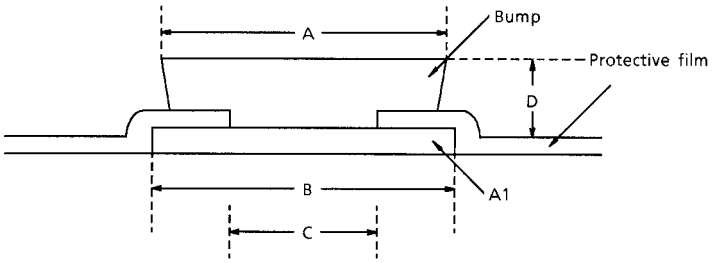
No.	PAD Name	X Point	Y Point
39	V1	2275	−1207
40	V2	2405	−1207
41	V3	2535	−1207
42	V4	2665	−1207
43	COM13	2933	−914
44	COM12	2933	−829
45	COM11	2933	−749
46	COM10	2933	−669
47	COM9	2933	−589
48	COM8	2933	−509
49	COM7	2933	−429
50	COM6	2933	−349
51	COM5	2933	−269
52	COM4	2933	−189
53	COM3	2933	−109
54	COM2	2933	−29
55	COM1	2933	51
56	SEG1	2933	131
57	SEG2	2933	211
58	SEG3	2933	291
59	SEG4	2933	371
60	SEG5	2933	451
61	SEG6	2933	531
62	SEG7	2933	611
63	SEG8	2933	691
64	SEG9	2933	771
65	SEG10	2933	851
66	SEG11	2933	936
67	DUMMY1	2720	1207
68	DUMMY2	2626	1207
69	SEG12	2537	1207
70	SEG13	2448	1207
71	SEG14	2359	1207
72	SEG15	2270	1207
73	SEG16	2181	1207
74	SEG17	2092	1207
75	SEG18	2003	1207
76	SEG19	1914	1207

No.	PAD Name	X Point	Y Point
77	SEG20	1825	1207
78	SEG21	1736	1207
79	SEG22	1647	1207
80	SEG23	1558	1207
81	SEG24	1469	1207
82	SEG25	1380	1207
83	SEG26	1291	1207
84	SEG27	1202	1207
85	SEG28	1113	1207
86	SEG29	1024	1207
87	SEG30	935	1207
88	SEG31	846	1207
89	SEG32	757	1207
90	SEG33	668	1207
91	SEG34	579	1207
92	SEG35	490	1207
93	SEG36	401	1207
94	SEG37	312	1207
95	SEG38	223	1207
96	SEG39	134	1207
97	SEG40	45	1207
98	SEG41	−45	1207
99	SEG42	−134	1207
100	SEG43	−223	1207
101	SEG44	−312	1207
102	SEG45	−401	1207
103	SEG46	−490	1207
104	SEG47	−579	1207
105	SEG48	−668	1207
106	SEG49	−757	1207
107	SEG50	−846	1207
108	SEG51	−935	1207
109	SEG52	−1024	1207
110	SEG53	−1113	1207
111	SEG54	−1202	1207
112	SEG55	−1291	1207
113	SEG56	−1380	1207
114	SEG57	−1469	1207

No.	PAD NAME	X Point	Y Point
115	SEG58	−1558	1207
116	SEG59	−1647	1207
117	SEG60	−1736	1207
118	SEG61	−1825	1207
119	SEG62	−1914	1207
120	SEG63	−2003	1207
121	SEG64	−2092	1207
122	SEG65	−2181	1207
123	SEG66	−2270	1207
124	SEG67	−2359	1207
125	SEG68	−2448	1207
126	SEG69	−2537	1207
127	DUMMY3	−2626	1207
128	DUMMY4	−2720	1207
129	SEG70	−2933	936
130	SEG71	−2933	851
131	SEG72	−2933	771
132	SEG73	−2933	691
133	SEG74	−2933	611
134	SEG75	−2933	531
135	SEG76	−2933	451
136	SEG77	−2933	371
137	SEG78	−2933	291
138	SEG79	−2933	211
139	SEG80	−2933	131
140	COM14	−2933	51
141	COM15	−2933	−29
142	COM16	−2933	−109
143	COM17	−2933	−189
144	COM18	−2933	−269
145	COM19	−2933	−349
146	COM20	−2933	−429
147	COM21	−2933	−509
148	COM22	−2933	−589
149	COM23	−2933	−669
150	COM24	−2933	−749
151	COM25	−2933	−829
152	COM26	−2933	−914

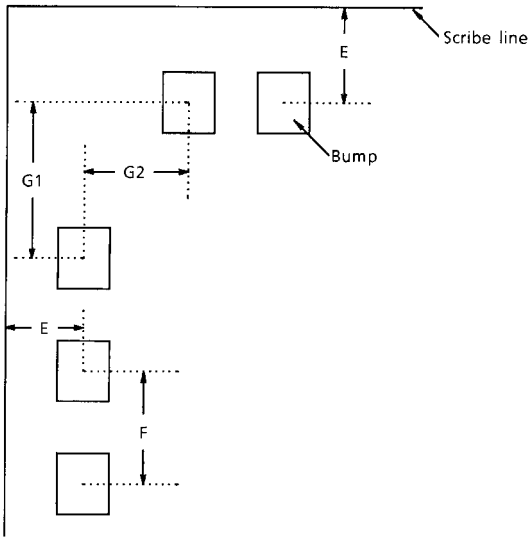
- **Shape of bump chip**

1. Au bump shape



	Characteristics	Ratings
1	A (Bump size)	53 to 77 μm 65 μm (typ.)
2	B (A1 size)	70 μm (typ.)
3	C (Protective film aperture size)	35 μm (typ.)
4	D (Bump height)	12 to 20 μm 16 μm (typ.)
5	Gold bump height variation per chip	±3 μm
6	Gold bump strength (Adhesive strength)	≥ 20 g
7	Gold bump hardness	30 to 80 HV (Vickers hardness tester)

2. Bump layout



	Characteristics	Ratings
8	E Bump center to scribe line distance	min 80 μm
9	F Bump pitch	min 80 μm
10	G Corner pad arrangement (either G1 or G2)	min 130 μm

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000707EBE

- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
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- Light striking a semiconductor device generates electromotive force due to photoelectric effects. In some cases this can cause the device to malfunction.
  This is especially true for devices in which the surface (back), or side of the chip is exposed. When designing circuits, make sure that devices are protected against incident light from external sources. Exposure to light both during regular operation and during inspection must be taken into account.
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