TOSHIBA CMOS Digital Integrated Circuits Silicon Monolithic

T6L52

Gate Driver for TFT LCD Panel

The T6L52 is a 258-channel output gate driver for TFT LCD panels. In addition to three output voltage levels available, this device accepts external input of the panel drive voltage. These features make this device ideal for the S-XGA and XGA-compatible TFT LCD panel drive systems.

The T6L52 offers high integration circuit due to CMOS technology.

Unit: mm

T6L52	User Area Pitch	
	IN	OUT

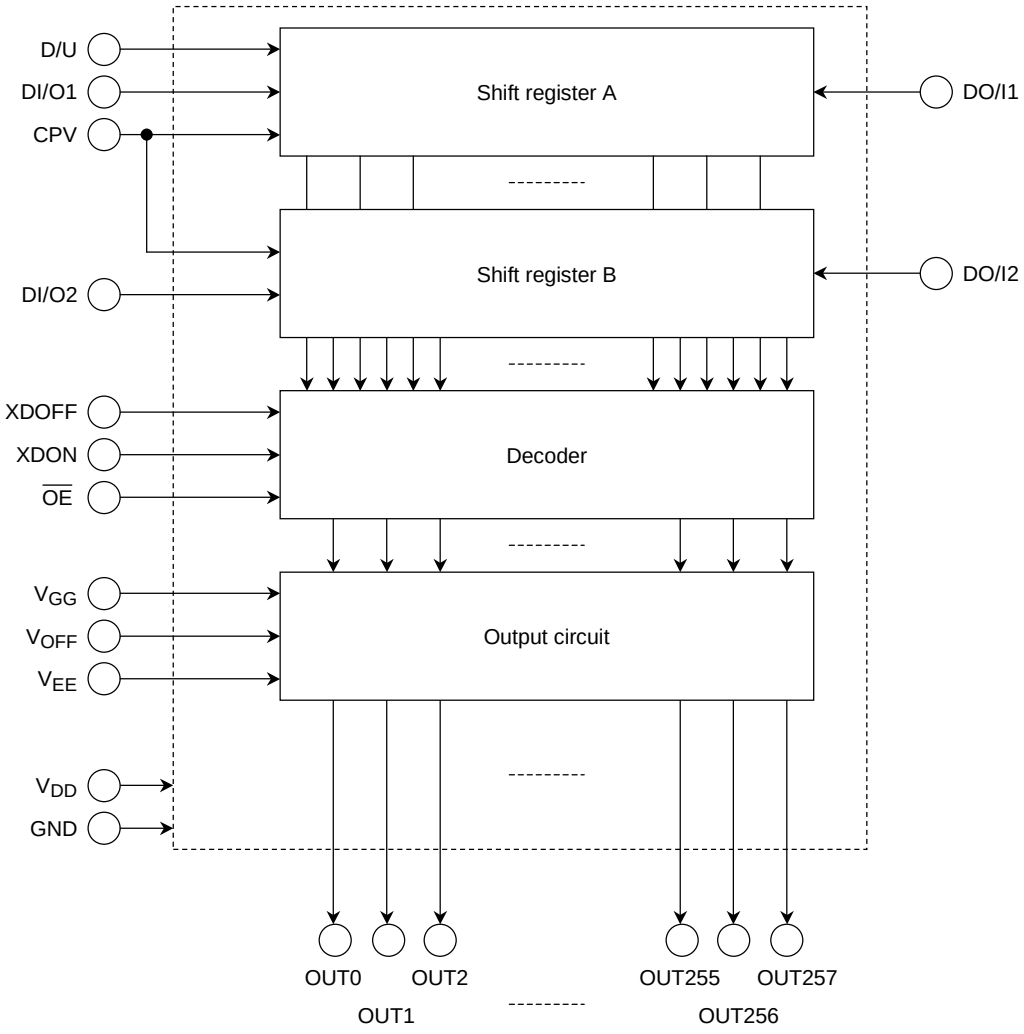
Please contact Toshiba or an authorized Toshiba dealer for the latest TCP specification and product lineup.

TCP (Tape Carrier Package)

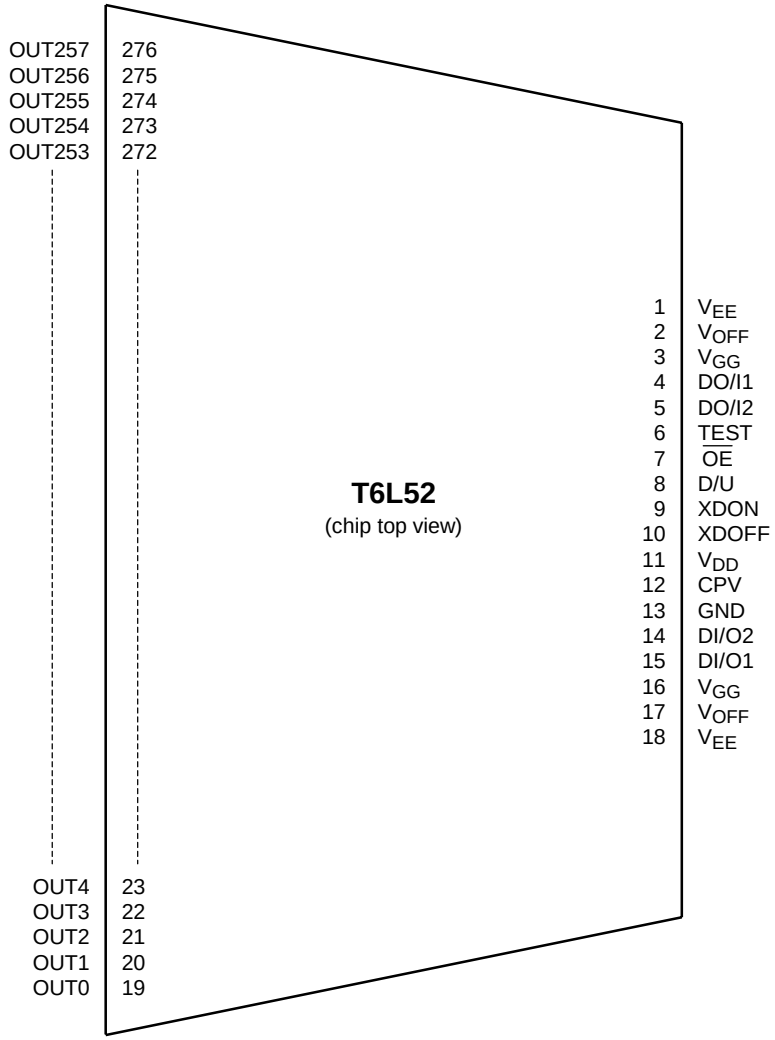
Features

- LCD drive output pins: 258 pins (including two dummy line drive channels)
- Data transfer method : Bidirectional shift register
- Package : Tape carrier package (TCP)
- Built-in input signal level-shifting circuit

Block Diagram



Pin Assignment



The above diagram shows the device's pin configuration only and does not necessarily correspond to the pad layout on the chip. Please contact Toshiba or our distributors for the latest TCP specification.

Pin Description

Pin Name	I/O	Function
DI/O1 DO/I1 DI/O2 DO/I2	I/O	Vertical shift data input/output pins These pins are used to input and output shift data. The function of these pins is switched for input or output by D/U as shown below. When set for input The data is latched into the internal shift registers synchronously with the rising edge of CPV. When set for output When two or more T6L52s are cascaded, this pin outputs the data to be fed into the next stage.
D/U	I	Transfer direction select pin This pin specifies the direction in which data is transferred through the shift registers. When D/U = Low, data is shifted in the direction D/U = "L": OUT0 → OUT1 → OUT3 ⋯ → OUT256 → OUT257 When D/U=High, the direction is reversed to give. D/U = "H": OUT257 → OUT256 → OUT255 ⋯ → OUT1 → OUT0 The voltage applied to this pin must be a DC-level voltage that is either High (V_{DD}) or Low (GND).
CPV	I	Vertical shift clock This is the shift clock for the shift registers. The data in shift registers A and B are shifted synchronously with each rising edge of CPV.
$\overline{OE}$	I	Output-fixing input pin When $\overline{OE}$ = High, the LCD drive output V_{GG} level is fixed to V_{EE} while CPV is High. This pin is only valid during the V_{GG} level output. The voltage applied to this pin must be a DC-level voltage that is either V_{DD} or GND.
XDOFF	I	Display-OFF input pin When XDOFF = Low, the V_{OFF} voltage is output all output pins irrespective of the shift data and the content of input data. However, this does not cause the contents of the shift registers to be cleared. XDOFF operates asynchronously with CPV.
XDON	I	Display-ON input pin When XDON = Low, the V_{GG} voltage is output all output pins irrespective of the shift data and the content of input data. However, this does not cause the contents of the shift registers to be cleared. XDON does not operate asynchronously with CPV. XDON is pull-up registered to V_{DD}. Note: If XDON = Low, it must be $V_{GG} - V_{EE}$ = below 38 V. Connect the external resistor above 62 Ω to V_{GG} line, and above 100 Ω to V_{OFF} line. Please contact a Toshiba dealer before using this pin.
TEST	I	Test pin Leave this pin open.
OUT0 to OUT257	O	LCD panel drive pins
V_{GG}		Power supply for LCD drive
V_{OFF}		LCD-OFF level input pin
V_{EE}		Power supply for LCD drive
V_{DD}		Power supply for the internal logic
GND		Power supply for the internal logic

*: If XDON, XDOFF, and $\overline{OE}$ are asserted simultaneously, they are accepted in order of XDON, XDOFF, and $\overline{OE}$.

Operation Description

(1) Shift data transfer method

D/U Pin	Shift Data Input		Data Transfer Direction
	Input	Output	
L	DI/O1	DO/I1	OUT0 → OUT1 → OUT2 → OUT3 → ··· → OUT256 → OUT257
	DI/O2	DO/I2	
H	DO/I1	DI/O1	OUT257 → OUT256 → OUT255 → OUT254 → ··· → OUT2 → OUT1 → OUT0
	DO/I2	DI/O2	

(2) LCD panel drive outputs

Except for the first output, the LCD panel drive outputs are controlled by the data in shift registers A and B and the input signals XDON, XDOFF, and $\overline{OE}$ as shown below.

A	B	XDON	XDOFF	$\overline{OE}$	LCD Panel Drive Output
L	L	H	H	L	V_{OFF}
L	H	H	H	L	V_{EE}
H	L	H	H	L	V_{EE}
H	H	H	H	L	V_{GG}
X	X	H	L	X	V_{OFF}
L	L	H	H	H	V_{OFF}
L	H	H	H	H	V_{EE}
H	L	H	H	H	V_{EE}
H	H	H	H	H	V_{EE} (When CPV = high) V_{GG} (When CPV = low)
X	X	L	X	X	V_{GG}

X: Don't care

(3) First LCD panel drive output

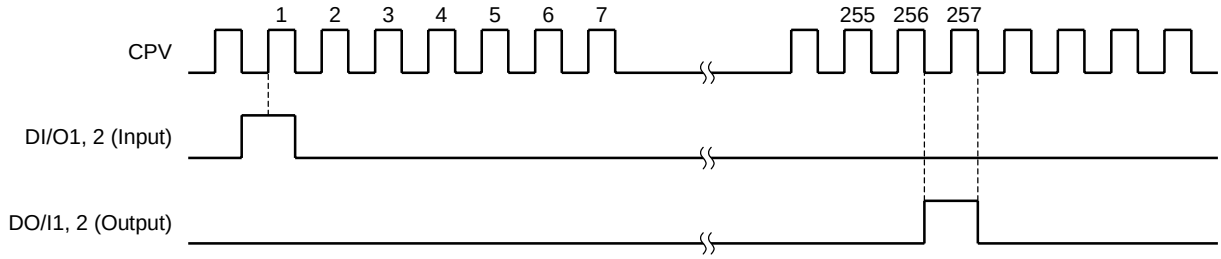
The first output (OUT0, OUT257) is output to the LCD according to the shift data (A1, B1/A256, B256) that respectively controls output 1 and output 256 as shown below.

The first output here means OUT0 when D/U = low and OUT257 when D/U = high.

D/U = "L"			D/U = "H"		
A1	B1	OUT0	A256	B256	OUT257
L	L	V_{OFF}	L	L	V_{OFF}
L	H	V_{EE}	L	H	V_{EE}
H	L	V_{EE}	H	L	V_{EE}
H	H	V_{EE}	H	H	V_{EE}

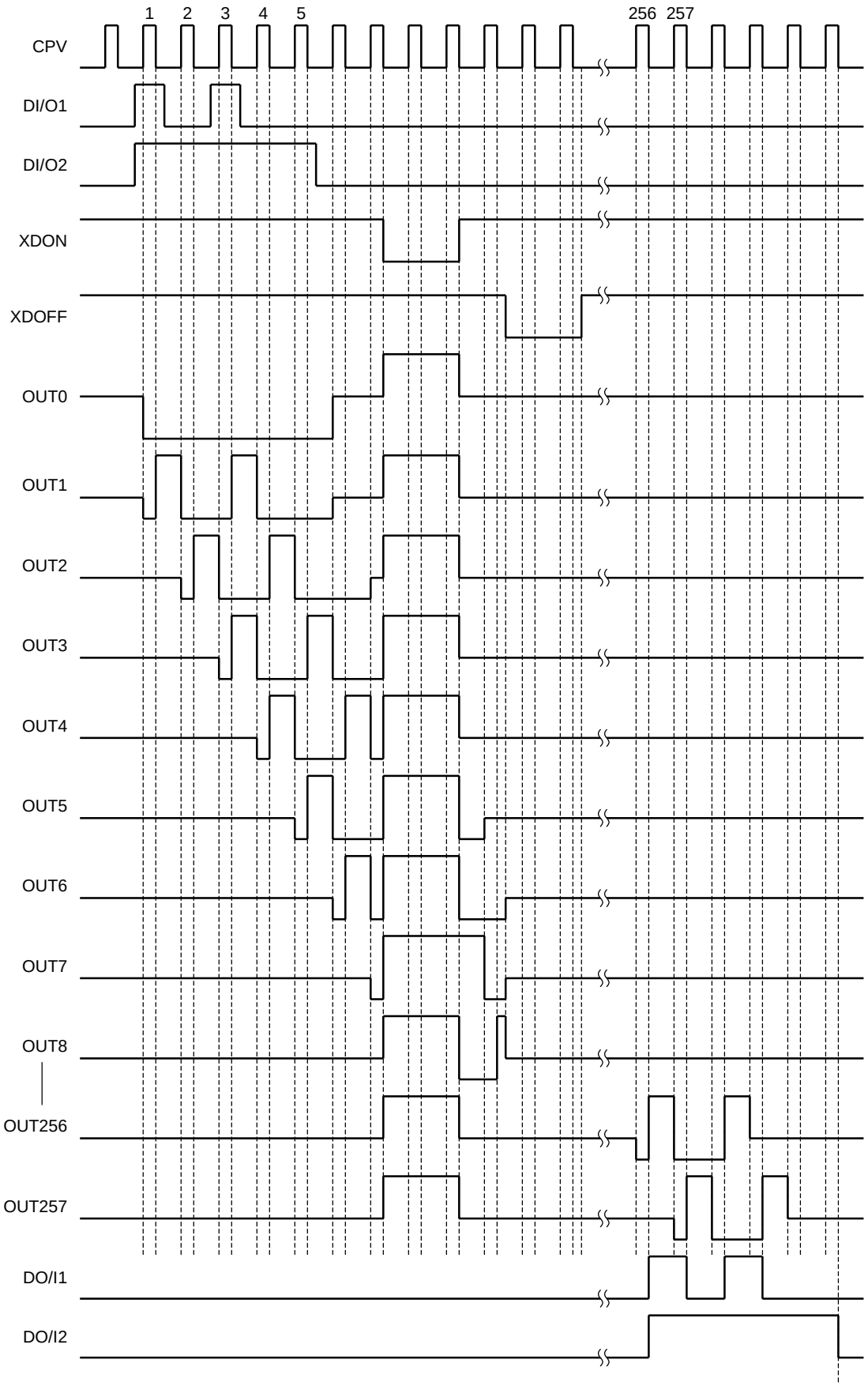
(4) Vertical shift data output

The vertical shift data output (When V_{DD} = high level, when GND = low level) is latched into the LCD synchronously with the falling edge of the last valid shift data (OUT256 or OUT1).



Timing Diagram

- **When D/U = low**
  When $\overline{OE}$ = high



Absolute Maximum Ratings (GND = 0 V)

Characteristics	Symbol	Rating	Unit	Relevant Pin
Supply voltage (1)	$V_{GG} - V_{EE}$	−0.3 to 48	V	
Supply voltage (2)	V_{EE}	−20 to 0.3		
Supply voltage (3)	V_{DD}	−0.3 to 6.0		
Input voltage	V_{IN}	GND to V_{DD} + 0.3	V	
Analog input voltage	V_{OFF}	V_{EE} − 0.3 to V_{GG} + 0.3	V	
Storage temperature	T_{stg}	−55 to 125	°C	

Recommended Operating Conditions (GND = 0 V)

Characteristics	Symbol	Rating	Unit	Note
Supply voltage (1)	$V_{GG} - V_{EE}$	20 to 42	V	When XDON is fixed to high level.
		20 to 38		When XDON is enabled.
Supply voltage (2)	V_{EE}	−15 to −5		
Supply voltage (3)	V_{DD}	2.7 to 3.6		
Supply voltage (4)	V_{GG}	10 to 28		
Operating temperature	T_{opr}	−20 to 75	°C	
Operating frequency	f_{CPV}	DC to 100	kHz	
Output load capacitance	C_L	300	pF/PIN	
Analog input voltage	V_{OFF}	V_{EE} to V_{EE} + 10	V	

Electrical Characteristics

DC Characteristics (GND = 0 V, V_{DD} = 2.7 to 3.6 V, Ta = −20 to 75°C)

Characteristics		Symbol	Testci-rcuit	Test Condition	Min	Max	Unit	Relevant Pin
Input voltage	Low level	V_{IL}	—	—	GND	0.2 × V_{DD}	V	(Note 1)
	High level	V_{IH}		—	0.8 × V_{DD}	V_{DD}		
Output voltage	Low level	V_{OL}	—	I_{OL} = 40 μA	GND	0.4	V	DI/O1, DI/O2, DO/I1, DO/I2
	High level	V_{OH}		I_{OH} = −40 μA	V_{DD} − 0.4	V_{DD}		
Output resistance	V_{EE} level	R_{EE}	—	V_{OUT} = V_{EE} + 0.5 V (Note 2)	—	1.0	kΩ	OUT0~ OUT257
	V_{OFF} level	R_{OFF}		V_{OUT} = V_{OFF} + 0.5 V (Note 2)				
	V_{GG}v	R_{GG}		V_{OUT} = V_{GG} − 0.5 V (Note 2)				
Input leakage current		I_{IN}	—	—	−1.0	1.0	μA	(Note 1)
Current consumption (1)		I_{DD}	—	(Note 3)	—	500	μA	V_{DD}
Current consumption (2)		I_{GG}		(Note 3)	—	100	μA	V_{GG}
Current consumption (3)		I_{GND}		(Note 3)	—	100	μA	GND

Note 1: DI/O1, DI/O2, DO/I1, DO/I2, CPV, D/U, XDON, XDOFF, $\overline{OE}$

Note 2: V_{GG} = 25 V, V_{OFF} = 0 V, V_{EE} = −10 V

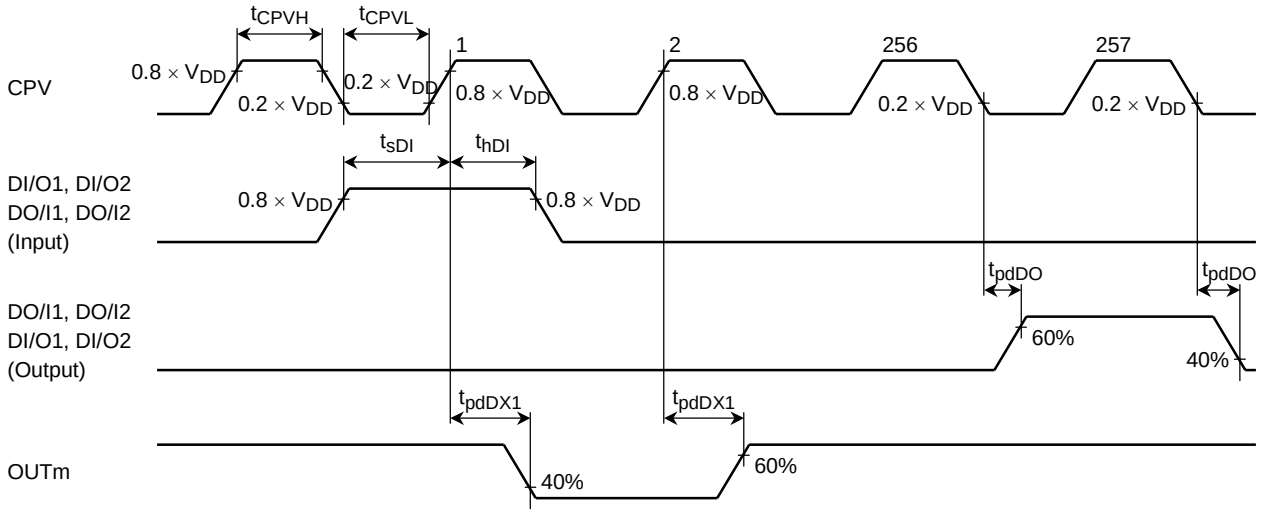
Note 3: CPV = 50 kHz, shift data input cycle = 60 Hz

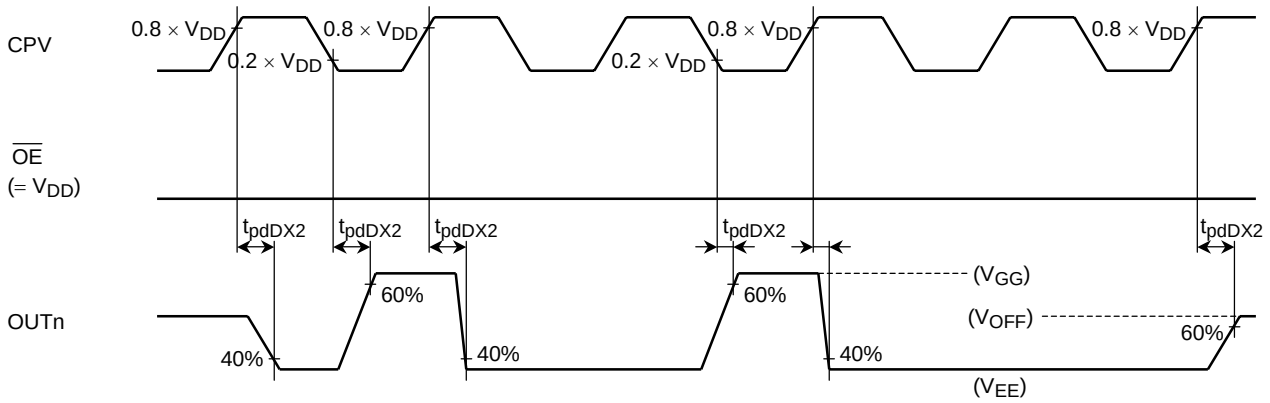
AC Characteristics (GND = 0 V, V_{DD} = 2.7 to 3.6 V, Ta = −20 to 75°C)

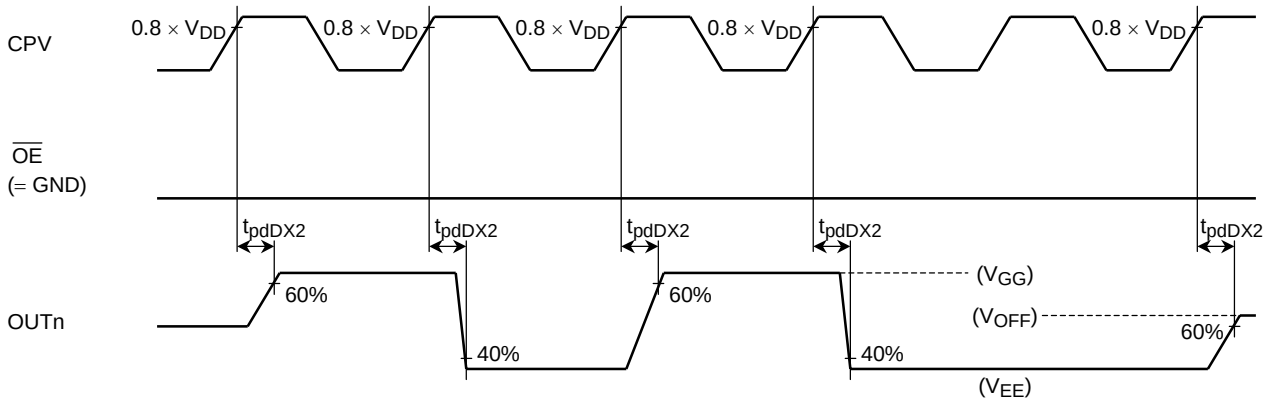
Characteristics	Symbol	Testci-rcuit	Test Condition		Min	Max	Unit
Clock period	t_{CPV}	—	—		10	—	μs
Clock pulse L	t_{CPVL}	—	—		4	—	μs
Clock pulse H	t_{CPVH}	—	—		1	—	μs
Data setup time	t_{sDI}	—	Ta = −20°C		1.3	—	μs
			Ta = 0°C		1.0	—	
Data setup time	t_{hDI}	—	—		0.5	—	ns
Output delay time (1)	t_{pdDO}	—	C_L = 15 pF (Note 4)		—	1.0	μs
Output delay time (2)	t_{pdDX1}	—	C_L = 300 pF (Note 4)	Ta = −20°C	—	1.6	
				Ta = 0°C	—	1.0	
Output delay time (3)	t_{pdDX2}	—	C_L = 300 pF (Note 4)	Ta = −20°C	—	1.6	
				Ta = 0°C	—	1.0	
Output delay time (4)	t_{pdOF}	—	C_L = 300 pF (Note 4)		—	1.0	
Output delay time (5)	t_{pdON}	—	C_L = 300 pF (Note 4) (Note 5)		—	10	
Display-off pulse	t_{wOF}	—	—		1	—	μs

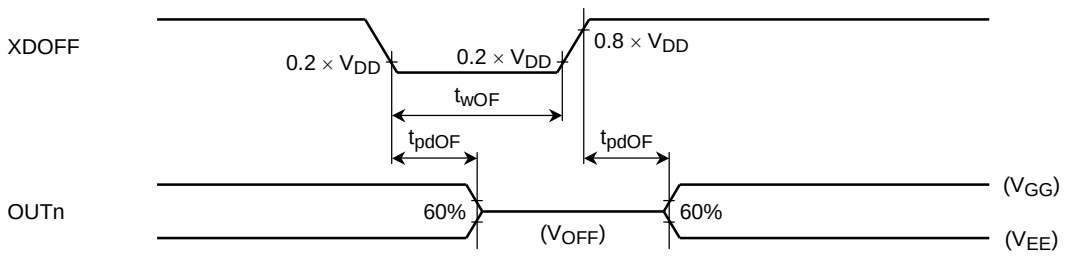
Note 4: V_{GG} = 20 to 28 V, V_{EE} = −15 to −6 V, V_{OFF} = V_{EE} + 3 V to V_{EE} + 7 V, but V_{GG} − V_{EE} = below 42 V.

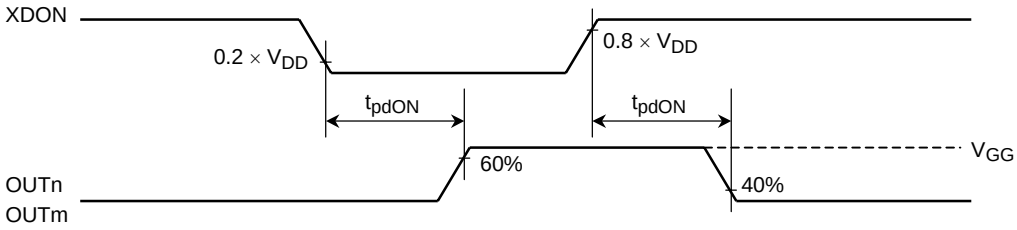
Note 5: V_{GG} − V_{EE} = below 38 V. Connect the external resistor above 62 Ω to V_{GG} line, and above 100 Ω to V_{OFF} line.


CPV
DI/O1, DI/O2
DO/I1, DO/I2
(Input)
DO/I1, DO/I2
DI/O1, DI/O2
(Output)
OUTm
tCPVH
tCPVL
tsDI
thDI
tpdDO
tpdDX1
0.8 × VDD
0.2 × VDD
1
2
256
257
60%
40%


CPV
OE
(= VDD)
OUTn
tpdDX2
0.8 × VDD
0.2 × VDD
60%
40%
(VGG)
(VOFF)
(VEE)


CPV
OE
(= GND)
OUTn
tpdDX2
0.8 × VDD
60%
40%
(VGG)
(VOFF)
(VEE)


XDOFF
OUTn
twOF
tpdOF
0.2 × VDD
0.8 × VDD
60%
(VOFF)
(VGG)
(VEE)

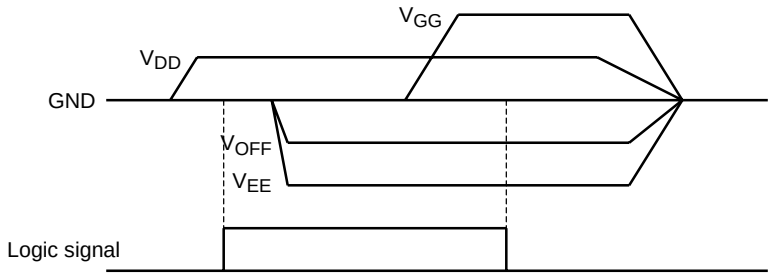


D/U = low level → OUTn: n = 1 to 257, OUTm: m = 0
D/U = high level → OUTn: n = 0 to 256, OUTm: m = 257

Power Supply Sequence

When the device is powerd ON, V_{DD} → logic signal → V_{EE}、V_{OFF} → V_{GG}; when power OFF, logic signal V_{DD} → V_{EE}, V_{OFF}, V_{GG}.

However, the relative potentials when the power is turned OFF are $V_{GG} \geqq V_{DD} \geqq V_{OFF} \geqq V_{EE}$.



*: The above sequence for the logic signal includes not only high and low-going transitions but also high and low levels (DC voltage levels).

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