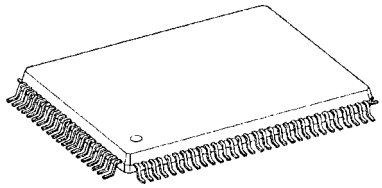
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T7779

CRT / LCD Controller LSI

The T7779 is a controller LSI for a raster−scan−type CRT display and large−scale dot matrix LCD. It can be used in applications ranging from small−scale character display systems to large−scale graphic display systems.



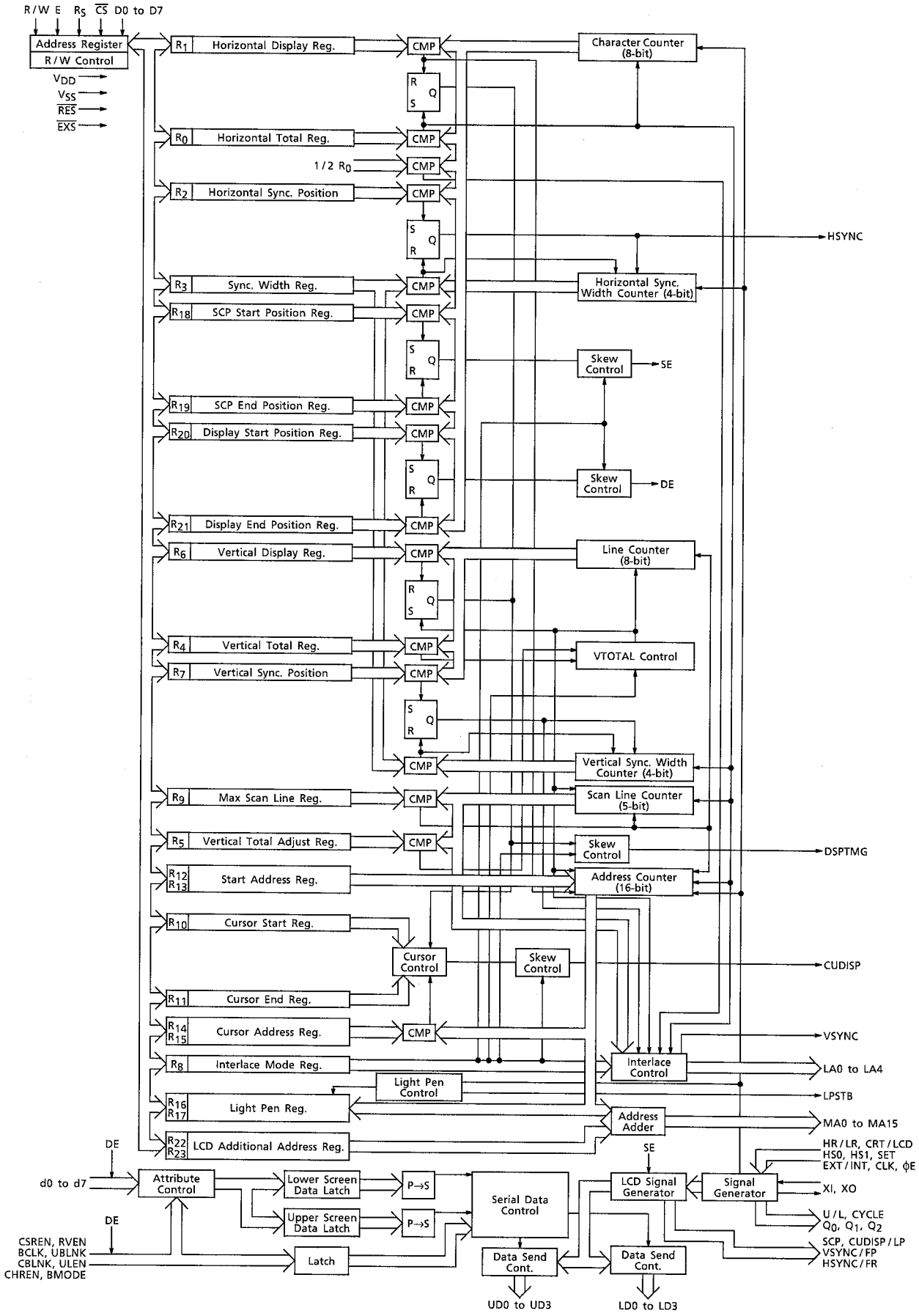
QFP100-P-1420-0.65J

Weight: 1.6 g (typ.)

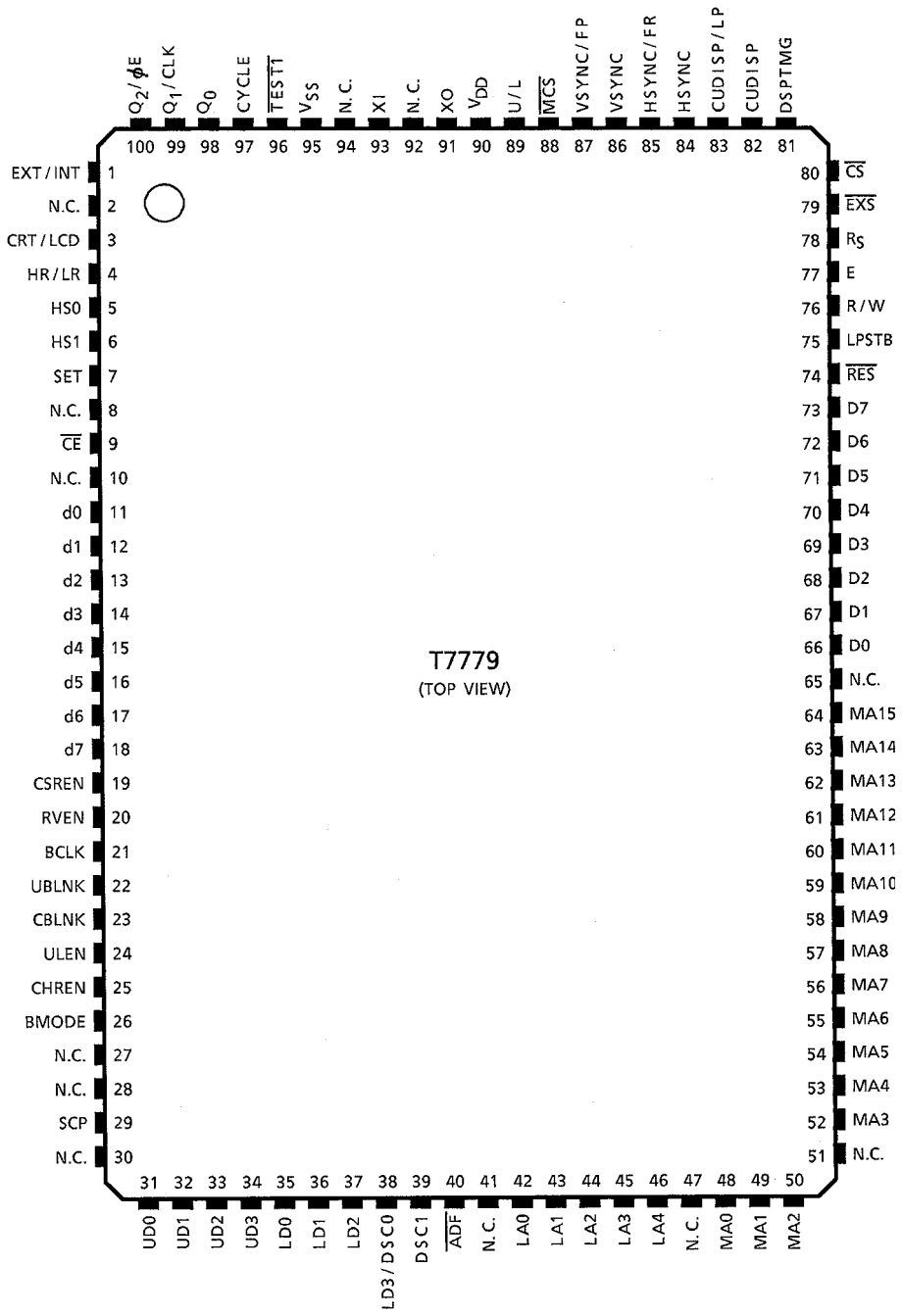
Features

- Refresh memory address : MA0 to MA15 (2^{16})
- Line scanning address : LA0 to LA4 (2^5)
- Frame buffer capacity : Max 64 KBytes (character)
  Max 2 MBytes (graphic)
- Number of characters per line : 1 to 255
- Number of character rows : 1 to 255
- Scrolling, Paging
- Built-in light pen−detecting function
- Horizontal dots per character according to font : 5, 6, 7, 8
- Vertical dots per character according to font : 1 to 32
- Data output : 1−bit output, 2−bit (odd/even) output, 4−bit output
- Various attribute functions : Underline Cursor ON/OFF
  Underline Cursor Blink
  Character ON/OFF
  Character Normal/Inverse
  Character Blink
  Blink Frequency Change
- External synchronization (Non−Interlace mode only)
- HMCS6800−family−compatible bus interface
- Single 5−V power supply
- High speed operation : 18 MHz
- Low power consumption
- CMOS, Si−Gate structure
- 100−pin flat plastic package

Block Diagram



Pin Assignment



Pin Functions

Pin Name	I / O	Functions
MA0 to MA15	Output	(Memory Address) Memory refresh address
LA0 to LA4	Output	(Line Address) Line scanning address for character generator
D0 to D7	I / O	(Data) Data I / O terminal for built−in registers
d0 to d7	Input	(Data) Parallel data input for LCD
$\overline{ADF}$	Input	(Address Float) For LA / MA outputs in High Impedance mode. High impedance when set to 0
CSREN	Input	(Cursor Enable) Underline cursor enabling signal Display of cursor is enabled when set to 1 (d0 to d7 are inhibited)
RVEN	Input	(Reverse Enable) Reverse attribute signal. Display of d0 to d7 is inverted when set to 1 (except for the cursor)
BCLK	Input	(Blink Clock) Clock input for blink. 0 = ON, 1 = OFF
UBLNK	Input	(Underline Blink) Underline blink attribute signal. Blink is enabled when set to 1
CBLNK	Input	(Character Blink) Character blink attribute signal. Blink is enabled when set to 1
ULEN	Input	(Underline Enable) Underline attribute signal. Underline is displayed when set to 1
CHREN	Input	(Character Enable) Data input enabling signal. Display is enabled when set to 1
BMODE	Input	(Blink Mode) To change an external / internal blink clock f_{BCLK}: Clock frequency supplied to the BCLK f_{FR} : Frame frequency

BMODE	0	1	1
BCLK	—	0	1
Blink Freq.	f_{BCLK}	f_{FR} / 8	f_{FR} / 16

Pin Name	I / O	Functions
SET	Input	(Set) To set built−in registers. Set when SET = 1 and CRT / LCD = 1
HR / LR	Input	(High Resolution / Low Resolution) High Resolution / Low Resolution mode select. High Resolution mode is selected when set to 1
CRT / LCD	Input	(Cathode Ray Tube / Liquid Crystal Display) CRT / LCD mode select. LCD mode is selected when set to 1

Pin Name	I / O	Functions			
$\overline{CS}$	Input	(Chip Select) Chip select signal input	$\overline{CS}$	R_S	Register name
			1	—	Invalid
R_S	Input	(Register Select) Register select signal input	0	0	Address register
			0	1	Control register
E	Input	(Enable) Enable signal input. Usually connected to system φ2 clock.			
R / W	Input	(Read / Write) R / W signal input. Read when set to 1			
$\overline{RES}$	Input	(Reset) Reset signal input. Reset when set to 0			
LPSTB	Input	(Light Pen Strobe) Light pen strobe signal input			
DSPTMG	Output	(Display Timing) Display timing signal			
CUDISP	Output	(Cursor Display) Cursor display signal			
CUDISP / LP	Output	(Cursor Display / Latch Pulse) Cursor display / latch pulse			
HSYNC	Output	(Horizontal SYNC) Horizontal synchronization			
HSYNC / FR	Output	(Horizontal SYNC / Frame) Horizontal sync / frame			
VSYNC	Output	(Vertical SYNC) Vertical synchronization			
VSYNC / FP	Output	(Vertical SYNC / Frame Pulse) Vertical sync / frame pulse			
SCP	Output	(Shift Clock Pulse) Shift clock pulse for column driver			
$\overline{MCS}$	Output	(Multi Controller Sync) Multi controller synchronization			
U / L	Output	(Upper / Lower) Upper / lower screen signal. Upper screen when set to 0			
CYCLE	Output	(Cycle Steal) Cycle steal signal			
$\overline{CE}$	Output	(Chip Enable) Chip enable signal			
DSC1	Input	(Data Sending Control 1) Serial data format select			
LD3 / DSC0	O / I	(Lower Data 3 / Data Sending Control 0) Serial data for column driver / serial data format select			

Pin Name	I / O	Functions					
LD0 to LD2	Output	(Lower Data 0 to 2) Serial data for column driver					
UD0 to UD3	Output	(Upper Data 0 to 3) Serial data for column driver					
$\overline{EXS}$	Input	(External Sync) External synchronization					
HS0, HS1	Input	(Horizontal Select) To determine the number of horizontal dots per font	HS0	0	1	0	1
			HS1	0	0	1	1
			Horizontal dot	5	6	7	8
Q_0	Output	Built−in dot counter output					
Q_1 / CLK	O / I	Built−in dot counter output / word clock input					
Q_2 / φE	O / I	Built−in dot counter output / dot clock input					
EXT / INT	Input	(External / Internal) External / internal clock select. Internal clock when set to 1					
XI, XO	—	Connect to crystal oscillator					
$\overline{TEST1}$	Input	(Test) Usually connected to V_{DD}					
V_{DD}	—	Power supply (5 V)					
V_{SS}	—	Power supply (0 V)					

Note 1: DSC1 = 0: LD3 / DSC0 = DSC0 (input)

(a) DSC0 = 0 (1−bit mode)

UD0: for dots in the upper area

LD0: for dots in the lower area

(b) DSC0 = 1 (2−bit mode)

UD0: for even dots in the upper area

UD1: for odd dots in the upper area

LD0: for even dots in the lower area

LD1: for odd dots in the lower area

Note 2: DSC1 = 1 (4−bit mode): LD3 / DSC0 = LD3 (output)

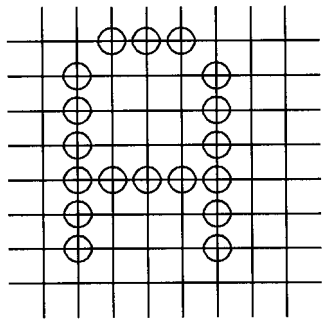
UD0 to UD3: for dots in the upper area

LD0 to LD3: for dots in the lower area

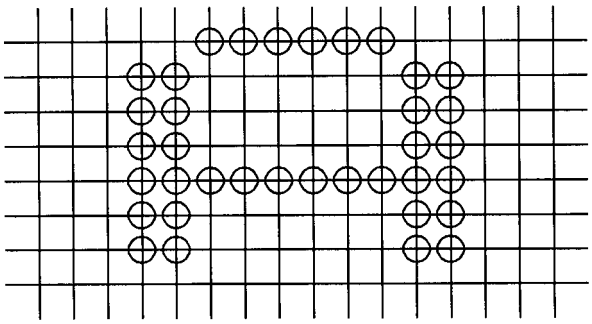
Description of Pins

- **HR / LR**

The HR / LR input is used to select either High Resolution mode or Low Resolution mode, in the LCD mode. The difference between the High Resolution mode and the Low Resolution mode is shown in the following diagram.



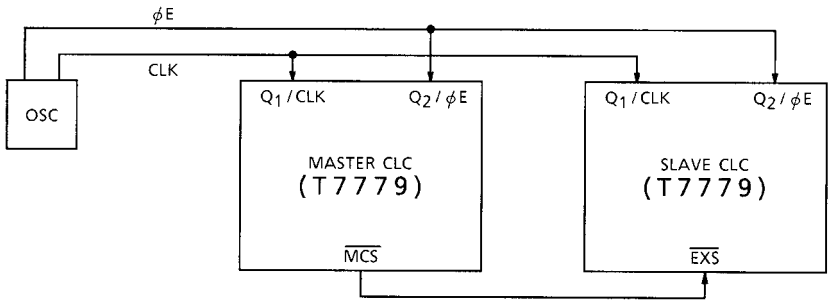
"A" displayed in High Resolution mode



"A" displayed in Low Resolution mode

- $\overline{EXS}$

In Non−Interlace mode only, the $\overline{EXS}$ input is used to synchronize the slave−CLC to the master−CLC.



- **SET**

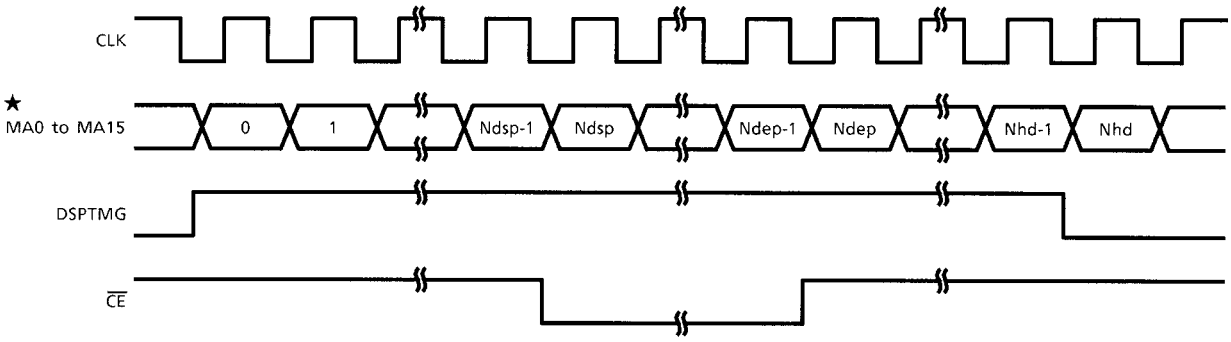
The SET input is used to set the internal registers. In LCD mode, a high level on the SET input forces the internal registers into the following state:

Register No.	Register Name	2 ≤ Nr ≤ 31		Nr = 0 or 1	
		LR	HR	LR	HR
R_0	Horizontal Total	47	87	47	87
R_1	Horizontal Displayed	*	*	*	*
R_2	H. Sync Position	*	*	*	*
R_3	Sync Width	*	*	*	*
R_4	Vertical Total	12	12	51	51
R_5	V. Total Adjust	0	0	0	0
R_6	Vertical Displayed	255	255	255	255
R_7	V. Sync Position	255	255	255	255
R_8	Interlace Mode and Skew	0	0	0	0
R_9	Max. Scan Line Address	*	*	*	*
R_{10}	Cursor Start	*	*	*	*
R_{11}	Cursor End	*	*	*	*
R_{12}	Start Address (H)	*	*	*	*
R_{13}	Start Address (L)	*	*	*	*
R_{14}	Cursor Address (H)	*	*	*	*
R_{15}	Cursor Address (L)	*	*	*	*
R_{16}	Light Pen (H)	*	*	*	*
R_{17}	Light Pen (L)	*	*	*	*
R_{18}	SCP Start Position	128	128	128	128
R_{19}	SCP End Position	Nhd	Nhd	Nhd	Nhd
R_{20}	Display Start Position	0	0	0	0
R_{21}	Display End Position	Nhd	Nhd	Nhd	Nhd
R_{22}	Additional Address (H)	2	4	8	8
R_{23}	Additional Address (L)	8	16	32	32

LR: Low Resolution mode
HR: High Resolution mode
*: Does not change

- $\overline{CE}$

  The $\overline{CE}$ output is a low−active signal which indicates the presence of a valid data address (d0 to d7, attribute) to the external logic



★ The initial MA is determined by R_{12} / R_{13} (Start Address Register), which is zero in this timing example.

Built−in Registers

Internal operation of the T7779 is determined by the value of the built−in registers. When you want to write to these registers, first you must write the control register address into the address register (R_S = 0). Then you can write (or read) the value into (or from) the control register (R_S = 1).

$\overline{CS}$	R_S	Register	Read	Write
1	—	Invalid	—	—
0	0	Address Register	×	O
0	1	Control Register	—	—

Register No.	Register Name	SYM.	Data Bit							
			7	6	5	4	3	2	1	0
R_0	Horizontal Total*	Nht								
R_1	Horizontal Displayed	Nhd								
R_2	Horizontal Sync Position*	Nhsp								
R_3	Sync Width	Nvsw Nhsw	VW3 to VW0				HW3 to HW0			
R_4	Vertical Total*	Nvt								
R_5	Vertical Total Adjust	Nadj	—							
R_6	Vertical Displayed	Nvd								
R_7	Vertical Sync Position*	Nvsp								
R_8	Interlace Mode and Skew		C_1	C_0	D_1	D_0	—		V	S
R_9	Max Scan Line Address	Nr	—							
R_{10}	Cursor Start	Ncsr	CUL	B	P					
R_{11}	Cursor End	Ncer	—							

Register No.	Register Name	SYM.	Data Bit							
			7	6	5	4	3	2	1	0
R_{12}	Start Address (H)									
R_{13}	Start Address (L)									
R_{14}	Cursor Address (H)									
R_{15}	Cursor Address (L)									
R_{16}	Light Pen (H)									
R_{17}	Light Pen (L)									
R_{18}	SCP Start Position	Nssp	SC							
R_{19}	SCP End Position	Nsep								
R_{20}	Display Start Position	Ndsp								
R_{21}	Display End Position	Ndep								
R_{22}	Additional Address (H)									
R_{23}	Additional Address (L)									

Note 1: Write Value of register marked by "*"
(Write value) = (fixed value) −1

Note 2: Write Value of R_9
- Non−Interlace mode ····· (Write Value Nr) = (Appointing value) − 1
  Interlace Sync mode ····· (Write Value Nr) = (Appointing value) − 1
- Interlace Sync and Video mode (Write Value Nr) = (Appointing value) − 2

Note 3: For Interlace mode, the horizontal total register (R_0) must be odd.

Note 4: Bits 0 to 3 of R_3 determine the width of the horizontal sync. pulse.
Bits 4 to 7 of R_3 determine the width of the vertical sync. pulse.

Vw3	Vw2	Vw1	Vw0	Pulse Width
0	0	0	0	16H
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

H: Scan−line time

Hw3	Hw2	Hw1	Hw0	Pulse Width
0	0	0	0	Don't care
0	0	0	1	1HC
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

HC: Character time

Note 5: Bits 0 and 1 of R_8 control the Interlace mode. Bits 4 and 5 of R_8 control the DSPTMG skew. Bits 6 and 7 of R_8 control the CUDISP skew.

V	S	Raster−Scan Mode
0	0	Non−Interlace Mode
0	1	
1	0	Interlace Sync Mode
1	1	Interlace Sync and Video Mode

D_1	D_0	Dsptmg Skew
0	0	No Character Skew
0	1	One Character Skew
1	0	Two Character Skew
1	1	Not Available

C_1	C_0	Cudisp Skew
0	0	No Character Skew
0	1	One Character Skew
1	0	Two Character Skew
1	1	Not Available

Note 6: Bit 5 of R_{10} is used for blink period control, bit 6 is used to select blink or non−blink, and Bit 7 is used to select the cursor display screen for the LCD.

B	P	Cursor Display Mode
0	0	Non−Blink
0	1	Cursor Non−Display
1	0	Blink 1/16 Field Rate
1	1	Blink 1/32 Field Rate

CUL	Cursor Display Screen
0	Upper Screen
1	Lower Screen

Note 7: Bit 7 of R_{18} determines the number of the LCD screen.

S_C	Number of LCD Screen
0	1
1	2

- **Address register**

R_S	R / W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	Write				REGISTER ADDRESS				

This 5−bit write−only register contains the address of one of the other 24 registers. When you want to write or read one of the registers (R_0 to R_{23}), first you must write the address of the register in this register.

- **Control register**

Note: ▽= CRT mode, ▼= LCD mode

(1) Horizontal total register (R_0)

R_S	R / W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	Write	Nht-1							

▽ This 8−bit write−only register determines the horizontal sync. frequency. The value entered in this register should be one less than the total number of characters on one line.

▼ This 8−bit write−only register determines the non−displayed character times (retrace). If there is no retrace period, this LSI does not operate correctly. The retrace period is the difference between Nht + 1 and Nhd (= Nht + 1 − Nhd). Usually this value should be set to Nhd + 1. In 1 Character Skew mode, set the value to Nhd + 2. In 2 Character Skew mode, set the value to Nhd + 3.

(2) Horizontal displayed register (R_1)

R_S	R / W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	Write	Nhd							

▽▼ This 8−bit write−only register determines the number of characters displayed per line. The contents of R_1 must be less than the contents of R_0 (Nhd < Nht).

(3) Horizontal sync. position register (R_2)

R_S	R / W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	Write	Nhsp-1							

▽ This 8−bit write−only register determines the horizontal sync. position. The value held in this register is one less than the computed number of characters.

▼ The horizontal sync. pulse is not necessary. However, you can use it if you wish.

(4) Sync width register (R_3)

R_S	R / W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	Write	Nvsw				Nhsw			

▽▼ This 8−bit write−only register determines the width of the vertical and horizontal sync. pulses.
When Nvsw = 1 to 15, pulse width = 1 to 15H (H: time to scan 1 line)
When Nvsw = 0, pulse width = 16 H
When Nhsw = 1 to 15, pulse width = 1 to 15HC (HC: time to scan 1 character)
When Nhsw = 0, don't care.

(5) Vertical total register (R_4)

R_S	R / W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	Write	Nvt-1							

▽ This 8−bit write−only register determines the vertical sync. frequency. The value entered in this register is one less than the number of lines of characters.

▼ This 8−bit write−only register determines the number of rows displayed on the screen. The value held in the register is one less than the number of lines of characters.

(6) Vertical total adjust register (R_5)

R_S	R / W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	Write				Nadj				

▽ This 5−bit write−only register adjusts the total number of scan lines per frame.

▼ Usually set to 0.

(7) Vertical displayed register (R_6)

R_S	R / W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	Write	Nvd							

▽ This 8−bit write−only register determines the number of character rows displayed on the screen. The contents of R6 is less than the contents of R4 (Nvd < Nvt).

▼ The contents of R_6 must be more than the contents of R_4 (Nvd > Nvt). Usually set to FF (Hex).

(8) Vertical sync. position register (R_7)

R_S	R / W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	Write	Nvsp-1							

▽ This 8−bit write−only register determines the vertical sync. position. The value entered in this register is one less than the computed number of character lines.

▼ The vertical sync. pulse is not necessary. However, you can use it if you wish.

(9) Interlace mode and skew register (R_8)

R_S	R / W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	Write	C_1	C_0	D_1	D_0			V	S

V	S	INTERLACE MODE
0	0	Non-Interlace Mode
0	1	
1	0	Interlace Sync Mode
1	1	Interlace Sync and Video Mode

D_1	D_0	DSPTMG
0	0	No Character Skew
0	1	1-Character Skew
1	0	2-Character Skew
1	1	Not Available

C_1	C_0	CUDISP
0	0	No Character Skew
0	1	1-Character Skew
1	0	2-Character Skew
1	1	Not Available

▽ Interlace modes are selected using the two low order bits of this 6−bit write−only register. DSPTMG skew is controlled by bits 4 and 5 of R_8. CUDISP skew is controlled by bits 6 and 7 of R_8.

▼ Non−Interlace mode only is available. The skew function is the same as for CRT mode.

(10) Max scan line address register (R_9)

R_S	R / W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	Write				Nr-1				

▽ This 5−bit write−only register determines the number of scan lines per character row. In Non−Interlace or Interlace Sync mode, the value programmed in the register is one less than the number of scan lines. In Interlace Sync and Video mode, the value is two less than the number of scan lines.

▼ This 5−bit write−only register determines the number of horizontal dots per character row. The value is one less than the number of horizontal dots.

(11) Cursor start register (R_{10})

R_S	R / W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	Write	C_{UL}	B	P	Ncsr				

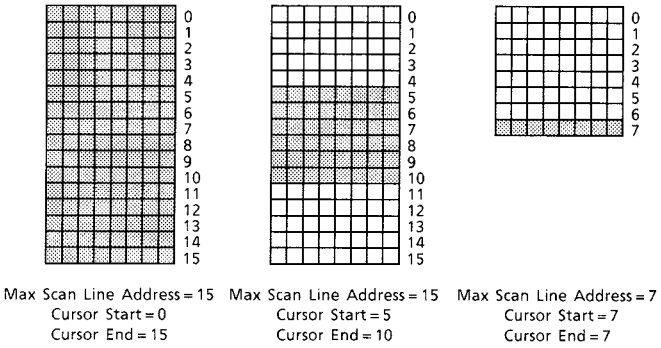
▽ This register determines the start scan line of the cursor and the cursor display mode. Bits 0 to 4 of R10 determine the start scan line of the cursor. Bits 5 and 6 (P, B) of R_{10} determine the cursor display mode.

▼ In LCD 2−screen mode, bit 7 of R_{10} determines the cursor display screen. If you want to program the cursor position anywhere in the lower screen, bit 7 of R_{10} must be set to 1.

(12) Cursor end register (R_{11})

R_S	R / W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	Write				Ncer				

▽▼ This 5−bit write−only register determines the last scan line of cursor.



B	P	CURSOR DISPLAY MODE
0	0	Non-Blink
0	1	Non-Display
1	0	Blink 1 / 16 Field Rate
1	1	Blink 1 / 32 Field Rate

(13) Start address register (R_{12}, R_{13})

R_S	R / W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	R / W	START ADDRESS (H)-R_{12}							
1	R / W	START ADDRESS (L)-R_{13}							

▽▼ This 16−bit read / write register pair determines the memory address corresponding to the first line on the screen. Hardware scrolling by line or page may be accomplished by modifying the contents of this register.

(14) Cursor address register (R_{14}, R_{15})

R_S	R / W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	R / W	CURSOR ADDRESS (H)-R_{14}							
1	R / W	CURSOR ADDRESS (L)-R_{15}							

▽ This 16−bit read / write register pair determines the cursor display address.

▼ The built−in address counter generates only upper screen addresses. If you want to program the cursor position anywhere in the lower screen, this register pair must be programmed with the upper screen address corresponding to the lower screen address.

(15) Light pen register (R_{16}, R_{17})

R_S	R / W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	Read	LIGHT PEN ADDRESS (H)-R_{16}							
1	Read	LIGHT PEN ADDRESS (L)-R_{17}							

▽ This 16−bit read−only register pair captures the refresh address on the positive edge of LPSTB.

(16) SCP start position register (R_{18})

R_S	R / W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	R / W	S_C	Nssp						

$S_C = 0$: 1 screen, $S_C = 1$: 2 screens

▼ This 8−bit read / write register determines the SCP (Shift Clock Pulse) start position. The value held in bits 0 to 6 of this register is one less than the computed number of characters. This value is set to 0. Bit 7 of R_{18} determines the number of LCD screens.

(17) SCP end position register (R_{19})

R_S	R / W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	R / W	Nsep							

▼ This 8−bit read / write register determines the SCP end position. The value held in the register is one less than the computed number of characters. This register is usually set to the same value as R_1.

(18) Display start position register (R_{20})

R_S	R / W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	R / W	Ndsp							

▽▼ This 8−bit read / write register determines the display start position. The value held in the register is one less than the computed number of characters. The register is usually set to 0.

(19) Display end position register (R_{21})

R_S	R / W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	R / W	Ndep							

▽▼ This 8−bit read / write register determines the display end position. The value held in the register is one less than the computed number of characters. This register is usually set to the same value as R_1.

(20) Additional address register (R_{22}, R_{23})

R_S	R / W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	R / W	ADDITIONAL ADDRESS (H)-R_{22}							
1	R / W	ADDITIONAL ADDRESS (L)-R_{23}							

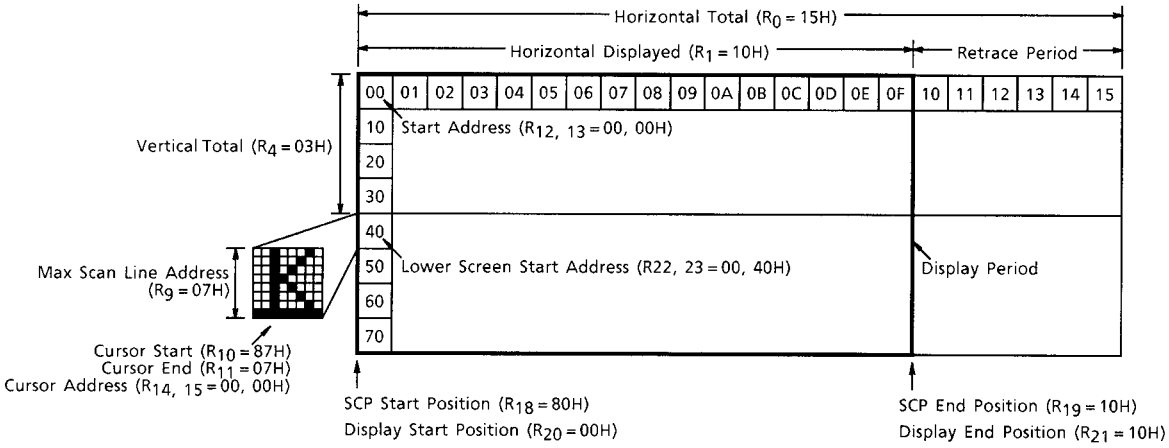
▼ The built−in address counter generates only upper screen addresses. The T7779 adds the contents of this 16−bit register pair to the address counter value to form the lower screen address.

Function Description

- **Register functions**

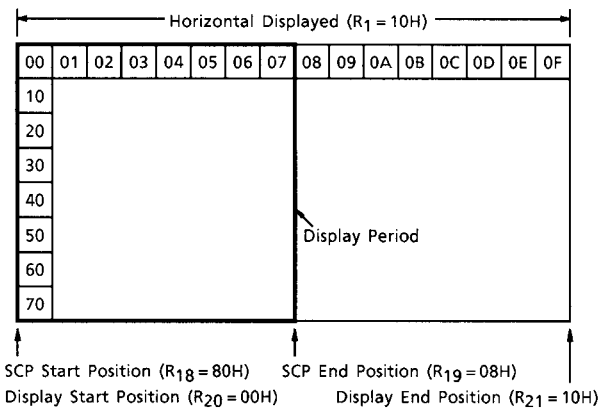
(1) An example of register values

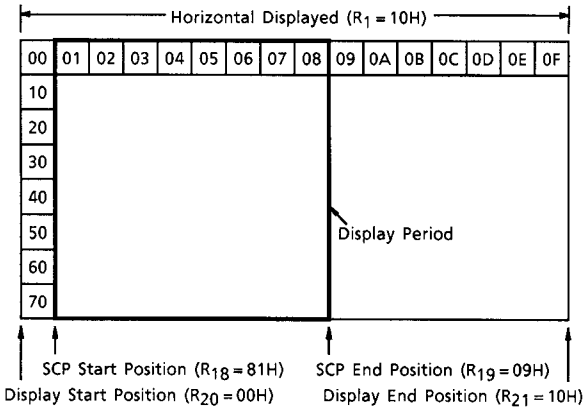
An example of register values in LCD 2−Screen mode is shown below



(2) Horizontal scroll function (LCD mode)

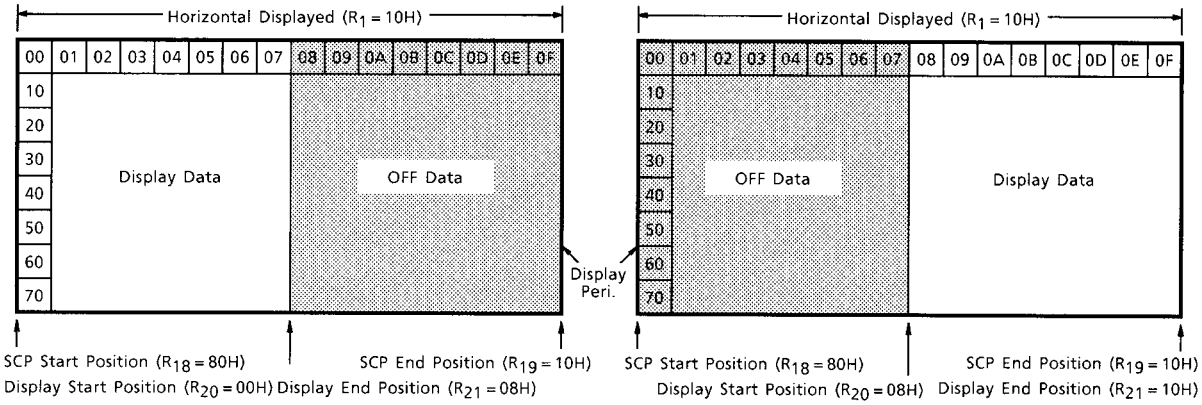
Hardware horizontal character scrolling may be accomplished by modifying the contents of the SCP start position register (R_{18}) and SCP end position register (R_{19}).





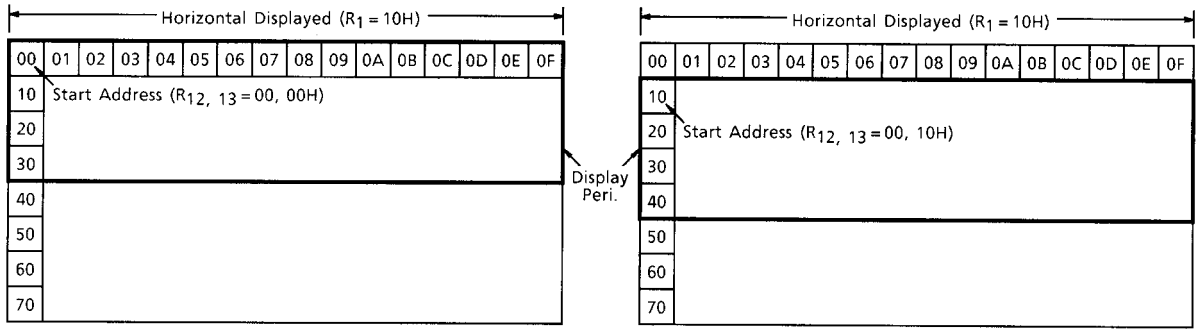
(3) Mask function

Hardware character masking may be accomplished by modifying the contents of the display start position register (R_{20}) and display end position register (R_{21}). This function is useful for the multicontroller system.



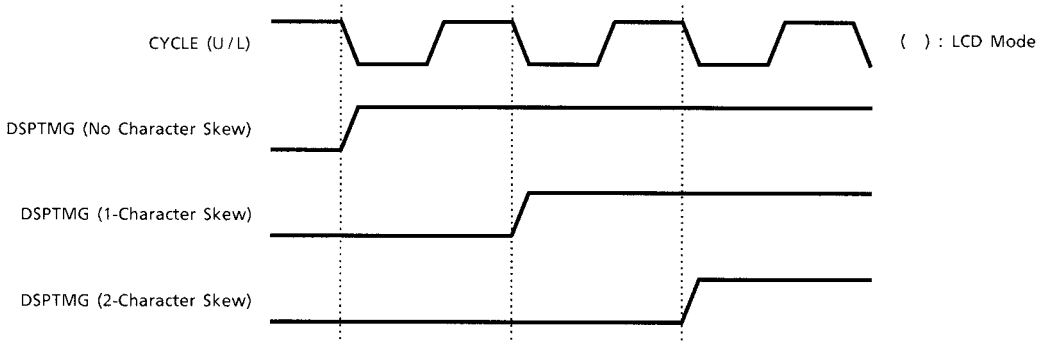
(4) Vertical scroll function

Hardware vertical scrolling by line or by page may be accomplished by modifying the contents of the start address register ($R_{12, 13}$) without modifying the contents of refresh memory.

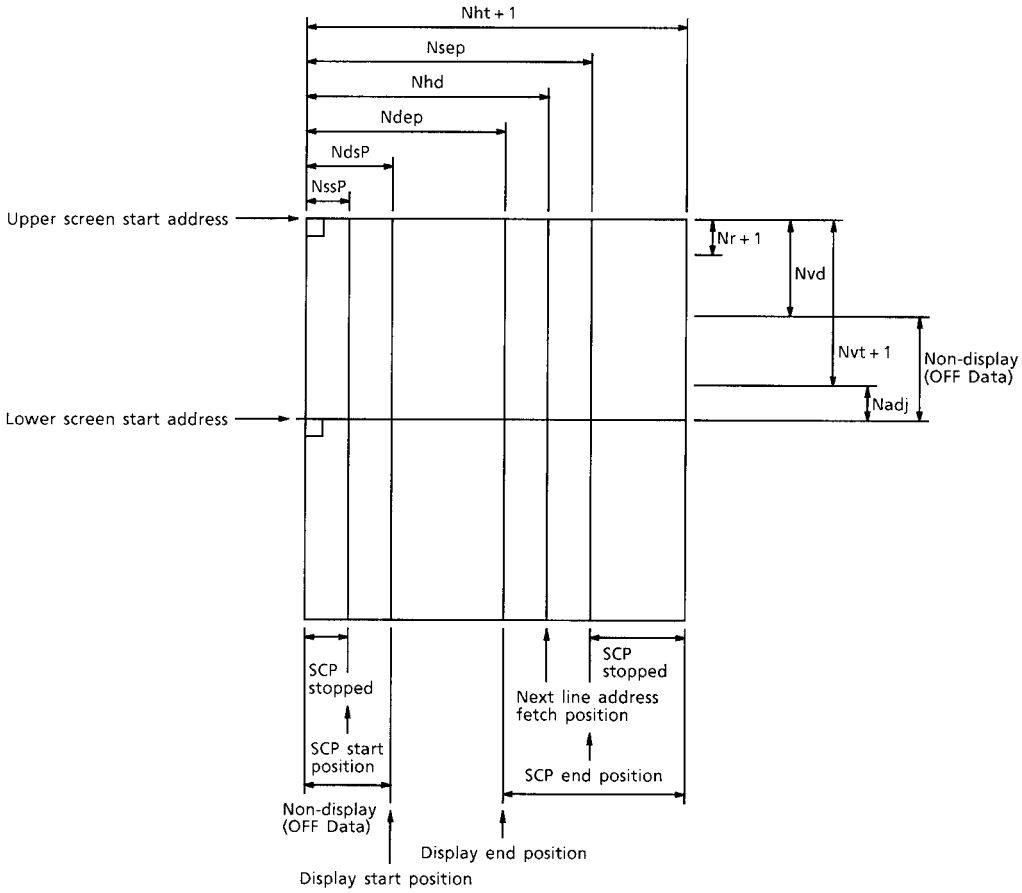


(5) Skew function

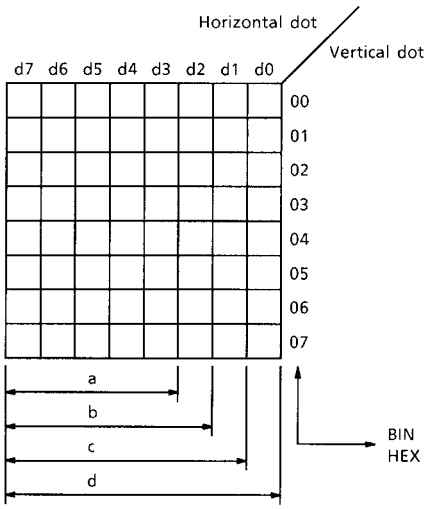
If the memory access cycle and the data latch are not synchronized to each other, this function must be used.



• Screen Format



- **Relationship between memory address (LA0 to LA4) and memory data (d0 to d7) The addresses of vertical dots are in hex. format.**



a : Valid data when these are 5 horizontal dots (HS0 = 0, HS1 = 0)
b : Valid data when these are 6 horizontal dots (HS0 = 1, HS1 = 0)
c : Valid data when these are 7 horizontal dots (HS0 = 0, HS1 = 1)
d : Valid data when these are 8 horizontal dots (HS0 = 1, HS1 = 1)

EX.) When address is 07H

LA4	LA3	LA2	LA1	LA0
0	0	1	1	1
0	7			

- **Relationship between the display screen and memory addresses (MA0 to MA15, LA0 to LA4)**

LINE \ CHAR-ACTER	LA	Display period 1	2		80	Retrace period 81		
1	000	0000	0001	→	004F	0050		Upper screen
	001	0000	0001	→	004F	0050		
	010							
	011							
	100							
	101							
	110							
	111	0000	0001	→	004F	0050		
2	000	0050	0051	→	009F	00A0		
	111	0050	0051	→	009F	00A0		
↓		↓	↓					
13	000	03C0	03C1	→	040F	0410		
	111	03C0	03C1	→	040F	0410		
14	000	0410	0411	→	045F	0460		Lower screen
	111	0410	0411	→	045F	0460		
↓		↓	↓					
25	000	0780	0781	→	07CF	07D0		
	111	0780	0781	→	07CF	07D0		

Note: State address: 0000H
LCD lower screen additional address: 0410H
Nr (maximum raster address): 07H
80 characters × 13 lines × 2 screens

● Operating Modes

The T7779 has two operating modes; CRT mode and LCD mode. LCD mode is further subdivided into 1−Screen mode, 2−Screen mode, High Resolution mode and Low Resolution mode.

(1) CRT mode

When CRT / LCD = 0, the T7779 operates in CRT mode. The T7779 consists of a CRT controller and LCD interface circuit. In CRT mode, the T7779 uses the CRT controller circuit only. When the T7779 is operating in CRT mode, you can use the parallel−to−serial circuit that is included in the LCD interface circuit. However, when you have to operate the P / S circuit at more than 18 MHz, you cannot use the built−in P / S circuit.

(2) LCD mode

When CRT / LCD = 1, the T7779 operates in LCD mode. When the T7779 is operating in LCD mode, the CRT controller circuit generates only upper screen addresses.

a) 2− Screen mode

When the T7779 is operating in LCD mode, the cycle time of the built−in address counter is twice that when the T7779 is operating in CRT mode. In 2−Screen mode (R_{18}−bit 7 = 1), the T7779 generates the lower screen address by adding the built−in address counter value and the contents of R_{22}, R_{23}. When U / L = L, the upper screen address is sent out from the MA0 to MA15 pins. When U / L = H, the lower screen address is sent out from the MA0 to MA15 pins. In this case, however, the LA0 to LA4 outputs do not change. So it is impossible to set a row that extends from the upper screen to the lower screen.
The cycle time of the U / L−signal is twice as long as that of the CYCLE−signal. The CYCLE−signal is L in the first half of the U / L−signal, and H in the second half of the U / L−signal. If the CPU accesses the display memory when CYCLE = L, you can rewrite the display memory without disturbing the display.

b) 1− Screen mode

When the T7779 is operating in LCD mode, the cycle time of the built−in address counter is twice that when the T7779 is operating in CRT mode. In 1−Screen mode (R_{18}−bit 7 = 0), the upper screen address is sent out from MA0 to MA15 pins during the cycle time of the U / L−signal. The CYCLE−signal is sent out using the same timing as in 2−Screen mode.

c) High Resolution mode

High Resolution mode is usually set (HR / LR = 1).

d) Low Resolution mode

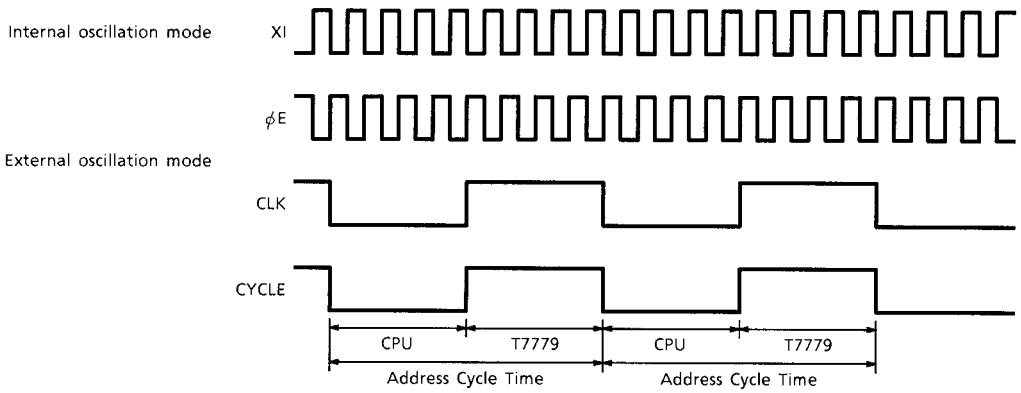
In Low Resolution mode (HR / LR = 0), each horizontal dot is displayed twice. When the total of horizontal dots = 640 and the number of horizontal dots per character = 8, 80−characters are displayed in High Resolution mode and 40−characters are displayed in Low Resolution mode. When you change the High Resolution / Low Resolution mode setting, you must change not only the HR / LR pin but also the contents of the built−in registers to match 40−character display.

- **Memory Interface**

If the CPU accesses the memory while the T7779 is accessing the memory, the display will be disturbed. There are two methods for rewriting the display memory without disturbing the display. One is to rewrite the display memory during the retrace period (DSPTMG = L). The other is to rewrite the display memory while CYCLE = L. A detailed explanation of the second case is shown below.

(1) Interface for CRT mode

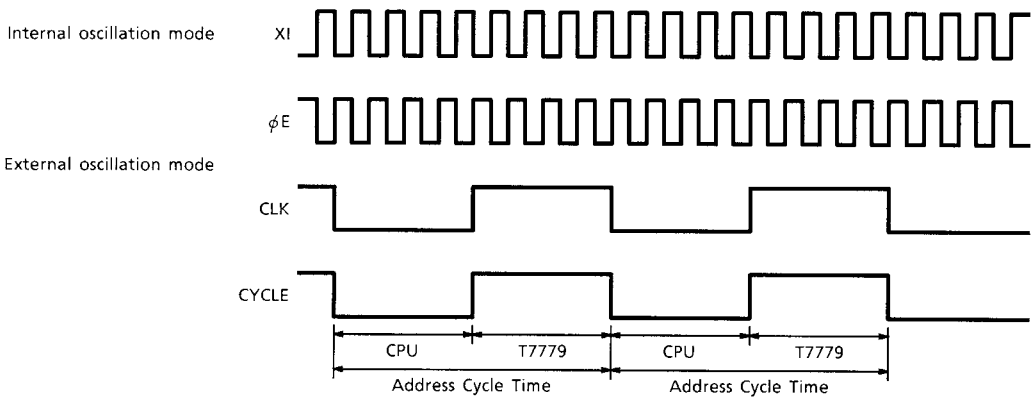
The interface circuit must be constructed so that the CPU can access the memory when CYCLE = L.



When $f\phi$ = 16 MHz, address cycle time = 500 ns

(2) Interface for LCD 2−Screen mode

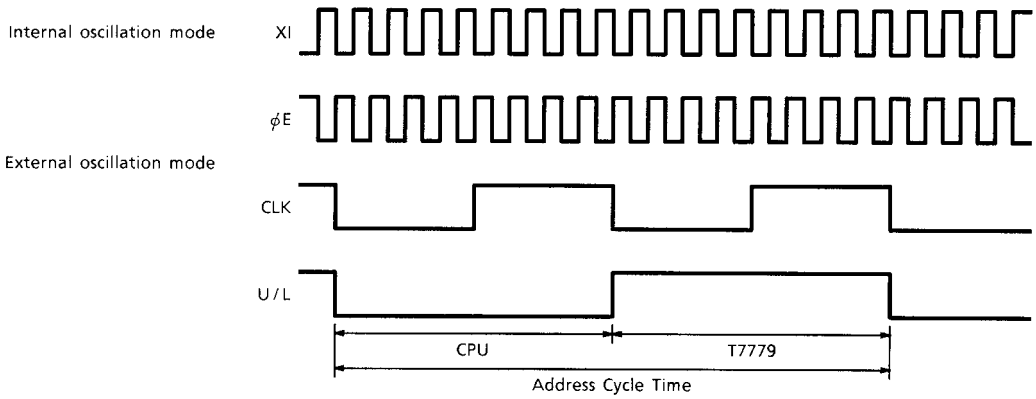
The interface circuit must be constructed so that the CPU can access the memory when CYCLE = L.



When $f\phi$ = 16 MHz, address cycle time = 500 ns

(3) Interface for LCD 1−Screen mode

The interface circuit must be constructed so that the CPU can access the memory when U / L = L.

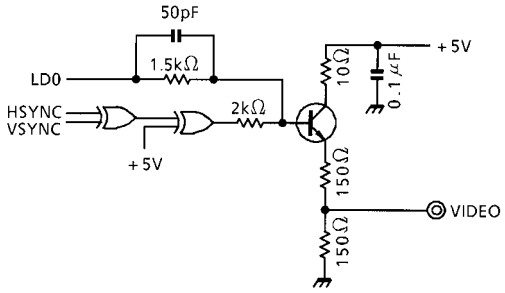


When fφ = 16 MHz, address cycle time = 1000 ns

• Monitor Interface

(1) CRT (NTSC)

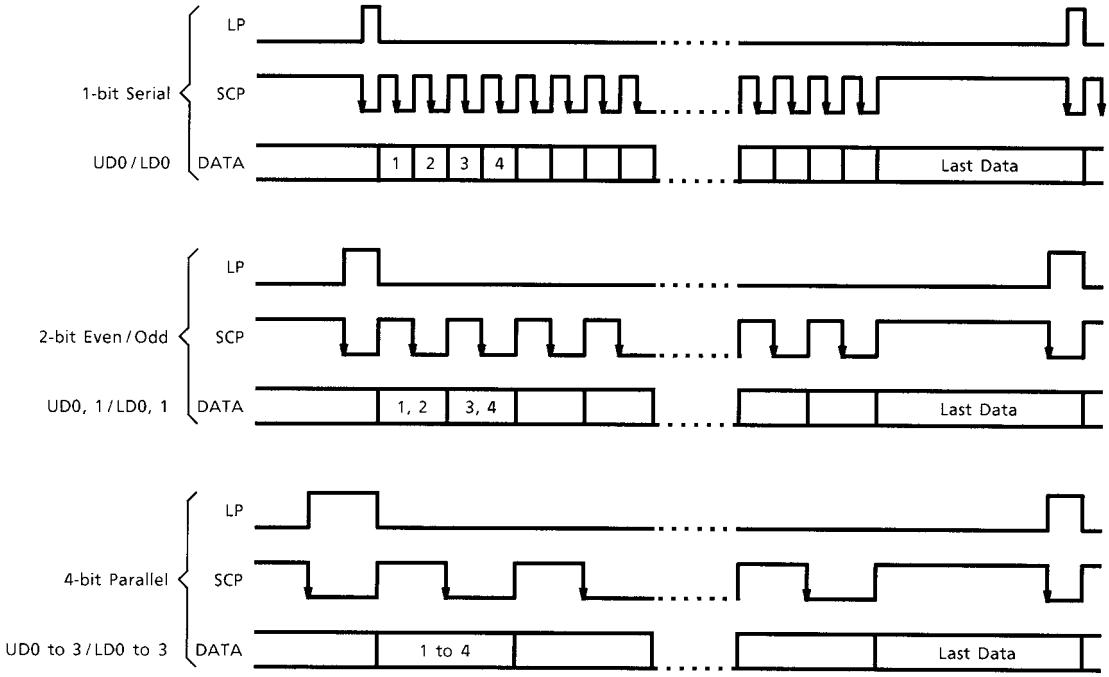
The resistance−mixing circuit generates a monochrome composite signal.



(2) LCD

You can connect the T7779 (directly or through a CMOS buffer) to various types of LCD module that are on the market, and make various settings, such as 1 or 2 screens, the number of data bus lines, the number of horizontal dots and the duty.

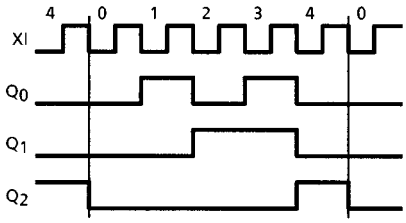
The relation between data transmission, the shift clock and latch pulse is as shown below. The shift clock frequency becomes low as the number of data lines increases. Hence it is useful for the low power system.



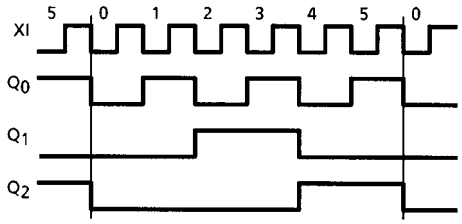
- **Timing Chart (I) (HR / LR = 1: High Resolution mode)**

(1) Internal clock (Q_1 / CLK = Q_1, Q_2 / φE = Q_2)

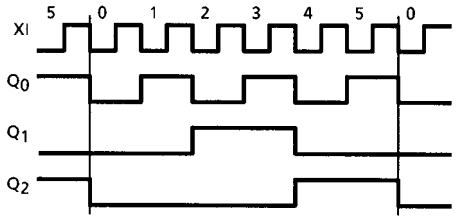
a) Hor. dots per font = 5
(HS0 = 0, HS1 = 0)



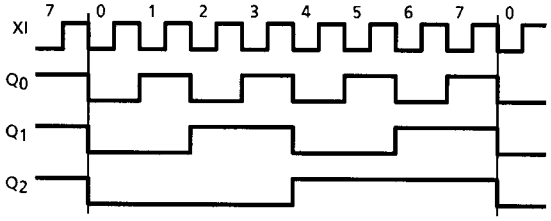
b) Hor. dots per font = 6
(HS0 = 1, HS1 = 0)



c) Hor. dots per font = 7
(HS0 = 0, HS1 = 1)

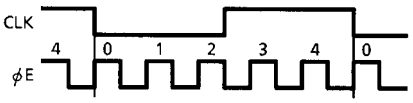


d) Hor. dots per font = 8
(HS0 = 1, HS1 = 1)

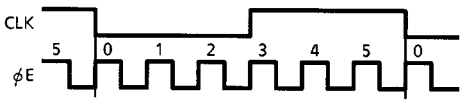


(2) External clock (Q_1 / CLK = CLK, Q_2 /φE = φE)

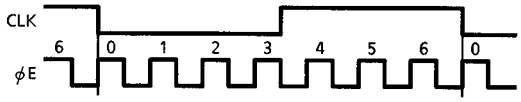
a) Hor. dots per font = 5
(HS0 = 0, HS1 = 0)



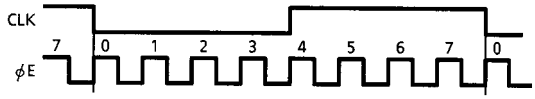
b) Hor. dots per font = 6
(HS0 = 1, HS1 = 0)



c) Hor. dots per font = 7
(HS0 = 0, HS1 = 1)



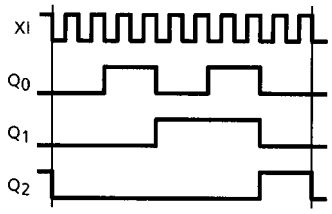
d) Hor. dots per font = 8
(HS0 = 1, HS1 = 1)



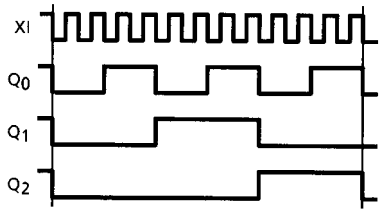
- **Timing Chart (II) (HR / LR=0: Low Resolution mode)**

(1) Internal clock (Q_1 / CLK=Q_1, Q_2 / φE = Q_2)

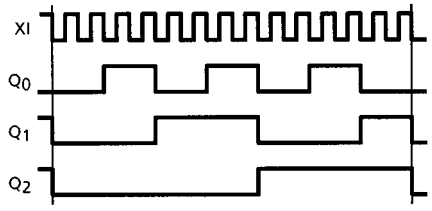
a) Hor. dots per font = 5
(HS0 = 0, HS1 = 0)



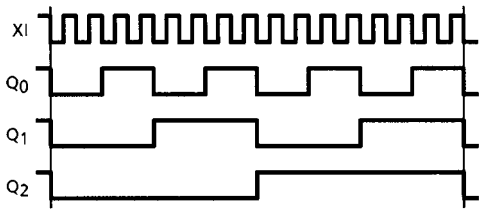
b) Hor. dots per font = 6
(HS0 = 1, HS1 = 0)



c) Hor. dots per font = 7
(HS0 = 0, HS1 = 1)



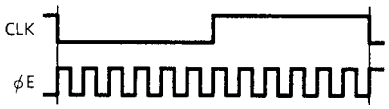
d) Hor. dots per font = 8
(HS0 = 1, HS1 = 1)



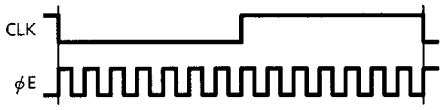
(2) External clock (Q_1 / CLK = CLK, Q_2 / φE = φE)

a) Hor. dots per font = 5
(HS0 = 0, HS1 = 0)

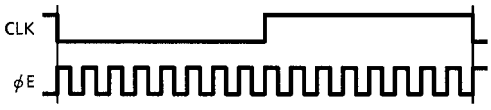
b) Hor. dots per font = 6
(HS0 = 1, HS1 = 0)



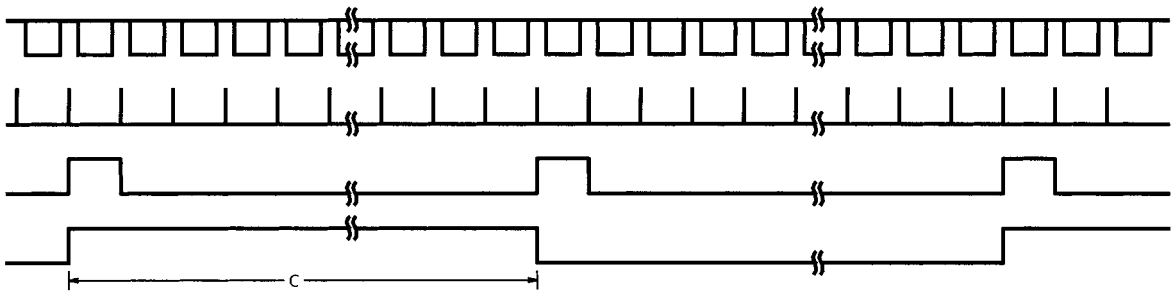
c) Hor. dots per font = 7
(HS0 = 0, HS1 = 1)



d) Hor. dots per font = 8
(HS0 = 1, HS1 = 1)



- **Timing chart (III)**



C : $1 / (2 \cdot f_{FR})$ = Hor. dots per font × Columns × Ver. dots per font × Rows × $2 / f_{OSC}$
f_{FR} : Frame frequency
Columns : Total number of horizontal characters
Rows : Total number of vertical characters
f_{OSC} : Oscillator frequency
$f_{OSC} = f\phi = 2 \cdot SCP$ (1-bit mode)
$= 4 \cdot SCP$ (2-bit mode)
$= 8 \cdot SCP$ (4-bit mode)

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{DD} (Note)	−0.3 to 7.0	V
Input Voltage	V_{IN} (Note)	−0.3 to V_{DD} +0.3	V
Operating Temperature	T_{opr}	−20 to 75	°C
Storage Temperature	T_{stg}	−55 to 125	°C

Note: Referenced to V_{SS} = 0 V

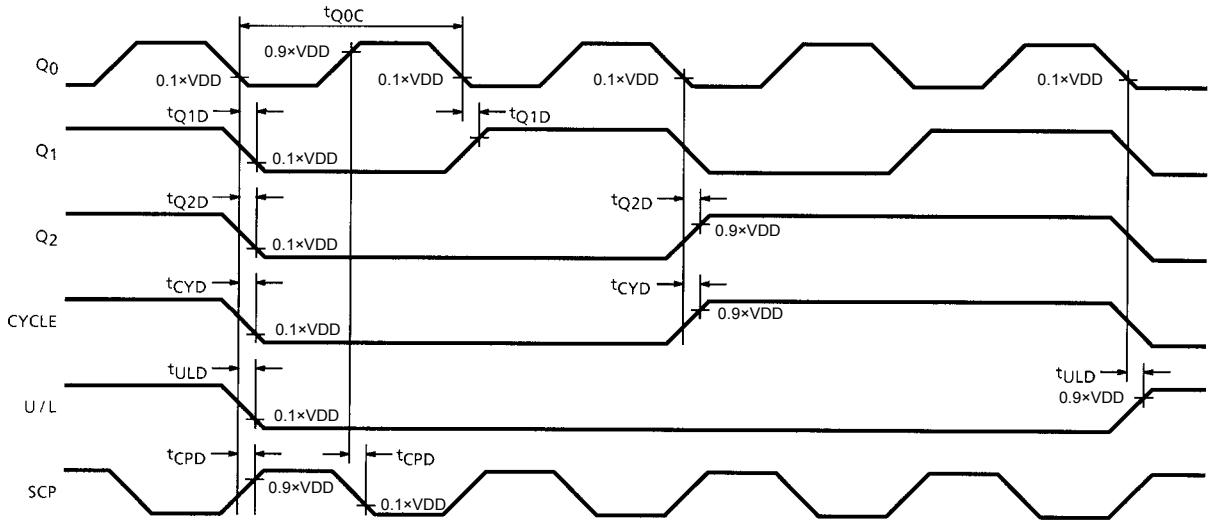
Electrical Characteristics
DC Characteristics
Test Conditions (Unless otherwise noted, V_{SS} = 0V, V_{DD} = 5.0 V ± 10%, Ta = −20 to 75°C)

Item		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	
Operating Voltage		V_{DD}	—	—	4.5	5.0	5.5	V	—
Input Voltage	H Level	V_{IH}	—	—	V_{DD} − 0.8	—	V_{DD}	V	(Note 1)
	L Level	V_{IL}	—	—	0	—	0.8	V	(Note 1)
Input Voltage	H Level	V_{IH}	—	—	2.2	—	V_{DD}	V	(Note 2)
	L Level	V_{IL}	—	—	0	—	0.8	V	(Note 2)
Output Voltage	H Level	V_{OH}	—	—	V_{DD} − 0.3	—	V_{DD}	V	—
	L Level	V_{OL}	—	—	0	—	0.3	V	—
Output Resistance	H Level	R_{OH}	—	V_{OUT} = V_{DD} − 0.5 V	—	—	400	Ω	—
	L Level	R_{OL}	—	V_{OUT} = 0.5 V	—	—	400	Ω	—
Operating Frequency		fφ	—	—	—	—	18	MHz	(Note 3)
		f_{CLK}	—	—	—	—	4.0	MHz	(Note 4)
Current Consumption		I_{DD}	—	V_{DD} = 5.0 V	—	4.0	6.0	mA	(Note 5)

Note 1: Applied to EXT / INT, HS0, HS1, LD3 / DSC0, DSC1, $\overline{TEST1}$
Note 2: Applied to inputs other than those marked Note 1:
Note 3: Applied to Q_2 / φE
Note 4: Applied to Q_1 / CLK
Note 5: LCD, High Resolution, 2−bit transfer, 8 dots / font
640 × 104 × 2 screens, fφ = 9 MHz

AC Characteristics

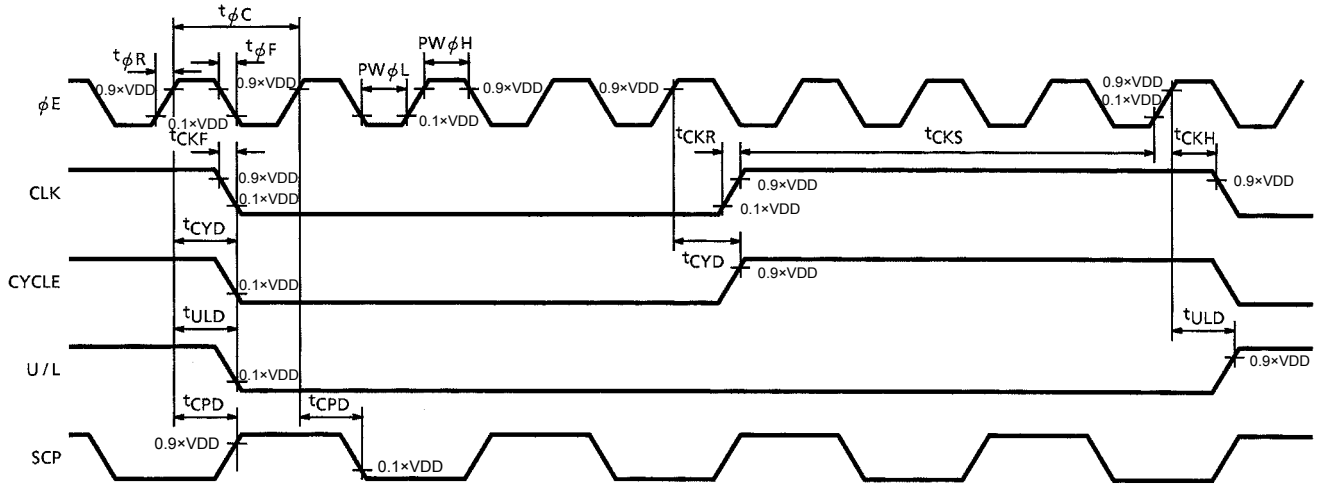
- **CRT / LCD = 1 (LCD mode), EXT / INT = 1 (Internal clock)**



Test Conditions (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, Ta = −20 to 75°C)

Item	Symbol	Test Conditions	Min	Max	Unit
Q_0 Cycle Time	t_{Q0C}	—	111	—	ns
Q_1 Delay Time	t_{Q1D}	—	—	20	ns
Q_2 Delay Time	t_{Q2D}	—	—	20	ns
CYCLE Delay Time	t_{CYD}	—	—	20	ns
U / L Delay Time	t_{ULD}	—	—	20	ns
SCP Delay Time	t_{CPD}	—	—	10	ns

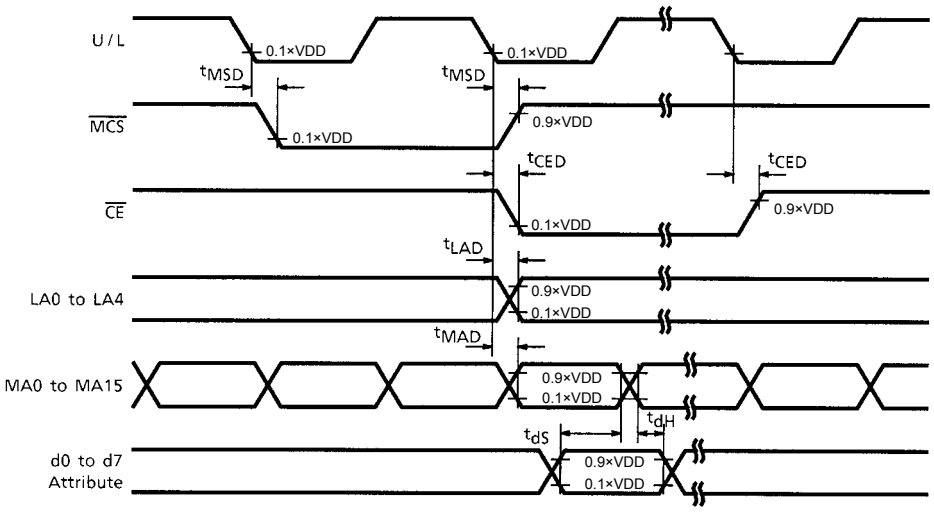
- **CRT / LCD = 1 (LCD mode), EXT / INT = 0 (External clock)**



Test Conditions (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, Ta = −20 to 75°C)

Item	Symbol	Test Conditions	Min	Max	Unit
φE Cycle Time	$t_{\varphi C}$	—	55.5	—	ns
φE 1 Pulse Width	PWφH	—	7.75	—	ns
φE 0 Pulse Width	PWφL	—	7.75	—	ns
φE Rise and Fall Time	$t_{\varphi R}$, $t_{\varphi F}$	—	—	20	ns
CLK Rise and Fall Time	t_{CKR}, t_{CKF}	—	—	20	ns
CLK Set−up Time	t_{CKS}	—	80	—	ns
CLK Hold Time	t_{CKH}	—	10	—	ns
CYCLE Delay Time	t_{CYD}	—	—	80	ns
U / L Delay Time	t_{ULD}	—	—	80	ns
SCP Delay Time	t_{CPD}	—	—	80	ns

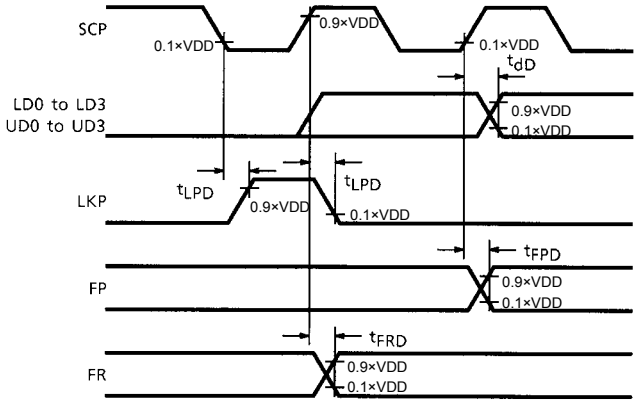
- **CRT / LCD = 1 (LCD mode)**



Test Conditions (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, Ta = −20 to 75°C)

Item	Symbol	Test Conditions	Min	Max	Unit
$\overline{MCS}$ Delay Time	t_{MSD}	—	—	80	ns
$\overline{CE}$ Delay Time	t_{CED}	—	—	100	ns
LA Delay Time	t_{LAD}	—	—	70	ns
MA Delay Time	t_{MAD}	—	—	50	ns
Data Set−up Time	t_{dS}	f_{OSC} = 10MHz	200	—	ns
Data Hold Time	t_{dH}	f_{OSC} = 10MHz	0	—	ns

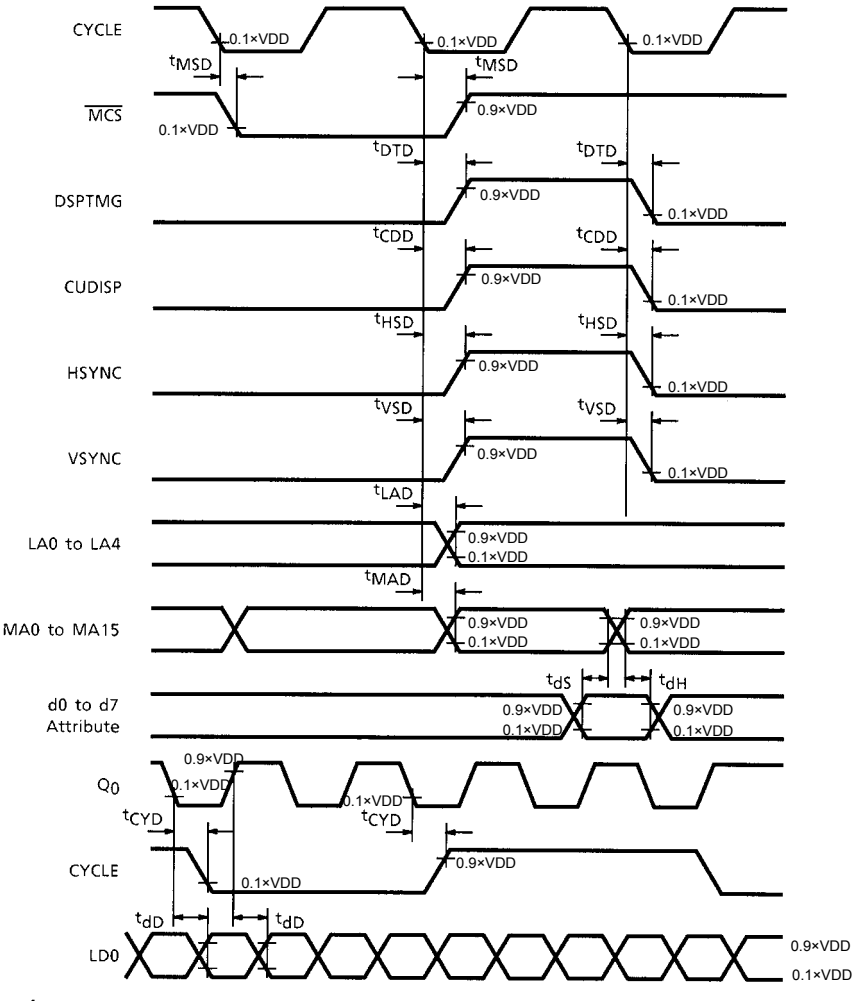
- **CRT / LCD = 1 (LCD mode)**



Test Conditions (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, Ta = −20 to 75°C)

Item	Symbol	Test Conditions	Min	Max	Unit
Data Delay Time	t_{dD}	—	—	20	ns
LP Delay Time	t_{LPD}	—	—	20	ns
FP Delay Time	t_{FPD}	—	—	20	ns
FR Delay Time	t_{FRD}	—	—	20	ns

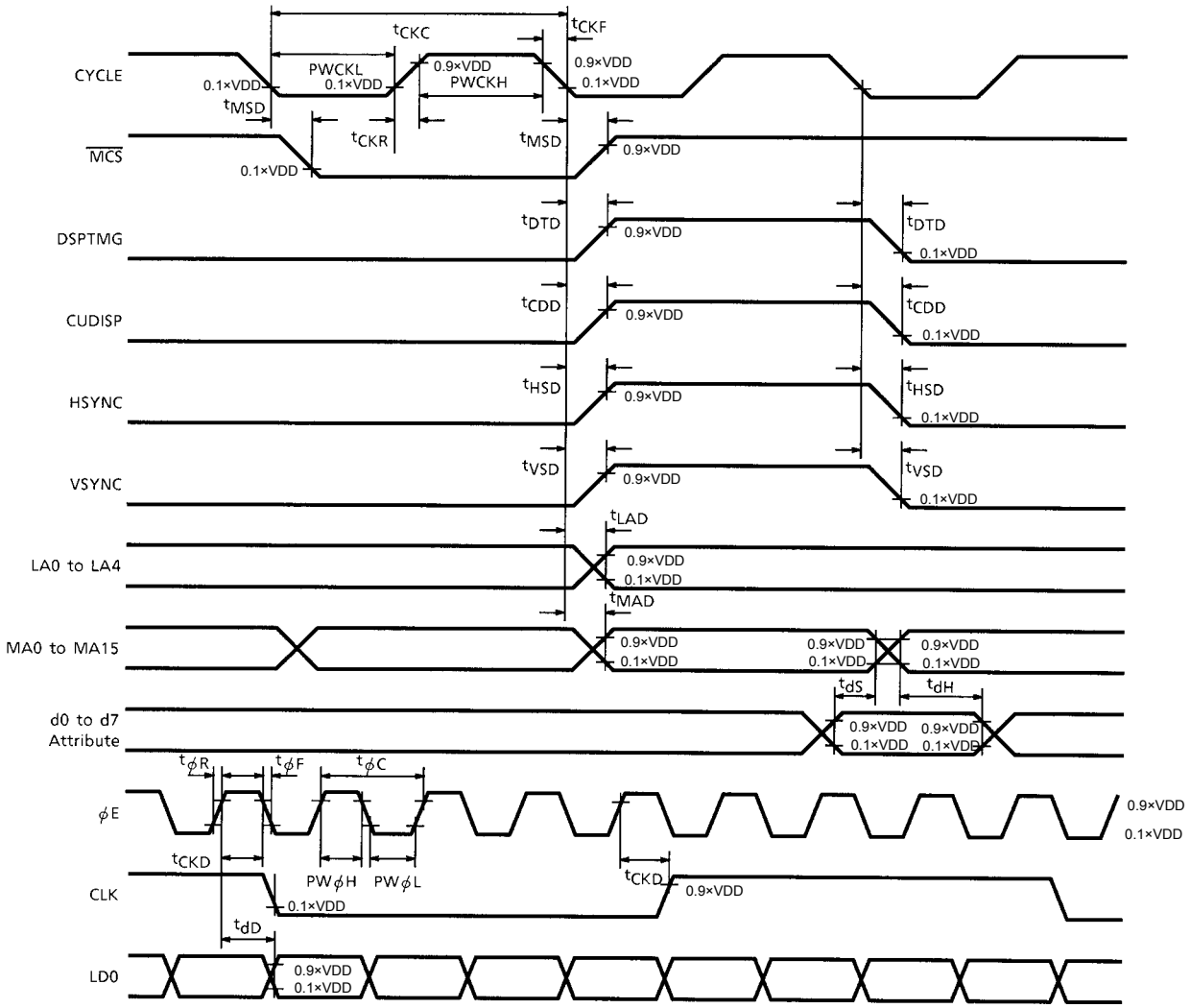
- **CRT / LCD = 0 (CRT mode), EXT / INT = 1 (Internal clock)**



Test Conditions (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, Ta = −20 to 75°C)

Item	Symbol	Test Conditions	Min	Max	Unit
$\overline{MCS}$ Delay Time	t_{MSD}	—	—	80	ns
DSPTMG Delay Time	t_{DTD}	—	—	100	ns
CUDISP Delay Time	t_{CDD}	—	—	100	ns
HSYNC Delay Time	t_{HSD}	—	—	80	ns
VSYNC Delay Time	t_{VSD}	—	—	100	ns
LA Delay Time	t_{LAD}	—	—	80	ns
MA Delay Time	t_{MAD}	—	—	100	ns
Data Set−up Time	t_{dS}	f_{OSC} = 10MHz	200	—	ns
Data Hold Time	t_{dH}	f_{OSC} = 10MHz	0	—	ns
CYCLE Delay Time	t_{CYD}	—	—	20	ns
Data Delay Time	t_{dD}	—	—	110	ns

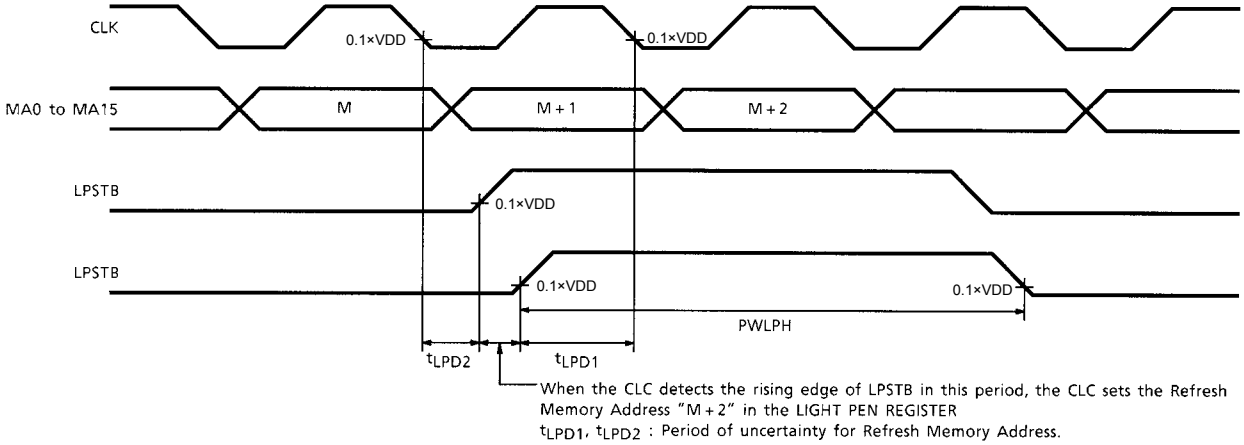
- **CRT / LCD = 0 (CRT mode), EXT / INT = 0 (External clock)**



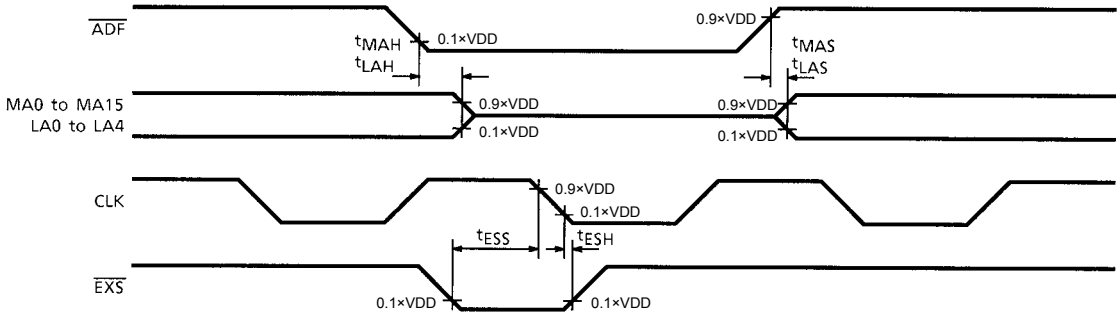
Test Conditions (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, Ta = −20 to 75°C)

Item	Symbol	Test Conditions	Min	Max	Unit
CLK Cycle Time	t_{CKC}	—	222	—	ns
CLK 1 Pulse Width	PWCKH	—	91	—	ns
CLK 0 Pulse Width	PWCKL	—	91	—	ns
CLK Rise and Fall Time	t_{CKR}, t_{CKF}	—	—	20	ns
$\overline{MCS}$ Delay Time	t_{MSD}	—	—	120	ns
DSPTMG Delay Time	t_{DTD}	—	—	140	ns
CUDISP Delay Time	t_{CDD}	—	—	140	ns
HSYNC Delay Time	t_{HSD}	—	—	120	ns
VSYNC Delay Time	t_{VSD}	—	—	130	ns
LA Delay Time	t_{LAD}	—	—	110	ns
MA Delay Time	t_{MAD}	—	—	140	ns
Data Set−up Time	t_{dS}	f_{OSC} = 10 MHz	200	—	ns
Data Hold Time	t_{dH}	f_{OSC} = 10 MHz	0	—	ns
φE Cycle Time	$t\varphi_C$	—	55.5	—	ns
φE 1 Pulse Width	PWφH	—	7.75	—	ns
φE 0 Pulse Width	PWφL	—	7.75	—	ns
φE Rise and Fall Time	$t\varphi_R$, $t\varphi_F$	—	—	20	ns
CLK Delay Time	t_{CKD}	—	10	—	ns
Data Delay Time	t_{dD}	—	—	160	ns

- **LPSTB timing**



- $\overline{\text{ADF}}$, $\overline{\text{EXS}}$ **timing**

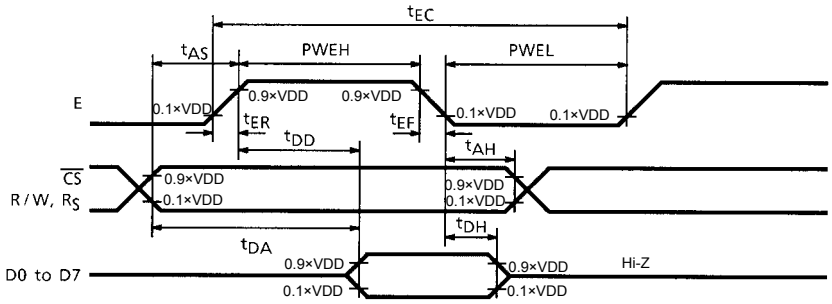


Test Conditions (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, Ta = −20 to 75°C)

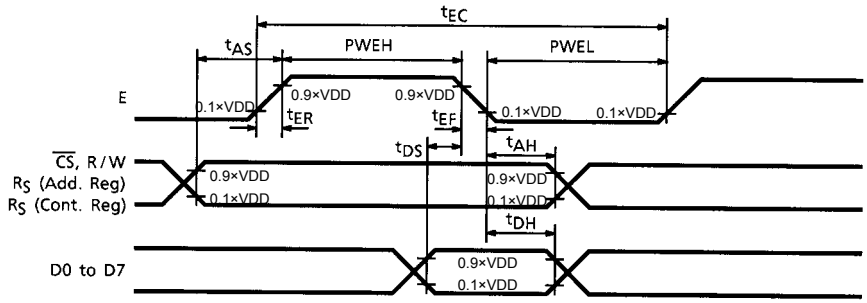
Item	Symbol	Test Conditions	Min	My	Unit
LPSTB Minimum Pulse Width	PWLPH	—	60	—	ns
LPSTB Disable Time	t_{LPD1}	—	—	20	ns
	t_{LPD2}	—	—	20	ns
MA Hold Time	t_{MAH}	—	—	50	ns
LA Hold Time	t_{LAH}	—	—	50	ns
MA Set−up Time	t_{MAS}	—	—	60	ns
LA Set−up Time	t_{LAS}	—	—	60	ns
$\overline{\text{EXS}}$ Set−up time	t_{ESS}	—	20	—	ns
$\overline{\text{EXS}}$ Hold Time	t_{ESH}	—	40	—	ns

- **BUS timing**

(1) Read sequence



(2) Write sequence



Test Conditions (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, Ta = −20 to 75°C)

CPU read timing

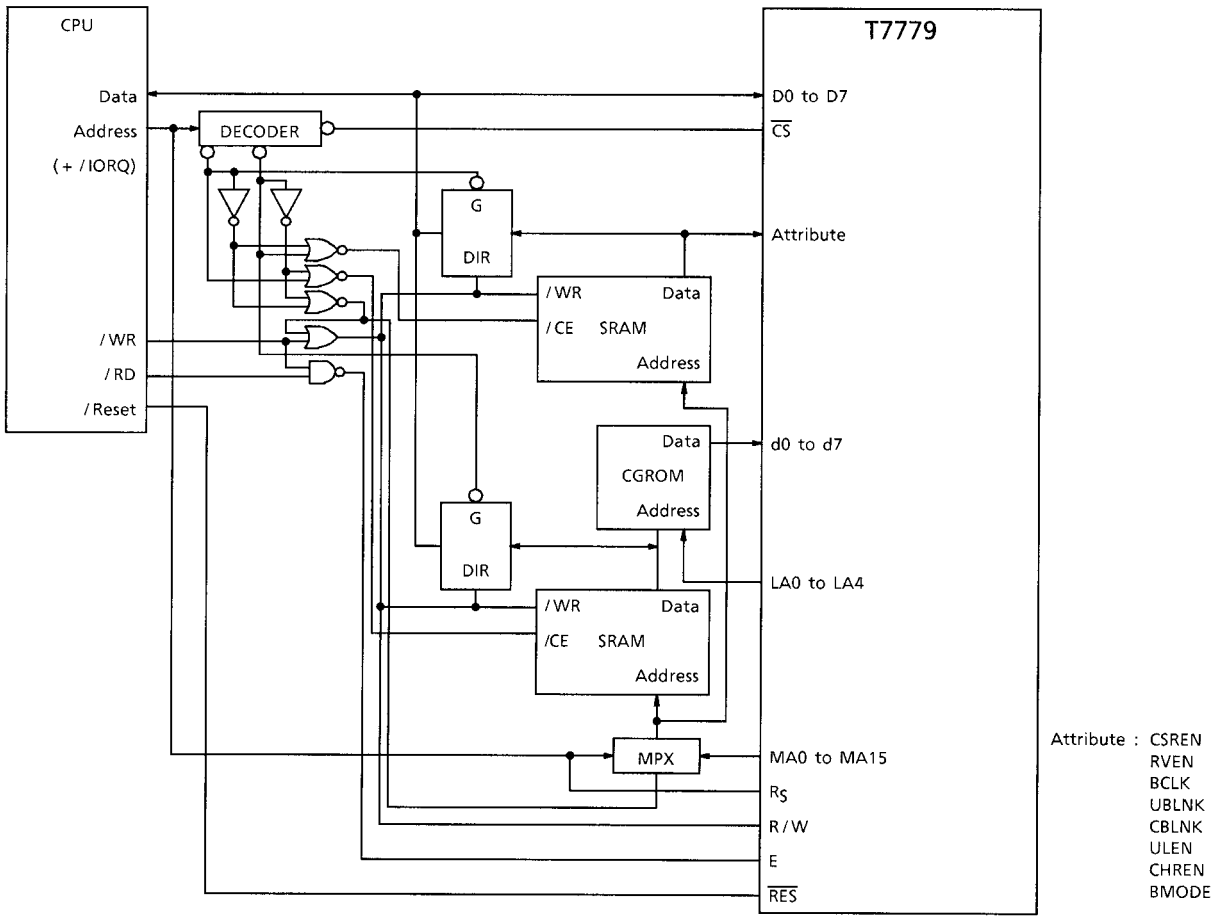
Item	Symbol	Test Conditions	Min	Max	Unit
E Cycle Time	t_{EC}	—	500	—	ns
E 1 Pulse Width	PWEH	—	220	—	ns
E 0 Pulse Width	PWEL	—	210	—	ns
E Rise and Fall Time	t_{ER}, t_{EF}	—	—	25	ns
Address Set−up Time	t_{AS}	—	70	—	ns
Data Delay Time	t_{DD}	CL=50pF	—	180	ns
Data Hold Time	t_{DH}	—	10	—	ns
Address Hold Time	t_{AH}	—	10	—	ns
Data Access Time	t_{DA}	—	—	250	ns

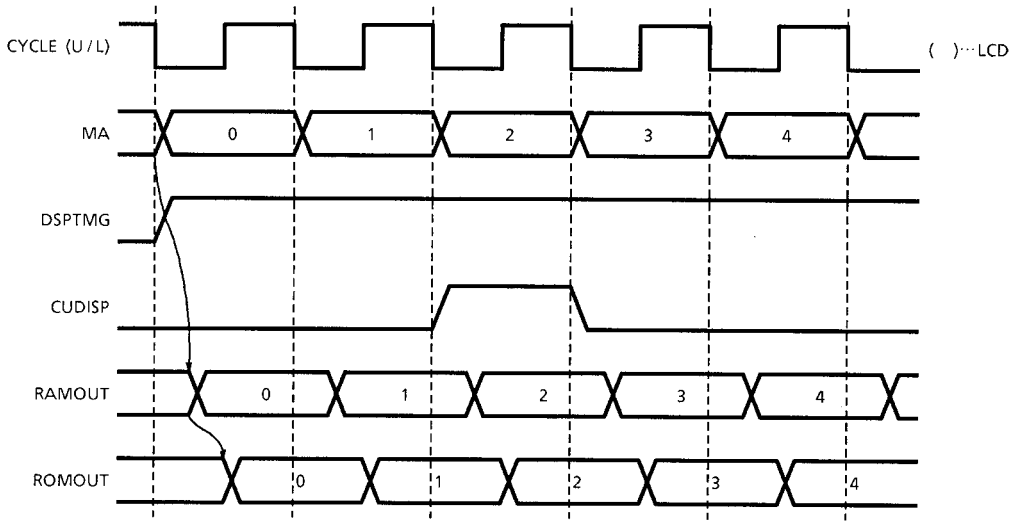
CPU write timing

Item	Symbol	Test Conditions	Min	Max	Unit
E Cycle Time	t_{EC}	—	500	—	ns
E 1 Pulse Width	PWEH	—	220	—	ns
E 0 Pulse Width	PWEL	—	210	—	ns
E Rise and Fall Time	t_{ER}, t_{EF}	—	—	25	ns
Address Set−up Time	t_{AS}	—	70	—	ns
Data Set−up Time	t_{DS}	—	60	—	ns
Data Hold Time	t_{DH}	—	10	—	ns
Address Hold Time	t_{AH}	—	10	—	ns

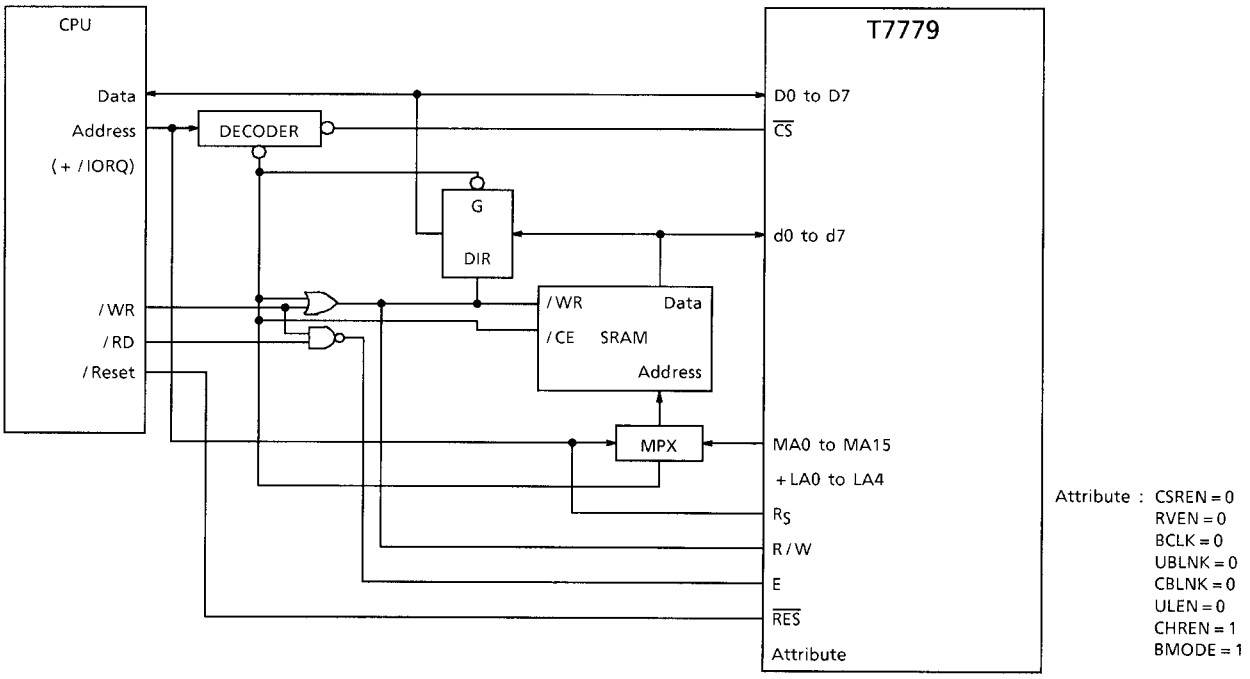
System Construction

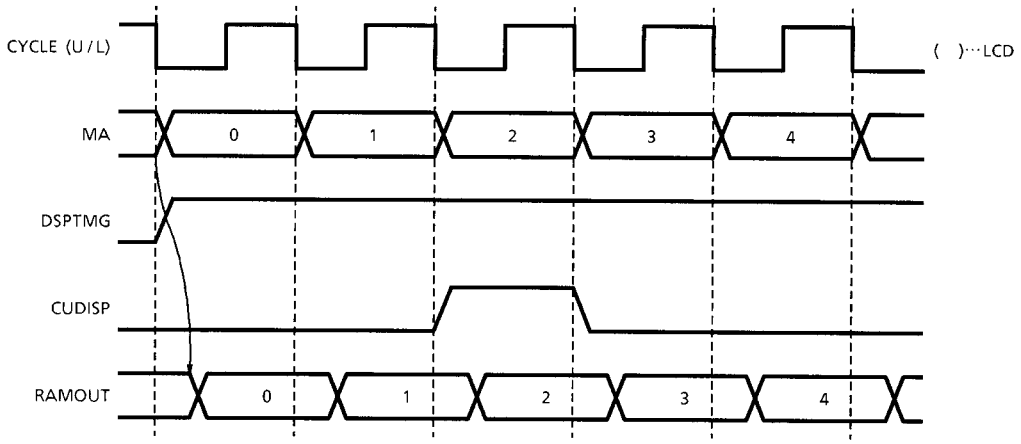
- **CG ROM + attribute RAM**



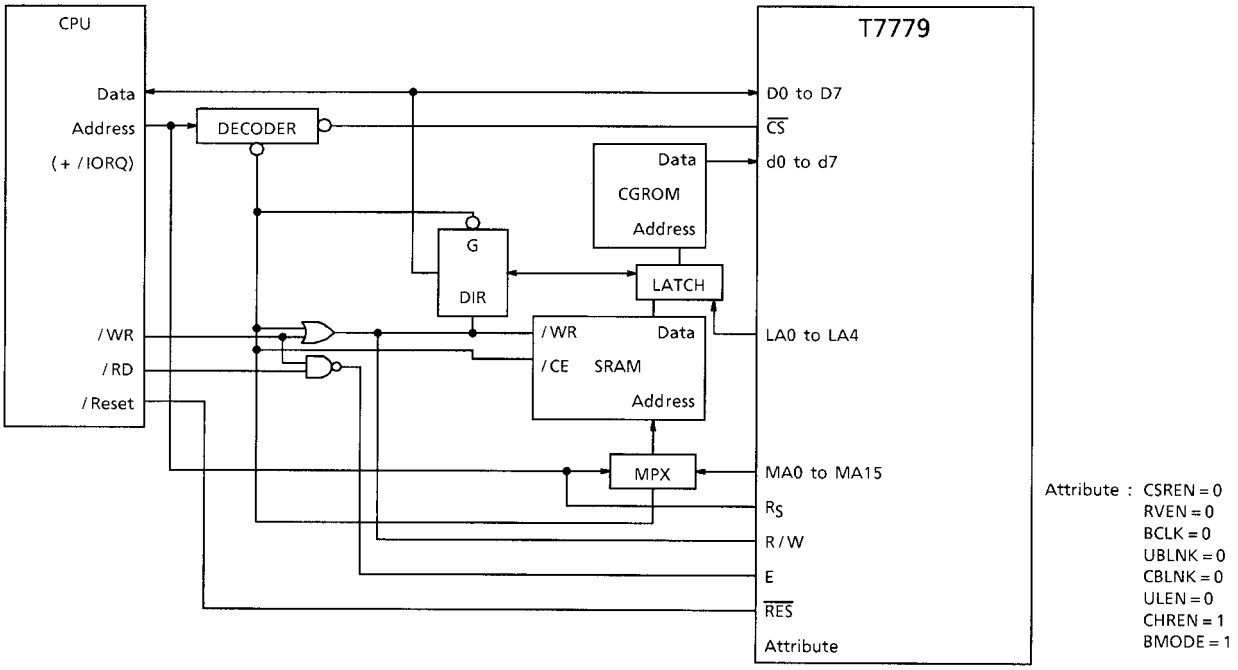


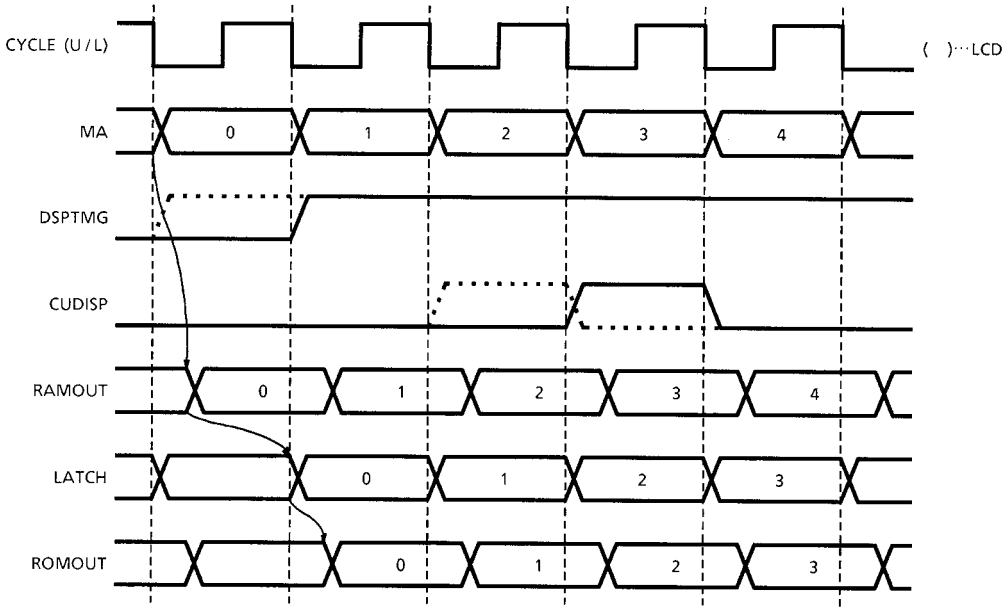
- **Bit map RAM**


CPU
Data
Address
(+ /IORQ)
/WR
/RD
/Reset
DECODER
G
DIR
/WR
/CE
SRAM
Data
Address
MPX
T7779
D0 to D7
CS
d0 to d7
MA0 to MA15
+LA0 to LA4
RS
R/W
E
RES
Attribute
Attribute : CSREN = 0
RVEN = 0
BCLK = 0
UBLNK = 0
CBLNK = 0
ULEN = 0
CHREN = 1
BMODE = 1

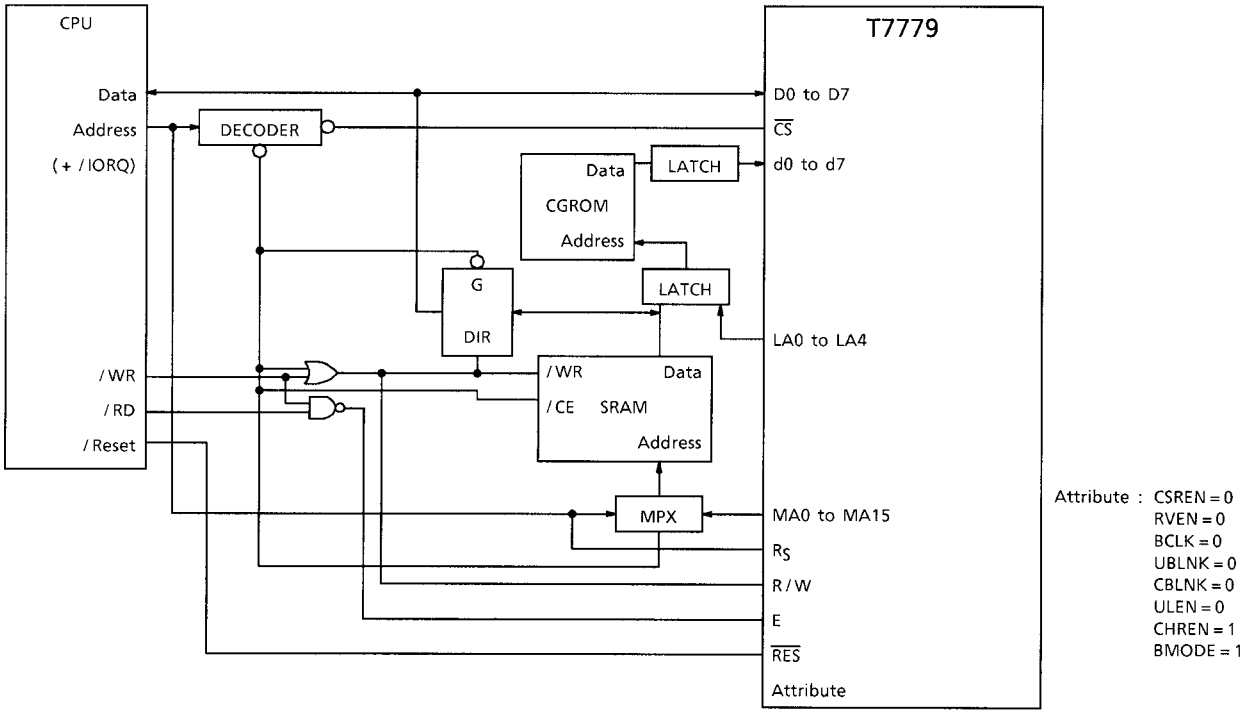

CYCLE (U/L)
( )···LCD
MA
0
1
2
3
4
DSPTMG
CUDISP
RAMOUT
0
1
2
3
4

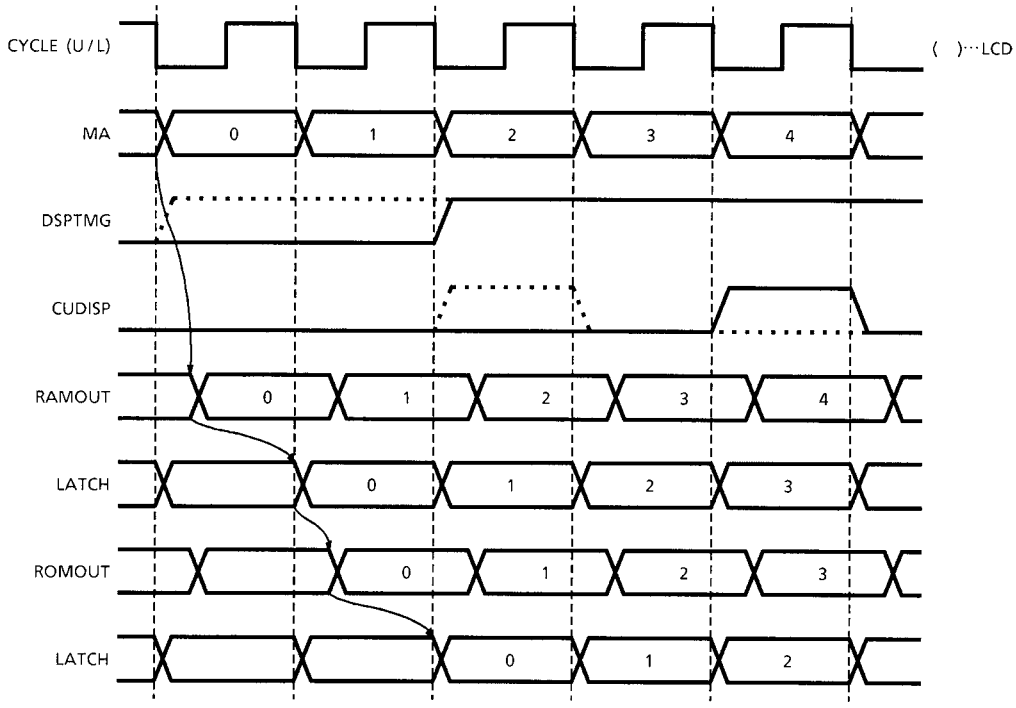
- **CG ROM (1−character skew)**





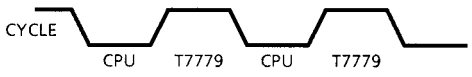
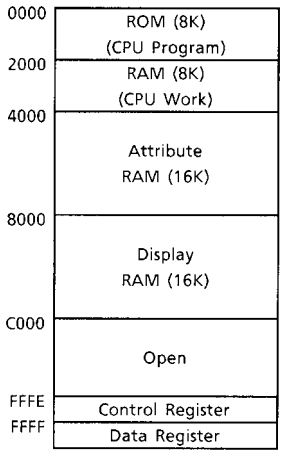
- **CG ROM (2−character skew)**





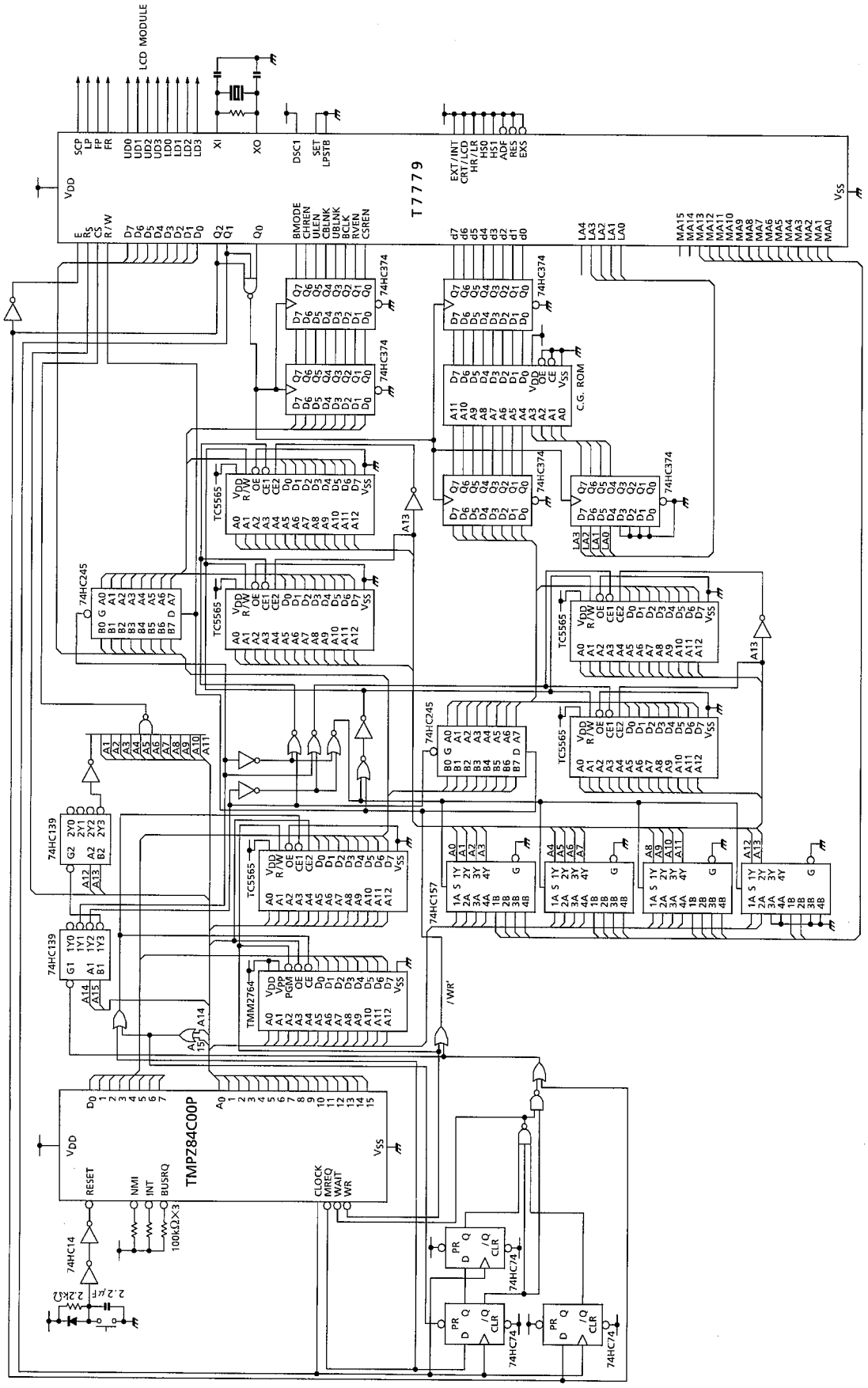
Application Circuit ··· 640 × 400 (1 / 200 duty) LCD

An application circuit for an LCD is shown overleaf.

Item	Specification
Character Font	8 × 8 dots
Displayed Chars	80 columns × 50 rows = 4000 characters
Refresh Memory Access Method	Synchronous 
Address Map	
Skew	1 character

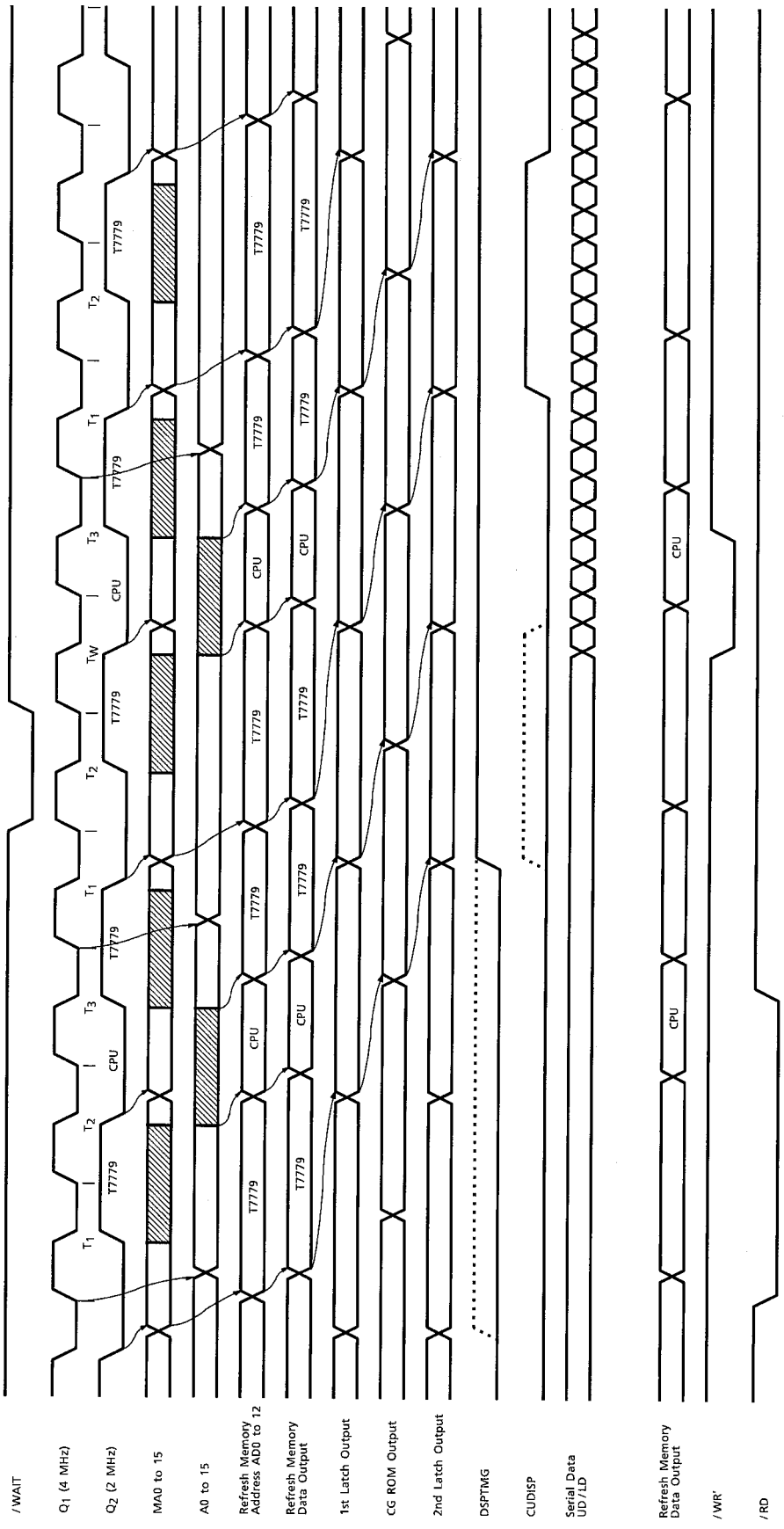
	LCD Specification
Dot Size	640 × 400
Duty	1/200
Frame Frequency	60 Hz
Dot Frequency	16 MHz
Character Font	8 × 8
Displayed Chars	80 × 50
Cursor Mode	Scan Line 0 to 7, Non−Blink

T7779 Initial Data			
Reg. No.	Register Name	SYM.	Value (HEX.)
R_0	Horizontal Total	Nht	52H
R_1	Horizontal Displayed	Nhd	50H
R_2	Horizontal Sync. Position	Nhsp	50H
R_3	Sync. Width	Nvsw Nhsw	11H
R_4	Vertical Total	Nvt	18H
R_5	Vertical Total Adjust	Nadj	00H
R_6	Vertical Displayed	Nvd	FFH
R_7	Vertical Sync. Position	Nvsp	FFH
R_8	Interlace Mode and Skew	—	50H
R_9	Max Scan Line Address	Nr	07H
R_{10}	Cursor Start	Ncsr	00H
R_{11}	Cursor End	Ncer	07H
R_{12}	Start Address (H)	—	00H
R_{13}	Start Address (L)	—	00H
R_{14}	Cursor Address (H)	—	00H
R_{15}	Cursor Address (L)	—	00H
R_{16}	Light Pen (H)	—	—
R_{17}	Light Pen (L)	—	—
R_{18}	SCP Start Position	Nssp	80H
R_{19}	SCP End Position	Nsep	50H
R_{20}	Display Start Position	Ndsp	00H
R_{21}	Display End Position	Ndep	50H
R_{22}	Additional Address (H)	—	07H
R_{23}	Additional Address (L)	—	D0H



Lcd control Logic Using T7779

Timing Chart



```
                                                ;
;       T7779 DEMO SET PROGRAM VER1.00
;       SOURCE PROGRAM for TMPZ84C00P
;              15-FEB.-1991
;
;       REGISTER NUMBER DEFINITION
;
CMD     EQU     OFFFEH            ;COMMAND REG.
DAT     EQU     OFFFEH            ;DATA REG.
ATRAM   EQU     4000H             ;ATTRIBUTE RAM ADDRESS
DPRAM   EQU     8000H             ;DISPLAY RAM ADDRESS
;
;       MAIN PROGRAM
;
        ORG     0000H
START:  LD      SP, 3FFFH         ;INIT STACPOINT
        LD      HL, CMD           ;HL < - COMMAND REG. ADDRESS
        LD      D, 00H
        LD      BC, TBL           ;BC < - REGISTER DATA ADDRESS
LOOP1:  LD      (HL), D           ;SET REGISTER NO.
        LD      A, (BC)
        LD      (DAT), A          ;SET REGISTER DATA
        INC     BC                ;INC REGISTER DATA ADDRESS
        INC     D                 ;INC REGISTER NO.
        LD      A, D
        CP      18H               ;LAST REGISTER ?
        JP      NZ, LOOP1
        LD      HL, ATRAM         ;HL < - ATTRIBUTE RAM ADDRESS
        LD      A, 80H            ;ATTRIBUTE RAM END ADDRESS
        LD      B, 40H            ;CHREN = "H"
LOOP2:  LD      (HL), B
        INC     HL
        CP      H                 ;END ADDRESS ?
        JP      NZ, LOOP2
        LD      BC, 4000          ;LOOP COUNT
        LD      DE, DPRAM         ;DE < - DISPLAY RAM ADDRESS
        LD      HL, DISP          ;HL < - DISPLAY DATA ADDRESS
        LDIR                      ;BLOCK TRANS.
        HALT                      ;END OF PROGRAM
```

```
;
;       REGISTER DATA
;
TBL:    DEFB    52H, 50H, 50H, 11H, 18H, 00H, OFFH, OFFH, 50H, 07H, 60H, 07H
        DEFB    00H, 00H, 00H, 00H, 00H, 00H, 80H, 50H, 00H, 50H, 07H, 0D0H
;
;       DISPLAY DATA
;
DISP:   DEFB    "                  T7779 (CRT / LCD CONTROLLER)                          "
        DEFB    "                                                                        "
        DEFB    "1. GENERAL DESCRIPTION                                                 "
        DEFB    "                                                                        "
        DEFB    "   The T7779 is a controller LSI for a raster-scan-type CRT display    "
        DEFB    "                                                                        "
        DEFB    "  and large-scale dot matrix LCD. It can be used in applications        "
        DEFB    "                                                                        "
        DEFB    "  ranging from small-scale character display systems to large-scale     "
        DEFB    "                                                                        "
        DEFB    "  graphic display systems.                                              "
        DEFB    "                                                                        "
        DEFB    "2. FEATURES                                                            "
        DEFB    "                                                                        "
        DEFB    "   a) Refresh memory address               : MA0-MA15                   "
        DEFB    "                                                                        "
        DEFB    "   b) Line scanning address                : LA0-LA4                    "
        DEFB    "                                                                        "
        DEFB    "   c) Frame buffer capacity                : Max 64 KBytes (character)"
        DEFB    "                                                                        "
        DEFB    "                                           : Max 2 MBytes (graphic)     "
        DEFB    "                                                                        "
        DEFB    "   d) Number of characters per line: 1-255                              "
        DEFB    "                                                                        "
DEFB            "   e) Number of character rows: 1-255                                   "
        DEFB    "                                                                        "
        DEFB    "   f) Scrolling, Paging                                                 "
        DEFB    "                                                                        "
        DEFB    "   g) Light pen                                                         "
        DEFB    "                                                                        "
```

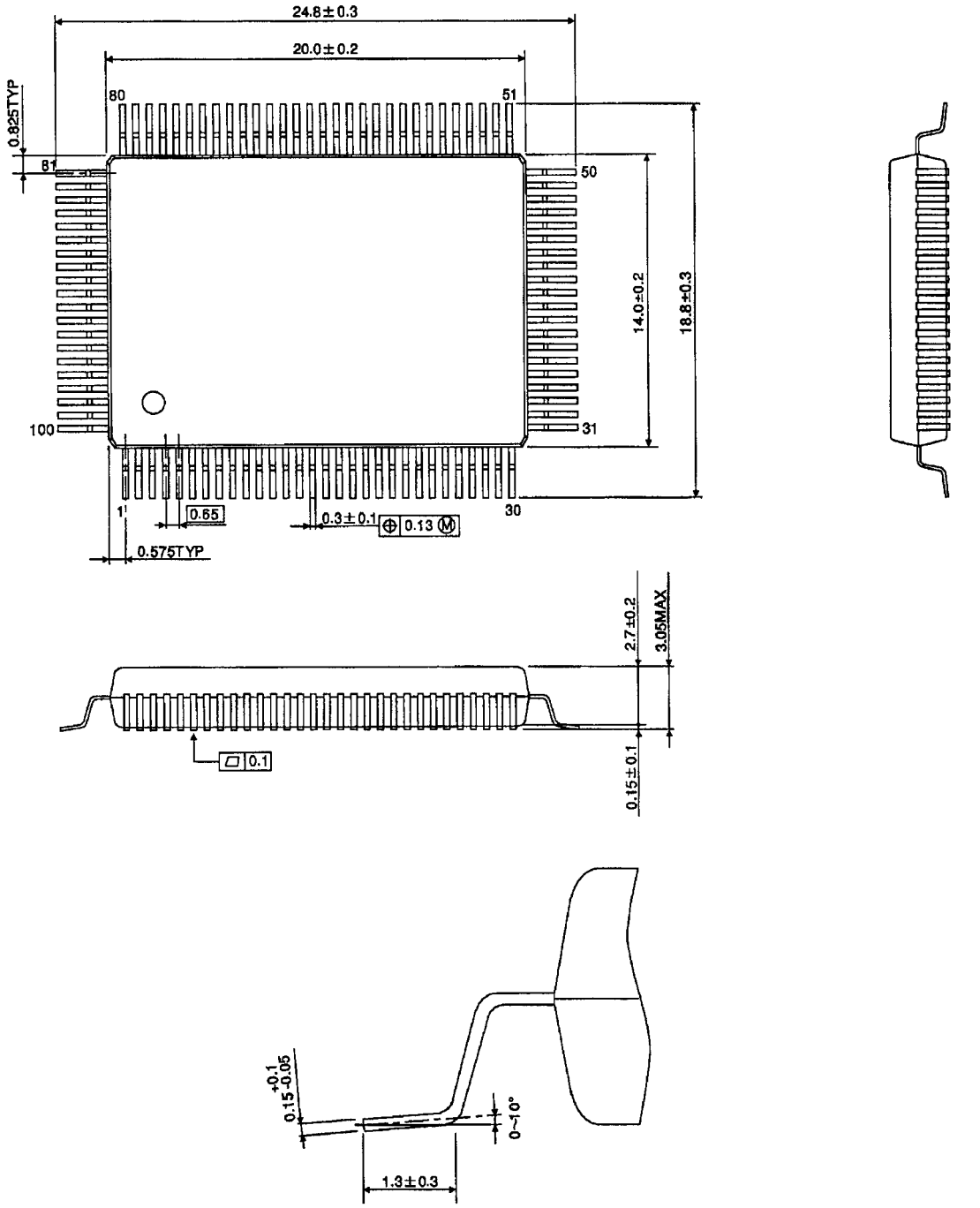
```
DEFB    "   h) Horizontal dots per character according to font: 5, 6, 7, 8       "
DEFB    "                                                                        "
DEFB    "   i) Vertical dots per character according to font: 1 to 32            "
DEFB    "                                                                        "
DEFB    "   j) Data output: 1-bit output, 2-bit (odd / even) output, 4-bit output"
DEFB    "                                                                        "
DEFB    "   k) Various attribute functions: Underline Cursor ON / OFF            "
DEFB    "                                                                        "
DEFB    "                              Underline Cursor Blink                    "
DEFB    "                                                                        "
DEFB    "                              Character ON / OFF                        "
DEFB    "                                                                        "
DEFB    "                              Character Normal / Inverse                "
DEFB    "                                                                        "
DEFB    "                              Character Blink                           "
DEFB    "                                                                        "
DEFB    "                              Blink Frequency Change                    "
DEFB    "                                                                        "
DEFB    "                                                                        "
DEFB    "                                                                 END!!"


END
```

Package Dimensions

QFP100-P-1420-0.65J

Unit : mm



Weight : 1.6g (Typ.)

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000707EBA

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