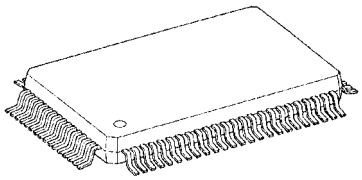
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T7934

DOT MATRIX LCD CONTROLLER AND DRIVER LSI

The T7934 is a dot matrix LCD controller. The T7934 realizes low power consumption for an LCD system using high speed CMOS silicon gate technology. The T7934 can display alphanumerics, kana and symbols, corresponding to the data received from a 4/8-bit MPU.
The T7934 has all the functions in one-chip to drive a dot matrix LCD. Therefore, the T7934 can constitute a minimal LCD drive and control system. The T7934 can drive the display of up to 80 characters by using an expansion driver (e.g.T6A41, T6A92).



QFP80-P-1420-0.80A

Weight: 1.5 g (typ.)

Features

- Built-in controller for character-type LCD
  (character fonts: 5 × 7, 5 × 10)
- Direct interface with 4/8-bit MPU
- Bus interface timing : 2 MHz max
- Display data RAM : 80 × 8 bits (80 characters max)
- Character generator ROM : 12000 bits (5 × 10 × 240)
  Character font ..... 5 × 10 dots × 240 characters
- Character generator RAM : 64 × 8 bits
  Character font ..... (1) 5 × 8 dots : 8 characters
  (2) 5 × 11 dots : 4 characters
- Both display data and character generator RAMs readable by MPU.
- Built-in LCD driver circuit
  40-output column driver
  16-output row driver
- Duty factor selection (programmable)
  1 / 8 duty : (5 × 7 dots + cursor) × 1 line
  1 / 11 duty : (5 × 10 dots + cursor) × 1 line
  1 / 16 duty : (5 × 7 dots + cursor) × 2 lines

Maximum number of characters displayed per line

Number of Characters	Expansion Driver	
	T6A41 (64−Output Columns)	T6A92 (80−output Columns)
8 characters × 1 line	—	—
80 characters × 1 line	6 units	5 units
8 characters × 2 lines	—	—
40 characters × 2 lines	3 units	2 units

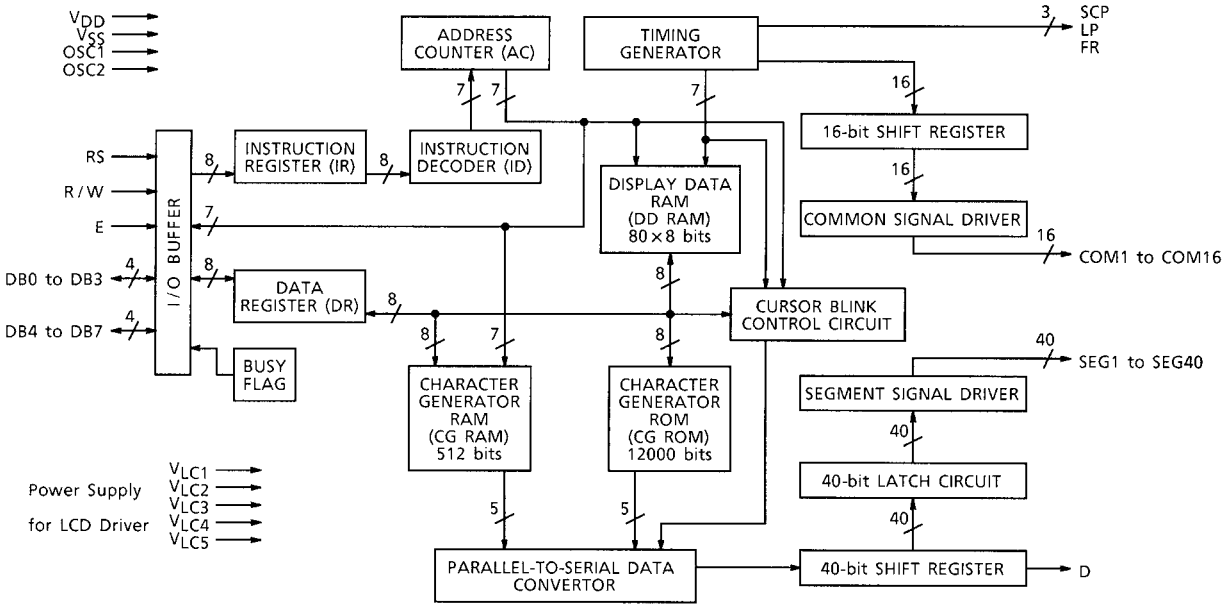
- Built−in power−on reset circuit
- Numerous functions
  Display clear, Cursor home, Display ON/OFF, Cursor ON/OFF,
  Display character blink, Display shift, Cursor shift
- Built−in clock generator (with external resistor or ceramic oscillator)
  (external clock operation possible)
- Power supply 5 V ± 10%
- Low power consumption
- Built−in resistance ladder for driver (1kΩ × 5)
- CMOS and Si−gate processes, 80−pin flat plastic package
- LSI mark

TOSHIBA
T 7 9 3 4
0000 JAPAN
8901H

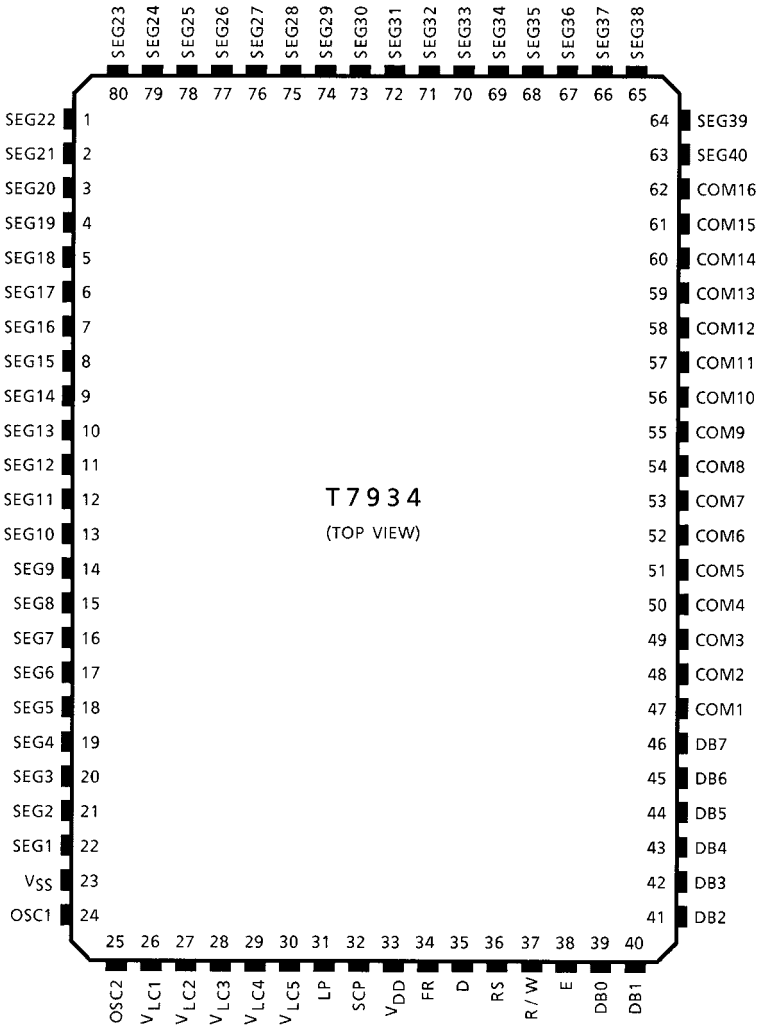
Rom Code	Column Driver	68 / 80	R.L.
0000	T6A41	68	YES
0100	T6A41	68	NO
0200	T6A41	80	YES
0300	T6A41	80	NO

Note: 68 / 80 . MPU series
R.L. ..... Built−in resistance ladder

Block Diagram (T7934 interior)



Pin Assignment



Pin Functions

(1) T7934−0000 pin functions

Symbol	Pin	Type	Name and Function
RS	36	Input	Register Select: Selects Data / Instruction register RS = 0 and R / W = 0: Instruction register is selected RS = 0 and R / W = 1: Busy flag and Address counter are selected RS = 1: Data register is selected
R / W	37	Input	Read / Write: Selects Read / Write data bus state
E	38	Input	Enable: Read / Write Enable
DB0 to DB3	39 to 42	I / O	Data Bus: Three−state bi−directional data bus (lower 4 bits) During 4−bit operation, these lines are not used
DB4 to DB7	43 to 46	I / O	Data Bus: Three−state bi−directional data bus (higher 4 bits)
LP	31	Output	Latch Pulse: Latch pulse for expansion driver
SCP	32	Output	Shift Clock Pulse: Shift clock pulse for expansion driver
FR	34	Output	Frame: Frame signal for expansion driver
D	35	Output	Data: Serial data output to the expansion driver 0: OFF 1: ON
COM1 to COM16	47 to 62	Output	Common: Row signal output 1 / 8 duty operation : COM9 to COM16 are not selected 1 / 11 duty operation: COM12 to COM16 are not selected
SEG1 to SEG40	1 to 22, 63 to 80	Output	Segment: Column signal output
V_{LC5}	30	Input	Power supply for LCD
V_{LC1} to V_{LC4}	26 to 29	Output	Power supply for LCD
V_{DD}, V_{SS}	33, 23	Input	Power supply for T7934 V_{DD} = 5.0 V ± 10% V_{SS} = 0 V
OSC1, OSC2	24, 25	—	When using the internal clock oscillator, connect a resistor or ceramic oscillator between OSC1 and OSC2 When using an external clock, connect the clock to OSC1 and leave OSC2 open

(2) T7934−0100 pin functions

Symbol	Pin	Type	Name and Function
RS	36	Input	Register Select: Selects Data / Instruction register RS = 0 and R / W = 0: Instruction register is selected RS = 0 and R / W = 1: Busy flag and Address counter are selected RS = 1: Data register is selected
R / W	37	Input	Read / Write: Selects Read / Write data bus state
E	38	Input	Enable: Read / Write Enable
DB0 to DB3	39 to 42	I / O	Data Bus: Three−state bi−directional data bus (lower 4 bits) During 4−bit operation, these lines are not used
DB4 to DB7	43 to 46	I / O	Data Bus: Three−state bi−directional data bus (higher 4 bits)
LP	31	Output	Latch Pulse: Latch pulse for expansion driver
SCP	32	Output	Shift Clock Pulse: Shift clock pulse for expansion driver
FR	34	Output	Frame: Frame signal for expansion driver
D	35	Output	Data: Serial data output to the expansion driver 0: OFF 1: ON
COM1 to COM16	47 to 62	Output	Common: Row signal output 1 / 8 duty operation : COM9 to COM16 are not selected 1 / 11 duty operation: COM12 to COM16 are not selected
SEG1 to SEG40	1 to 22,63 to 80	Output	Segment: Column signal output
V_{LC5}	30	Input	Power supply for LCD
V_{LC1} to V_{LC4}	26 to 29	Output	Power supply for LCD
V_{DD}, V_{SS}	33, 23	Input	Power supply for T7934 V_{DD} = 5.0 V ± 10% V_{SS} = 0 V
OSC1, OSC2	24, 25	—	When using the internal clock oscillator, connect a resistor or ceramic oscillator between OSC1 and OSC2 When using an external clock, connect the clock to OSC1 and leave OSC2 open

(3) T7934−0200 pin functions

Symbol	Pin	Type	Name and Function
RS	36	Input	Register Select: Selects Data / Instruction register RS = 0 and $\overline{WR}$ = 0: Instruction register is selected RS = 0 and $\overline{WR}$ = 1: Busy flag and address counter are selected RS = 1: Data register is selected
$\overline{WR}$	37	Input	Write: Selects Read / Write data bus state
$\overline{CS}$	38	Input	Chip Select: Read / Write Enable
DB0 to DB3	39 to 42	I / O	Data Bus: Three−state bi−directional data bus (lower 4 bits) During 4−bit operation, these lines are not used
DB4 to DB7	43 to 46	I / O	Data Bus: Three−state bi−directional data bus (higher 4 bits)
LP	31	Output	Latch Pulse: Latch pulse for expansion driver
SCP	32	Output	Shift Clock Pulse: Shift clock pulse for expansion driver
FR	34	Output	Frame: Frame signal for expansion driver
D	35	Output	Data: Serial data output to the expansion driver 0: OFF 1: ON
COM1 to COM16	47 to 62	Output	Common: Row signal output 1 / 8 duty operation : COM9 to COM16 are not selected 1 / 11 duty operation: COM12 to COM16 are not selected
SEG1 to SEG40	1 to 22, 63 to 80	Output	Segment: Column signal output
V_{LC5}	30	Input	Power supply for LCD
V_{LC1} to V_{LC4}	26 to 29	Output	Power supply for LCD
V_{DD}, V_{SS}	33, 23	Input	Power supply for T7934 V_{DD} = 5.0 V ± 10% V_{SS} = 0 V
OSC1, OSC2	24, 25	—	When using the internal clock oscillator, connect a resistor or ceramic oscillator between OSC1 and OSC2 When using an external clock, connect the clock to OSC1 and leave OSC2 open

(4) T7934−0300 pin functions

Symbol	Pin	Type	Name and Function
RS	36	Input	Register Select: Selects Data / Instruction register RS = 0 and $\overline{WR}$ = 0: Instruction register is selected RS = 0 and $\overline{WR}$ = 1: Busy flag and address counter are selected RS = 1: Data register is selected
$\overline{WR}$	37	Input	Write: Selects Read / Write data bus state
$\overline{CS}$	38	Input	Chip Select: Read / Write Enable
DB0 to DB3	39 to 42	I / O	Data Bus: Three−state bi−directional data bus (lower 4 bits) During 4−bit operation, these lines are not used
DB4 to DB7	43 to 46	I / O	Data Bus: Three−state bi−directional data bus (higher 4 bits)
LP	31	Output	Latch Pulse: Latch pulse for expansion driver
SCP	32	Output	Shift Clock Pulse: Shift clock pulse for expansion driver
FR	34	Output	Frame: Frame signal for expansion driver
D	35	Output	Data: Serial data output to the expansion driver 0: OFF 1: ON
COM1 to COM16	47 to 62	Output	Common: Row signal output 1 / 8 duty operation : COM9 to COM16 are not selected 1 / 11 duty operation: COM12 to COM16 are not selected
SEG1 to SEG40	1 to 22, 63 to 80	Output	Segment: Column signal output
V_{LC5}	30	Input	Power supply for LCD
V_{LC1} to V_{LC4}	26 to 29	Input	Power supply for LCD
V_{DD}, V_{SS}	33, 23	Input	Power supply for T7934 V_{DD} = 5.0 V ± 10% V_{SS} = 0 V
OSC1, OSC2	24, 25	—	When using the internal clock oscillator, connect a resistor or ceramic oscillator between OSC1 and OSC2 When using an external clock, connect the clock to OSC1 and leave OSC2 open

Function of Each Block

● Register

The T7934 has two 8−bit registers. One is an Instruction Register (IR), and the other is a Data Register (DR).
The IR stores an instruction code, DD RAM address data or CG RAM address data. The IR is a write−only register for the MPU.
The DR temporarily stores data that is to be written into or read from the DD RAM or the CG RAM. In the Write sequence, the data in the DR is automatically sent to the DD RAM or the CG RAM. In the Read sequence, when the address data has been written into the IR, the data is automatically sent to the DR from the DD RAM or the CG RAM. Therefore, the MPU can read the DD RAM or CG RAM data from the DR.
The address data is automatically incremented or decremented after a Read operation.
The relation between RS, R / W ($\overline{WR}$) and the operation is as shown below.

RS	R / W ($\overline{WR}$)	Operation
0	0	Write into IR
0	1	Read busy flag (DB7) and Address Counter (DB0 to DB6)
1	0	Write into DR
1	1	Read from DR

● Busy flag (BF)

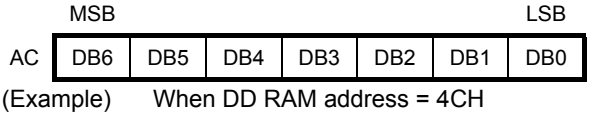
When an instruction is executed, the T7934 sets the Busy flag. The MPU reads the status of the Busy flag using the Read Busy Flag instruction. When the Busy flag is set, the T7934 cannot accept any instructions from the MPU (other than Read Busy Flag). The MPU must check the setting of the Busy flag before sending each instruction.

● Address Counter (AC)

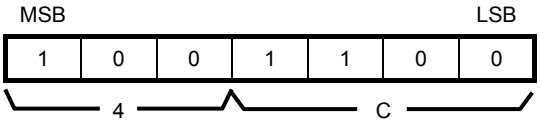
The T7934 has a 7−bit Address Counter. The Address Counter points to an address in DD RAM or CG RAM, or to the cursor position. The Set DD RAM Address or Set CG RAM Address instruction specifies which type of address Address Counter contains. The Address Counter is automatically incremented (or decremented) after the data has been written into or read from RAM. When RS = 0 and R / W ($\overline{WR}$) = 1, the contents of the Address Counter is output on DB0 to DB6.

- **Display data RAM (DD RAM)**

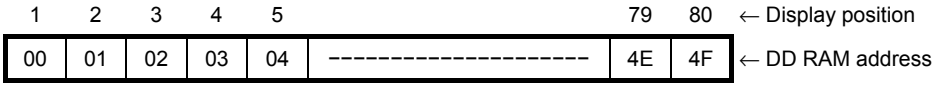
The display data RAM (DD RAM) stores the display data as 8−bit character codes. Its capacity is 80 characters × 8 bits. The relation between the DD RAM address and the display position is shown below. A DD RAM address is expressed as shown below.



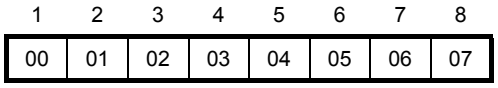
(Example) When DD RAM address = 4CH



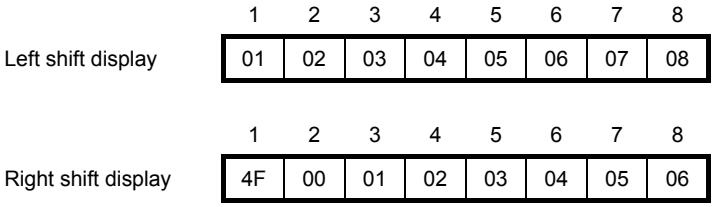
(1) The relation between the DD RAM address and the display position in 1−Line Display mode (N = 0)



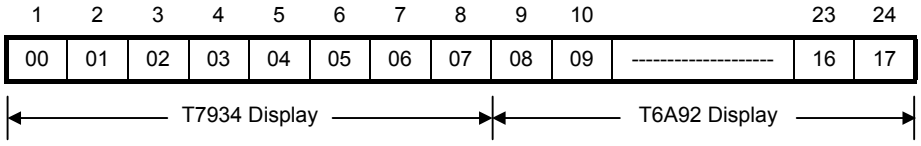
a) Using one T7934, the first 8 characters are displayed as shown below.



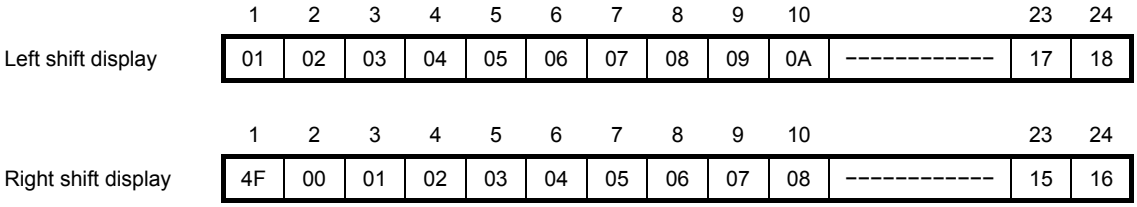
When a Display Shift operation is executed, the relation between the DD RAM address and the display position is as shown below.



b) When the T7934 is used with one T6A92, the first 24 characters are displayed as shown below.



When a Display Shift operation is executed, the relation between the DD RAM address and the display position is as shown below.



c) Each extra T6A92 allows 16 more characters to be displayed. A maximum of five T6A92s can be used, allowing display of up to 80 characters.

(2) The relation between the DD RAM address and the display position in 2−Line Display mode (N = 1)

	1	2	3	4		39	40	← Display position
1st line	00	01	02	03	----------	26	27	← DD RAM address
2nd line	40	41	42	43	----------	66	67	

Note: The DD RAM address of the 2nd line is not the next address after the last address of the 1st line.

a) Using one T7934, the first 16 characters (8 characters × 2 lines) are displayed as shown below.

	1	2	3	4	5	6	7	8
1st line	00	01	02	03	04	05	06	07
2nd line	40	41	42	43	44	45	46	47

When a Display Shift operation is executed, the relation between the DD RAM address and the display position is as shown below.

	1	2	3	4	5	6	7	8
Left shift display	01	02	03	04	05	06	07	08
	41	42	43	44	45	46	47	48

	1	2	3	4	5	6	7	8
Right shift display	27	00	01	02	03	04	05	06
	67	40	41	42	43	44	45	46

b) Using one T7934 with one T6A92, the first 48 characters (24 characters × 2 lines) are displayed as shown below.

	1	2	3	4	5	6	7	8	9	10		23	24
1st line	00	01	02	03	04	05	06	07	08	09	----------	16	17
2nd line	40	41	42	43	44	45	46	47	48	49	----------	56	57

T7934 Display → | T6A92 Display →

When a Display Shift operation is executed, the relation between the DD RAM address and the display position is as shown below.

	1	2	3	4	5	6	7	8	9	10		23	24
Left shift display	01	02	03	04	05	06	07	08	09	0A	----------	17	18
	41	42	43	44	45	46	47	48	49	4A	----------	57	58

	1	2	3	4	5	6	7	8	9	10		23	24
Right shift display	27	00	01	02	03	04	05	06	07	08	----------	15	16
	67	40	41	42	43	44	45	46	47	48	----------	55	56

c) Each extra T6A92 allows 16 more character to be displayed. Two T6A92s can be used, allowing display of up to 40 characters × 2 lines.

	1	2	3	4	5	6	7	8	9	10		23	24	25	26		39	40
1st line	00	01	02	03	04	05	06	07	08	09	−−−−−−−−	16	17	18	19	−−−−−−−−−	26	27
2nd line	40	41	42	43	44	45	46	47	48	49	−−−−−−−−	56	57	58	59	−−−−−−−−−	66	67

T7934 Display → | T6A92 (1) Display → | T6A92 (2) Display →

- **Character generator ROM (CG ROM)**

The character generator ROM generates 5 × 10−dot character patterns (for 240 different characters) according to the 8−bit character codes in the DD RAM. In the 5 × 7 Dots + Cursor Display mode, the character font uses the upper 5 × 7 dots. The relation between character codes and character patterns is as shown overleaf.

The Relation Between Character Codes and Character Pattern
(CG ROM TYPE 0000 / 0100 / 0200 / 0300)

HIGHER 4 BITS / LOWER 4 BITS	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
XXXX0000	CGRAM (0)															
XXXX0001	(1)															
XXXX0010	(2)															
XXXX0011	(3)															
XXXX0100	(4)															
XXXX0101	(5)															
XXXX0110	(6)															
XXXX0111	(7)															
XXXX1000	(0)															
XXXX1001	(1)															
XXXX1010	(2)															
XXXX1011	(3)															
XXXX1100	(4)															
XXXX1101	(5)															
XXXX1110	(6)															
XXXX1111	(7)															

- **Character generator RAM (CG RAM)**

The T7934 can display user−defined original character using the character generator RAM.
(5 × 7 dots: 8−type, 5 × 10 dots: 4−type)
The relation between the character codes, the CG RAM address and character patterns is as shown below.

(1) For 5 × 7−dot character patterns

CHARACTER CODES (DD RAM DATA)									CG RAM ADDRESS						CHARACTER PATTERNS (CG RAM DATA)								
7	6	5	4	3	2	1	0		5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	0	0	0	*	0	0	0		0	0	0	0	0	0	*	*	*	1	1	1	1	0
												0	0	1				1	0	0	0	1
												0	1	0				1	0	0	0	1
												0	1	1				1	1	1	1	0
												1	0	0				1	0	0	0	1
												1	0	1				1	0	0	0	1
												1	1	0				1	1	1	1	0
												1	1	1	*	*	*	0	0	0	0	0
0	0	0	0	*	0	0	1		0	0	1	0	0	0	*	*	*	0	1	1	1	1
												0	0	1				1	0	0	0	0
												0	1	0				1	0	0	0	0
												0	1	1				0	1	1	1	0
												1	0	0				0	0	0	0	1
												1	0	1				0	0	0	0	1
												1	1	0				1	1	1	1	0
												1	1	1	*	*	*	0	0	0	0	0
												0	0	0	*	*	*	1	1	1	1	1
												0	0	1				0	0	1	0	0
0	0	0	0	*	1	1	1		1	1	1	0	1	1				0	0	1	0	0
												1	0	0				0	0	1	0	0
												1	0	1				0	0	1	0	0
												1	1	0				0	0	1	0	0
												1	1	1	*	*	*	0	0	0	0	0

Character Pattern Example (1)

← Cursor Position

Character Pattern Example (2)

← Cursor Position

* : Invalid

Note 1: Character code bit 0 to bit 2 correspond to CG RAM address bit 3 to bit 5.
Note 2: Bit 0 to bit 2 of the CG RAM address indicate the row within the character bit map. The 8th row (the bottom row) corresponds to the cursor position on the LCD display. Normally the 8th row should be blank (all 0s), otherwise the lowest line of the character will be obscured when used with the cursor.
Note 3: Character pattern line positions correspond to CG RAM data bit 0 to bit 4. CG RAM data bit 5 to bit 7 is not used for display; the data can be used for general RAM data.
Note 4: If bit 4 to bit 7 are all 0, a CG RAM character is indicated. The value of bit 3 does not matter. Character codes 00H and 08H select the same character.
Note 5: 1: ON, 0: OFF

(2) For 5 × 10−dot character patterns

CHARACTER CODES (DD RAM DATA) 7 6 5 4 3 2 1 0		CG RAM ADDRESS 5 4 3 2 1 0	CHARACTER PATTERNS (CG RAM DATA) 7 6 5 4 3 2 1 0	
0 0 0 0 * 0 0 *		0 0 0 0 0	* * * 0 0 0 1 0	Character Pattern Example
		0 0 0 1	* * * 0 0 0 0 0	
		0 0 1 0	* * * 0 0 1 1 0	
		0 0 1 1	* * * 0 0 0 1 0	
		0 1 0 0	* * * 0 0 0 1 0	
		0 1 0 1	* * * 0 0 0 1 0	
		0 1 1 0	* * * 0 0 0 1 0	
		0 1 1 1	* * * 0 0 0 1 0	
		1 0 0 0	* * * 1 0 0 1 0	
		1 0 0 1	* * * 0 1 1 0 0	
		1 0 1 0	* * * 0 0 0 0 0	← Cursor Position
		1 0 1 1	* * * * * * * *	
		1 1 0 0	* * *	
		1 1 0 1	* * *	
		1 1 1 0	* * *	
		1 1 1 1	* * * * * * * *	
		0 0 0 0	* * *	
		0 0 0 1	* * *	
		0 0 1 0	* * *	
0 0 0 0 * 1 1 *		1 1 0 0 0		
		1 1 0 0 1		
		1 1 0 1 0	* * *	
		1 1 0 1 1	* * * * * * * *	
		1 1 1 0 0	* * *	
		1 1 1 0 1	* * *	
		1 1 1 1 0	* * *	
		1 1 1 1 1	* * * * * * * *	* : Invalid

Note 1: Character code bit 1 and bit 2 correspond to CG RAM address bit 4 and bit 5.

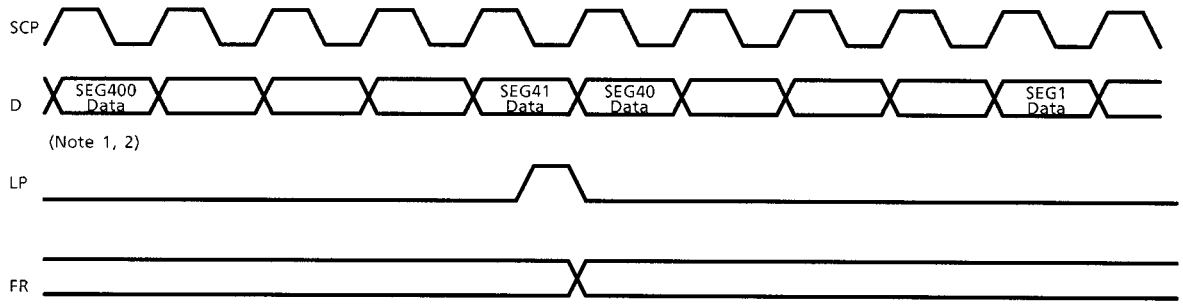
Note 2: Bit 0 to bit 3 of the CG RAM address indicate the row within the character bit map. The 1 1th row corresponds to the cursor position on the LCD display. Normally the 11th row should be blank (all 0s), otherwise the lowest line of the character will be obscured when used with the cursor. Lines 12 to 16 are not used for display data and can be used for general RAM data.

Note 3: If bit 4 to bit 7 are all 0, a CG RAM character is indicated. The values of bits 0 and 3 do not matter. Character codes 00 H, 01 H, 08 H and 09 H all select the same character.

Note 4: 1: ON, 0: OFF

● Timing generation circuit

The timing generation circuit generates timing signals for operating internal circuits such as the DD RAM, CG ROM and CG RAM.
The circuit is designed so that access by the MPU does not disturb the display. When data is written to the DD RAM, only the portion of RAM being written to is affected.
This circuit also generates timing signals which operate the extension driver (e.g. the T6A92).
The relation between the timing signals in 1−Line Display mode is as shown below.



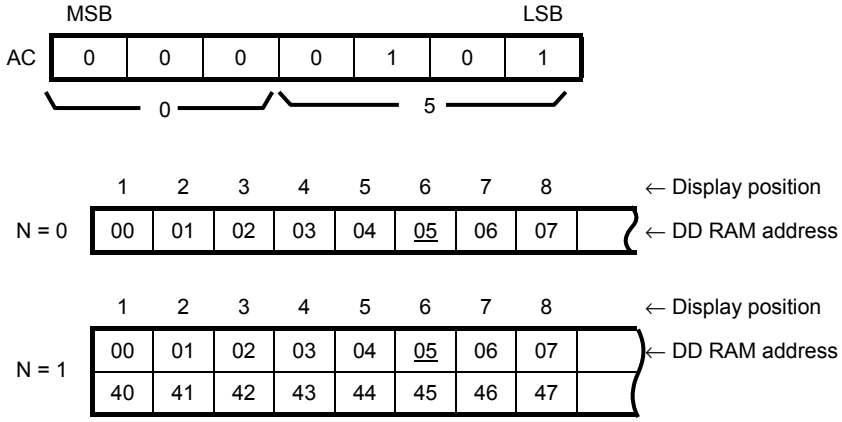
Note 1: SEG400 to SEG41 Data for the extension driver
SEG40 to SEG1 Data for the T7934
Note 2: In 2−Line Display mode, “SEG400 Data” changes to “SEG200 Data”

● LCD drive circuit

The LCD drive circuit consists of 16 row drivers and 40 column drivers. When the character font type and the number of lines have been selected by the appropriate command, the valid row drivers automatically output drive waveforms, and the other row drivers output OFF waveforms.
The T7934 0000 to 0300 all have the same type of column driver.

● Cursor / blink display control circuit

This circuit generates the cursor or blink display. The cursor or blink is displayed in the digit which corresponds to the DD RAM address set in the Address Counter.
When the Address Counter is 05H, the cursor is displayed as shown below.



Note: The cursor or blink is also displayed when the CG RAM address is set in the Address Counter. In this case, the cursor or blink is displayed regardless of the DD RAM address.

● Internal reset circuit

When the power is on, the T7934 is automatically initialized by the internal reset circuit. The Busy flag (BF) remains at 1 (Busy state) until initialization ends. The following instructions are executed during initialization.

(1) Display Clear
(2) Set Function ····· DL = 1 : 8−bit data interface
N = 0 : 1−line display
F = 0 : 5 × 7−dot character font
(3) Set Entry Mode ····· I / D = 1 : +1
S = 0 : No shift
(4) Display ON / OFF Control ··· D = 0 : Display OFF
C = 0 : Cursor OFF
B = 0 : Blink OFF

Note: The MPU should execute commands (1) to (4), because the internal reset circuit may not move normally according to the power supply condition.

- **Interfacing to the MPU**

  The T7934 has two methods of interfacing to the MPU. One is the 8−bit data interface and the other is the 4−bit data interface.

  (1) When using the 4−bit interface, the T7934 uses DB4 to DB7 as the interface, and does not use DB0 to DB3. The data from the MPU to the T7934 is sent as 2 sets of 4 bits. First the higher 4 bits are sent to the T7934, then the lower 4 bits are sent.
  The Busy flag and Address Counter data is also sent in 2 parts.

  (2) When the 8−bit interface is used, the T7934 uses DB0 to DB7 as the interface.

Instruction

The MPU can directly control two registers. One is the Instruction register (IR) and the other is the Data register (DR).
While the T7934 is executing an instruction, it cannot execute any other instructions (except for the Read Busy flag and Address instruction). The Busy flag is maintained at 1 (Busy state) until the instruction completes. Before the instruction is sent from the MPU to the T7934, the MPU must check that the busy flag is set to 0 (Not Busy state). If the instruction is sent to the T7934 without a Busy check, the MPU must wait the execution time of the instruction before sending the next instruction to the T7934.

Instruction	Code										Description	Execution Time (Max) (f_{osc} = 250 kHz)
	R_S	R / W ($\overline{WR}$)	D7	D6	D5	D4	D3	D2	D1	D0		
Test	0	0	0	0	0	0	0	0	0	0	Do not use.	0 μs
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears the display and sets DD RAM address 0 in Address Counter	1.64 ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in Address Counter and returns display to home position. The contents of the DD RAM do not change.	1.64 ms
Set Entry Mode	0	0	0	0	0	0	0	1	I / D	S	Sets cursor shift direction and display shift. These operations are executed when data is written.	40 μs
Display ON / OFF Control	0	0	0	0	0	0	1	D	C	B	Sets ON / OFF for all displays (D), cursor ON / OFF (C), cursor position blink (B).	40 μs

Instruction	Code										Description	Execution Time (Max) (f_{osc} = 250 kHz)
	R_S	R / W (WR)	D7	D6	D5	D4	D3	D2	D1	D0		
Cursor / Display Shift	0	0	0	0	0	1	S / C	R / L	*	*	Shifts cursor and display without changing DD RAM contents	40 µs
Set Function	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (N), and character font (F)	40 µs
Set CG RAM Address	0	0	0	1	CG RAM Address						Sets CG RAM Address	40 µs
Set DD RAM Address	0	0	1	DD RAM Address							Sets DD RAM Address	40 µs
Read Busy Flag and Address	0	1	BF	Address Counter							Reads Busy Flag (BF), and Address Counter contents	0 µs
Write Data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM	46 µs
Read Data from CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM	46 µs
—	I / D = 1 : Increment I / D = 0 : Decrement S = 1 : Display Shift On S / C = 1 : Display Shift S / C = 0 : Cursor Shift R / L = 1 : Shift to the Right R / L = 0 : Shift to the Left DL = 1 : 8 bits DL = 0 : 4 bits N = 1 : 2 lines N = 0 : 1 line F = 1 : 5×10 dots F = 0 : 5×7 dots BF = 1 : Busy State BF = 0 : Can Accept Instruction										—	—

*: Invalid

- **Clear Display**

	RS	R / W ($\overline{WR}$)	DB7	----------					DB0
Instruction Code	0	0	0	0	0	0	0	0	1

When the T7934 executes this instruction, code 20 H (code 20 H must be the “Space code”) is written to every address in the DD RAM. This command resets the DD RAM address in the Address Counter.
The display is inhibited and the cursor or blink is moved to the left of the display. (In 2−Line Display mode, the cursor moves to the left of 1st line of the display.) The I / D of Entry mode is set to 0. The S of Entry mode does not change.

- **Return Home**

	RS	R / W ($\overline{WR}$)	DB7	----------					DB0	
Instruction Code	0	0	0	0	0	0	0	0	1	*	*: invalid

The DD RAM address in the Address Counter is reset by this instruction, and the display shift is cancelled (this is known as returning to the home position). The contents of the DD RAM do not change. The cursor or blink moves to the extreme left of the display. (In 2−Line Display mode, the cursor moves to the extreme left of the 1st line of the display.)

- **Set Entry Mode**

	RS	R / W ($\overline{WR}$)	DB7	----------					DB0
Instruction Code	0	0	0	0	0	0	0	1	I / D	S

I / D : The Address Counter is incremented (I / D = 1) or decremented (I / D = 0) after the data has been written to or read from DD RAM.
The same is true when date is written to or read from CG RAM.

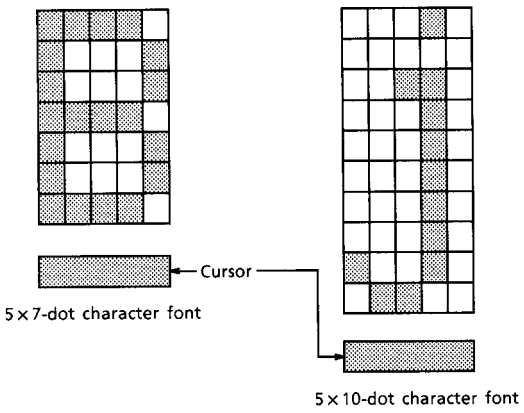
S : If S = 1, the entire display is shifted left (I / D = 1) or right (I / D = 0) when data is written to the DD RAM. (The cursor position does not move)
If S = 0, the display is not shifted.

- **Display ON / OFF Control**

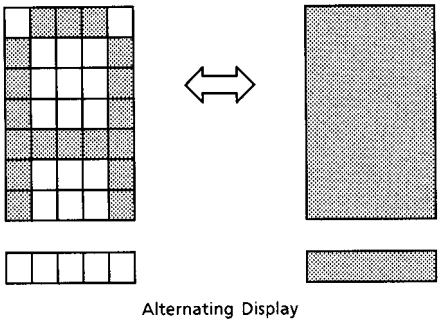
	R / W									
	RS	($\overline{WR}$)	DB7	----------						DB0
Instruction Code	0	0	0	0	0	0	1	D	C	B

D: D = 1, display is ON; D = 0, display is OFF.
When D is reset, the contents of the DD RAM do not change. Therefore, the contents can be displayed as before by setting D.
C: C = 1, cursor display is ON; C = 0, cursor display is OFF.
5 × 7−dot character font: cursor display uses 5 dots on the 8th line
5 × 10−dot character font: cursor display uses 5 dots on the 11th line
B: B = 1, character blink is ON (same position of cursor position); B = 0, character blink is OFF.
Cursor and blink can operate at same time.
Blink period: Font 5 × 7−dot, f_{osc} = 250 kHz
(1 / 250 k) × 5 × 80 × 8 × 32 = 409.6 (ms)

Font 5 × 10−dot, fosc = 250 kHz
(1 / 250 k) × 5 × 80 × 11 × 32 = 563.2 (ms)



(1) Cursor display example



(2) Blink display example

- **Cursor Display Shift**

	RS	R / W ($\overline{WR}$)	DB7							DB0	
Instruction Code	0	0	0	0	0	1	S / C	R / L	*	*	*: invalid

When this instruction is executed, the cursor or display is shifted to the right or left without display data being written or read.
In 2−Line Display mode, the cursor is shifted from the 40th digit of the 1st line to the 1st digit of the 2nd line.

S / C	R / L	Functions	Address Counter (AC)
0	0	Shift the cursor to the left.	AC = AC − 1
0	1	Shift the cursor to the right.	AC = AC + 1
1	0	Shift the whole display to the left. The cursor follows the display shift direction.	AC = AC
1	1	Shift the whole display to the right. The cursor follows the display shift direction.	AC = AC

When S / C = 1, the contents of the Address Counter do not change.

- **Set Function**

	RS	R / W ($\overline{WR}$)	DB7							DB0
Instruction Code	0	0	0	0	1	DL	N	F	*	*

DL: DL = 1, 8−bit data interface (DB0 to DB7)
DL = 0, 4−bit data interface (DB4 to DB7)
N : N = 0, 1−Line Display mode
N = 1, 2−Line Display mode
F : F = 0, 5 × 7−dot character font
F = 1, 5 × 10−dot character font

Note: Execute this instruction first in a program before executing any other instructions (except for the Busy Flag / Address Read instruction).
After this instruction has been used once, it cannot be used again, except to change the DL bit setting.

N	F	No. of Display Lines	Character Font	Duty	Note
0	0	1	5 × 7 dots	1 / 8	—
0	1	1	5 × 10 dots	1 / 11	—
1	*	2	5 × 7 dots	1 / 16	When N = 1, the 5 × 10 dots character font cannot be selected.

- **Set CG RAM Address**

	R / W									
	RS	($\overline{WR}$)	DB7	----------						DB0
Instruction Code	0	0	0	1	A	A	A	A	A	A
					MSB					LSB

This instruction writes CG RAM address data (e.g. AAAAAA (bin)) into Address Counter. The MPU can now read or write CG RAM data.

- **Set DD RAM Address**

	R / W									
	RS	($\overline{WR}$)	DB7	----------						DB0
Instruction Code	0	0	1	A	A	A	A	A	A	A
				MSB						LSB

This instruction writes DD RAM address data (e.g. AAAAAAA (bin)) into Address Counter. The MPU can now read or write DD RAM data.

- **Read Busy Flag and Address**

	R / W									
	RS	($\overline{WR}$)	DB7	----------						DB0
Instruction Code	0	1	BF	A	A	A	A	A	A	A
				MSB						LSB

This instruction makes the T7934 output the Busy flag and the contents of the Address Counter.
The Busy flag indicates whether the T7934 can receive an instruction or not. A Busy check must done before the next instruction is sent to the T7934.
The Address Counter indicates the CG or DD RAM address.
The preceding two instructions (Set CG RAM Address and Set DD RAM Address) determine whether the Address Counter is used to hold a CG RAM address or a DD RAM address.

- **Write Data to CG or DD RAM**

	R / W									
	RS	($\overline{WR}$)	DB7	----------						DB0
Instruction Code	1	0	D	D	D	D	D	D	D	D
			MSB							LSB

This instruction writes 8−bit data (e.g. DDDDDDDD (bin)) to CG RAM or DD RAM. The previous instruction (Set CG RAM Address or Set DD RAM Address) determines whether the data will be written to CG RAM or DD RAM. Before this instruction is executed, the Set CG RAM or DD RAM Address instruction must be executed.
After the data has been written, the address is automatically incremented by 1 or decremented by 1 according to the entry mode. The display mode is also determined by the entry mode.

- **Read Data from CG or DD RAM**

	R / W									
	RS	($\overline{WR}$)	DB7	----------						DB0
Instruction Code	1	1	D	D	D	D	D	D	D	D
			MSB							LSB

This instruction reads 8−bit data (e.g. DDDDDDDD (bin)) from CG RAM or DD RAM. The previous instruction (Set CG RAM Address or Set DD RAM Address) determines whether the data will be read from CG RAM or DD RAM. Before this instruction is executed, the Set CG RAM or DD RAM Address instruction must be executed. If neither of these instructions is executed, the first data read will not yield valid data.

A Read Data from CG or DD RAM instruction just after a Write Data to CG or DD RAM instruction cannot read the RAM data pointed to by Address Counter.

To read the RAM data indicated by Address Counter, perform one of the following operations:

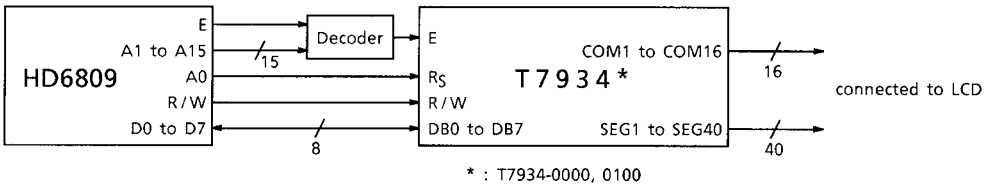
(1) Use Set CG RAM Address or Set DD RAM Address command.
(2) (For DD RAM only) perform a cursor shift. (Note)
(3) Read RAM data once (to read invalid data) then read RAM data again.

Note: A Cursor Shift instruction does the function which is the same as Set DD RAM Address instruction.

After the data has been read, the RAM address is automatically incremented by 1 or decremented by 1 according to the entry mode.

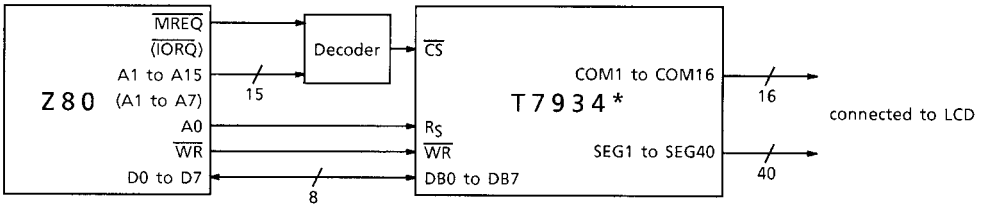
How to Use The T7934

- **Interface to 68−Series MPU**



* : T7934-0000, 0100

- **Interface to 80−Series MPU**



* : T7934-0200, 0300

Note: Z80 is a trademark of ZILOG Inc.

- **Interface to LCD**

The T7934 can display a 5 × 7−dot or 5 × 10−dot character font plus a cursor, and can display up to two lines with 5 × 7−dot characters.
The relationship between the character font and the number of lines is as shown below.

Number Of Lines	Character Font	Duty
1	5 × 7 dots + Cursor	1 / 8
1	5 × 10 dots + Cursor	1 / 11
2	5 × 7 dots + Cursor	1 / 16

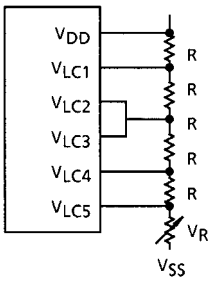
Power Supply for LCD Drive

- **For the T7934−0100 or T7934−0300**

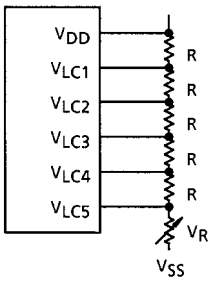
Various voltage levels must be applied to the T7934's V_{LC1} to V_{LC5} pins to obtain the LCD drive waveforms.
The voltage levels vary according to the duty factor. The following table shows the relation.

Power Supply \ Duty Factor / Bias	1 / 8, 1 / 11 $\frac{1}{4}$	1 / 16 $\frac{1}{5}$
V_{LC1}	$V_{DD} - 1 / 4\ V_{LCD}$	$V_{DD} - 1 / 5\ V_{LCD}$
V_{LC2}	$V_{DD} - 1 / 2\ V_{LCD}$	$V_{DD} - 2 / 5\ V_{LCD}$
V_{LC3}	$V_{DD} - 1 / 2\ V_{LCD}$	$V_{DD} - 3 / 5\ V_{LCD}$
V_{LC4}	$V_{DD} - 3 / 4\ V_{LCD}$	$V_{DD} - 4 / 5\ V_{LCD}$
V_{LC5}	$V_{DD} - V_{LCD}$	$V_{DD} - V_{LCD}$

$V_{LCD} = V_{DD} - V_{LC5}$



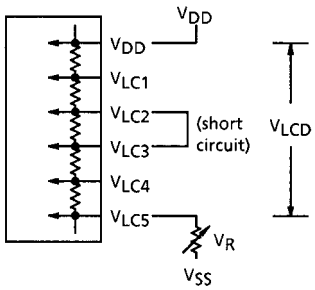
(1) 1 / 4 Bias



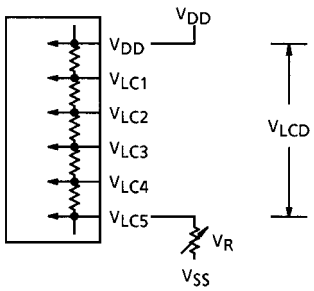
(2) 1 / 5 Bias

- **For the T7934−0000, 0200**

The T7934−0000, 0200 has an internal resistance ladder as shown below.



(1) 1 / 4 Bias

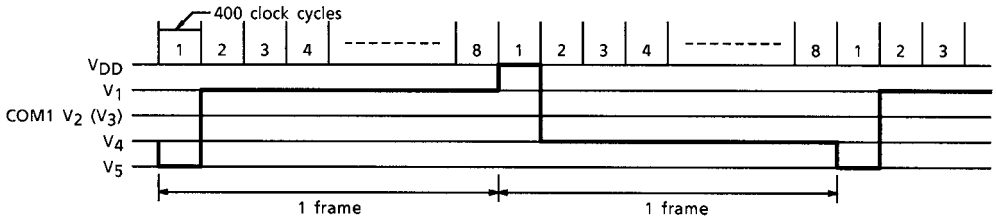


(2) 1 / 5 Bias

The Relation Between Oscillation Frequency and LCD Frame Frequency

LCD frame frequency example (f_{osc} = 250 kHz)

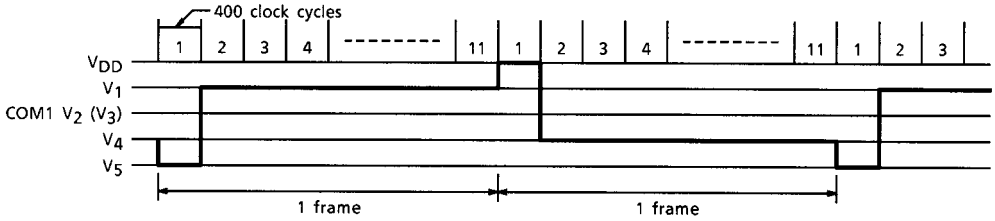
- **1 / 8 duty**



1 frame = 4 μs × 400 × 8 = 12800 μs = 12.8 ms

Frame frequency = $\frac{1}{12.8\ \text{ms}}$ = 78.1 Hz

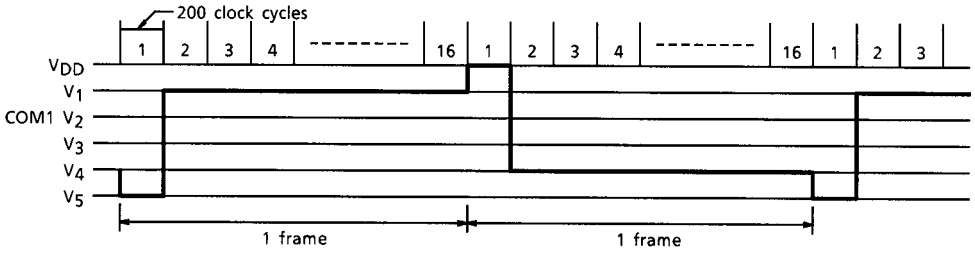
- **1 / 11 duty**



1 frame = 4 μs × 400 × 11 = 17600 μs = 17.6 ms

Frame frequency = $\frac{1}{17.6\ \text{ms}}$ = 56.8 Hz

- **1 / 16 duty**



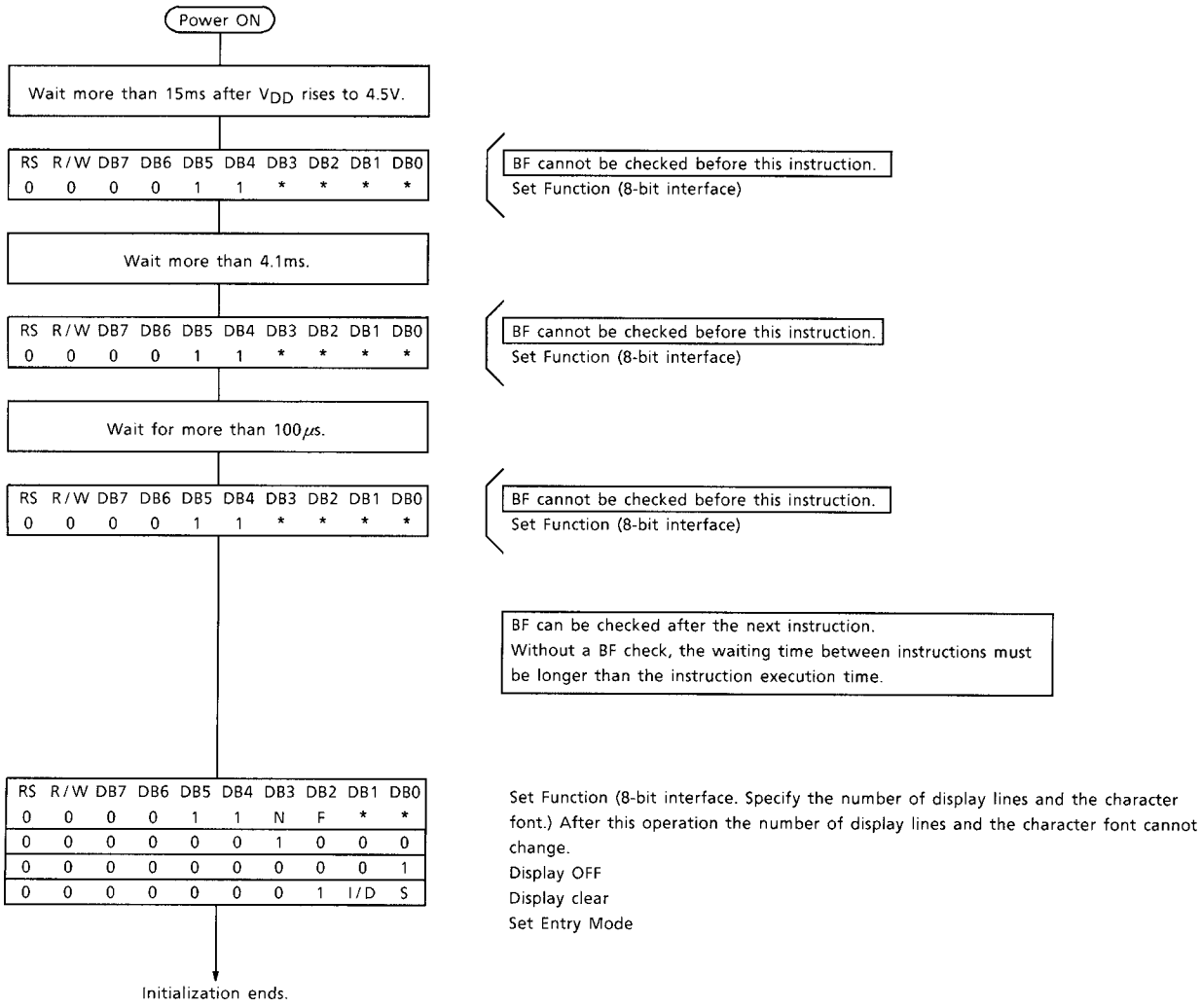
1 frame = 4 μs × 200 × 16 = 12800 μs = 12.8 ms

Frame frequency = $\frac{1}{12.8\ \text{ms}}$ = 78.1 Hz

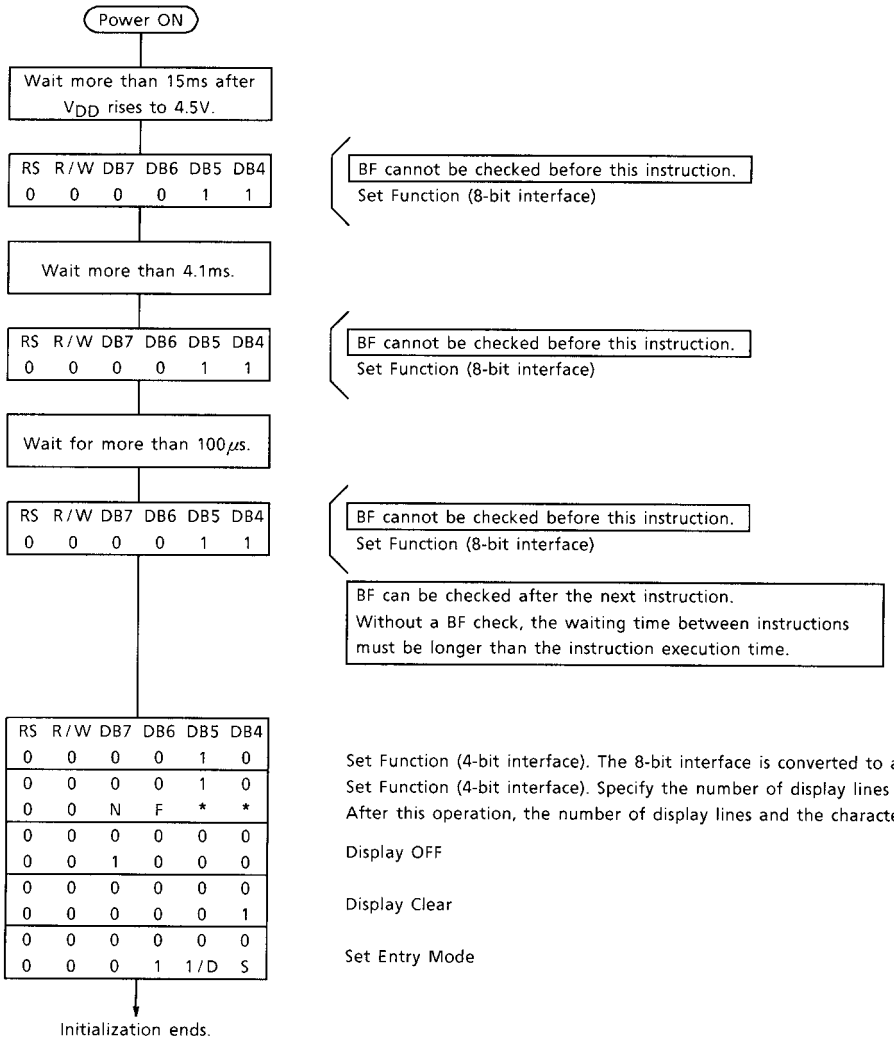
Initialization by Instruction (soft reset)

If the internal reset circuit does not operate correctly, initialization by instruction is required. Use the following initialization sequence.

- **8−bit data interface**



- **4−bit data interface**



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Power Supply Voltage	V_{DD}	−0.3 to 7.0	V
Input Voltage	V_{IN}	−0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opr}	−20 to 75	°C
Storage Temperature	T_{stg}	−55 to 125	°C

Note 1: All voltage values are referenced to V_{SS} = 0 V.

Note 2: Ensure that the following condition is always maintained.

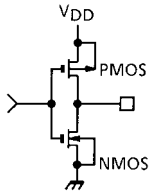
$V_{DD} \geq V_{LC1} \geq V_{LC2} \geq V_{LC3} \geq V_{LC4} \geq V_{LC5} \geq V_{SS}$

Electrical Characteristics
DC Characteristics
Test Conditions
(Unless otherwise noted, V_{DD} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = −20 to 75°C)

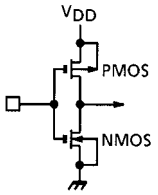
Item		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Pin Name
Operating Voltage (1)		V_{DD}	—	—	4.5	—	5.5	V	—
Operating Voltage (2)		V_{LCD}	—	$V_{LCD} = V_{DD} - V_{LC5}$	3.0	—	V_{DD}	V	—
Input Voltage (1)	H Level	V_{IH1}	—	—	V_{DD} − 1.0	—	V_{DD}	V	OSC1
	L Level	V_{IL1}	—	—	0	—	1.0	V	
Input Voltage (2)	H Level	V_{IH2}	—	—	2.0	—	—	V	R / W, R_S, E DB0 to DB7
	L Level	V_{IL2}	—	—	—	—	0.8	V	
Output Voltage (1)	H Level	V_{OH1}	—	I_{OH} = −0.625 mA	V_{DD} − 0.3	—	—	V	D, SCP LP, FR OSC2
	L Level	V_{OL1}	—	I_{OL} = 0.625 mA	—	—	0.3	V	
Output Voltage (2)	H Level	V_{OH2}	—	I_{OH} = −1.2 mA	2.4	—	—	V	DB0 to DB7
	L Level	V_{OL2}	—	I_{OL} = 2.0 mA	—	—	0.4	V	
Row Output Resistance		RCOM	—	I_d = ±50 μA	—	—	20	kΩ	COM1 to 16
Column Output Resistance		RSEG	—	I_d = ±50 μA	—	—	30	kΩ	SEG1 to 40
Input Leakage Current		I_{IL}	—	V_{IN} = 0 to V_{DD} (Note 2)	—	—	1	μA	R / W, R_S, E DB0 to DB7
Pull−up MOS Current		$-I_P$	—	V_{DD} = 5 V	50	125	250	μA	R / W, R_S DB0 to DB7
Power Supply Current (1)		I_{DD1}	—	(Note 3)	—	—	800	μA	V_{DD}
Power Supply Current (2)		I_{DD2}	—	(Note 4)	—	—	600	μA	V_{DD}
Clock Oscillation Frequency		f_{osc}	—	(Note 5)	190	270	350	kHz	OSC1, OSC2
External Clock Frequency		f_{IN}	—	(Note 6)	125	250	350	kHz	OSC1
External Clock Duty		f_{Duty}	—	(Note 7)	45	50	55	%	OSC1
External Clock Rise Time		t_r	—	(Note 8)	—	—	200	ns	OSC1
External Clock Fall Time		t_f	—	(Note 8)	—	—	200	ns	OSC1
Internal Clock Frequency		f_{osc}	—	(Note 9)	245	250	255	kHz	OSC1, OSC2

Note 1: I / O pin details (except for LCD output)

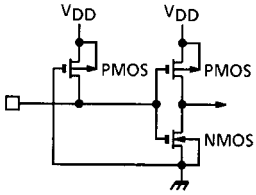
- **Output pin: SCP, LP, FR, D**



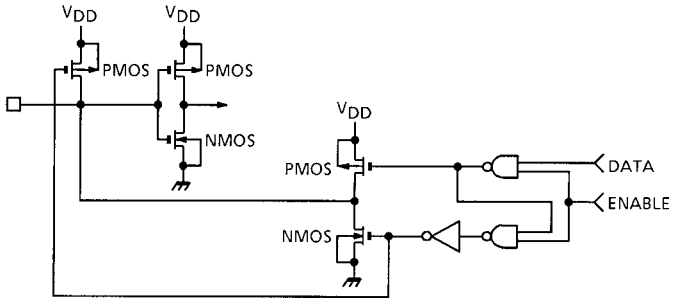
- **Input pin:**
  E (No pull−up MOS)



- **Input pin:**
  RS, R / W (With pull−up MOS)

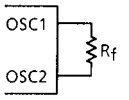


- **I / O pin: DB0 to DB7**



Note 2: This current does not include pull−up MOS current
Note 3: Ceramic oscillation mode ..... V_{DD} = 5.0 V, f_{osc} = 250 kHz
Note 4: R_f oscillation or external clock mode ..... V_{DD} = 5.0 V, $f_{osc} = f_{scp}$ = 270 kHz

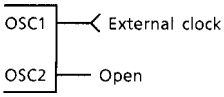
Note 5: External R_f oscillation



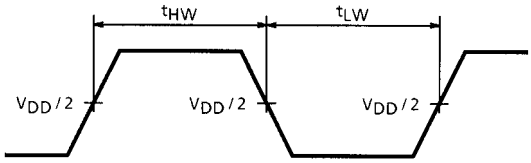
$R_f = 120k\Omega \pm 2\%$

Oscillation frequency depends on OSC1 and OSC2 pin capacitance, therefore wiring must be as short as possible.

Note 6: External clock operation

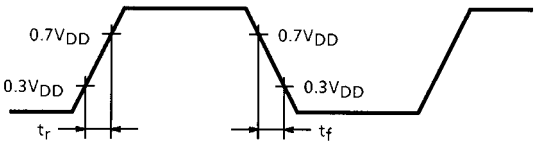


Note 7: External clock waveform1

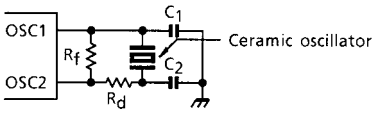


$f_{Duty} = t_{HW} / (t_{HW} + t_{LW}) \times 100\ (\%)$

Note 8: External clock waveform2



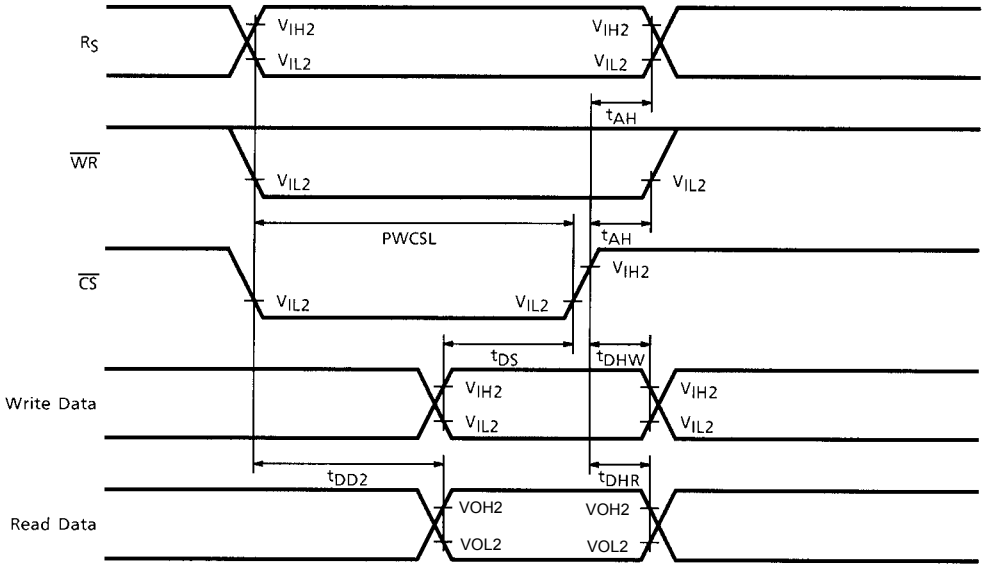
Note 9: External ceramic oscillator



Ceramic oscillator : CSB250D (Murata)
R_f : $1M\Omega \pm 10\%$
R_d : $3.3k\Omega \pm 5\%$
C_1 : $680pF \pm 10\%$
C_2 : $680pF \pm 10\%$

AC Characteristics

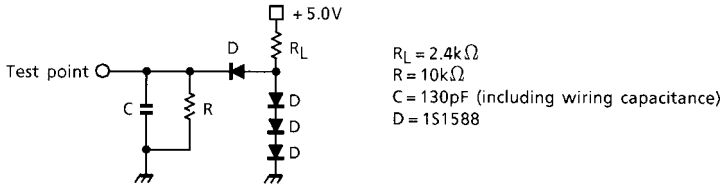
- **80−Series MPU Read / Write operation**



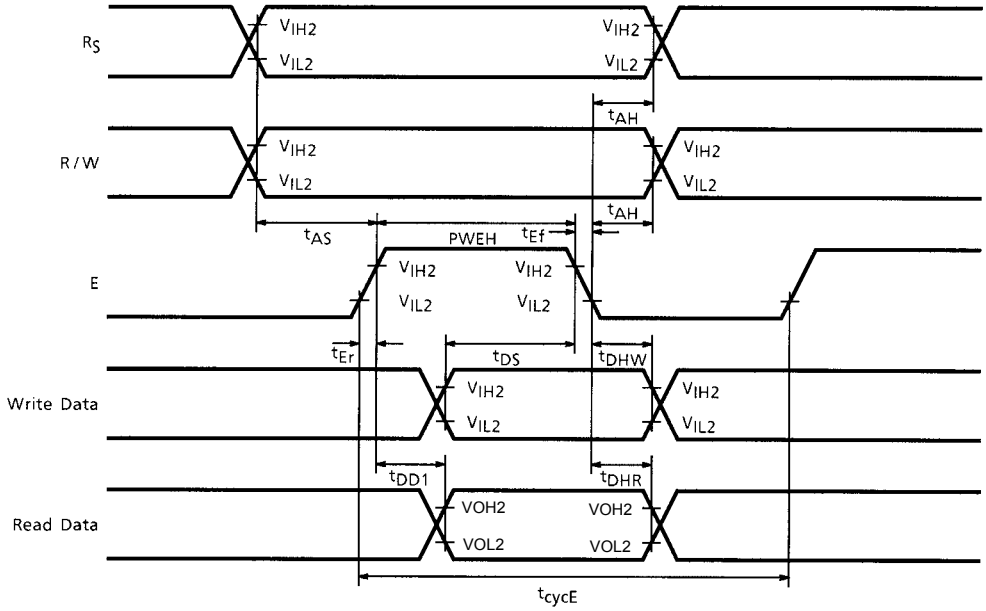
Test Conditions (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, Ta = −20 to 75°C)

Item	Symbol	Min	Max	Unit
Chip Select Pulse Width	PWCSL	260	—	ns
Address Hold Time	t_{AH}	10	—	ns
Data Set−up Time	t_{DS}	60	—	ns
Data Hold Time	t_{DHW}	10	—	ns
Data Delay Time	t_{DD2} (Note)	—	180	ns
Data Hold Time	t_{DHR} (Note)	20	—	ns

Note: With load circuit connected (DB0 to DB7)



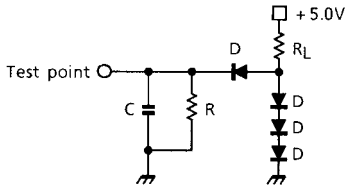
- **68−Series MPU Read / Write operation**



Test Conditions (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, Ta = −20 to 75°C)

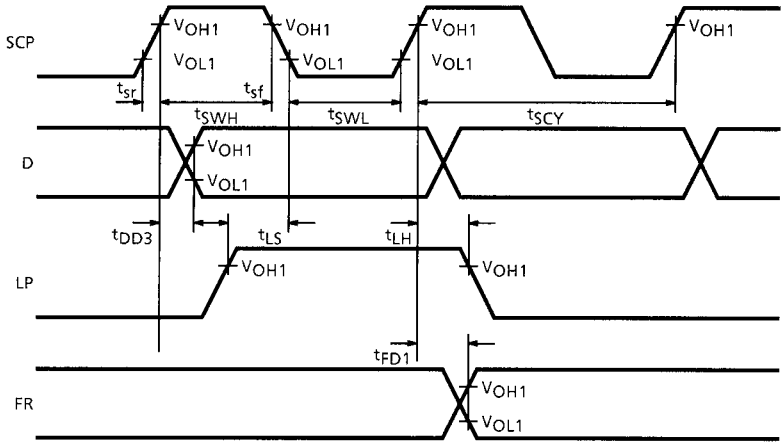
Item	Symbol	Min	Max	Unit
Enable Cycle Time	t_{cycE}	500	—	ns
Enable Pulse Width	PWEH	220	—	ns
Enable Rise / Fall Time	t_{Er}, t_{Ef}	—	20	ns
Address Set−up Time	t_{AS}	40		ns
Address Hold Time	t_{AH}	10	—	ns
Data Set−up Time	t_{DS}	60	—	ns
Data Hold Time	t_{DHW}	10	—	ns
Data Delay Time	t_{DD1} (Note)	—	120	ns
Data Hold Time	t_{DHR} (Note)	20	—	ns

Note: With load circuit connected (DB0 to DB7)



R_L = 2.4kΩ
R = 10kΩ
C = 130pF (including wiring capacitance)
D = 1S1588

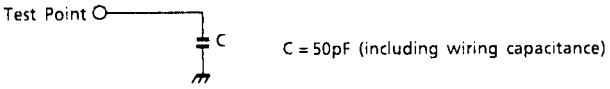
- **Interface timing for extension driver**



Test Conditions (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, Ta = −20 to 75°C)

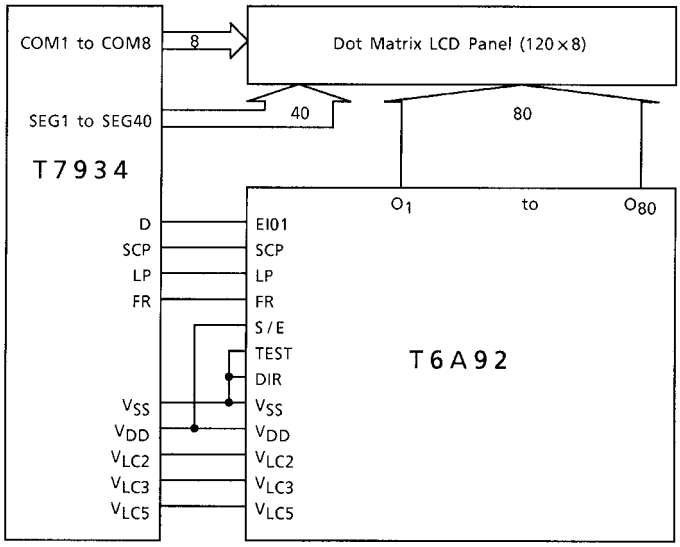
Item	Symbol	Min	Max	Unit
SCP Cycle Time	t_{SCY}	2000	—	ns
SCP Pulse Width	t_{SWH}, L	800	—	ns
SCP Rise / Fall Time	t_{sr}, t_{sf}	—	100	ns
Data Delay Time	t_{DD3} (Note)	—	100	ns
LP Set−up Time	t_{LS}	−120	0	ns
LP Hold Time	t_{LH} (Note)	−100	0	ns
FR Delay Time	t_{FD1} (Note)	−100	100	ns

Note: With load circuit connected

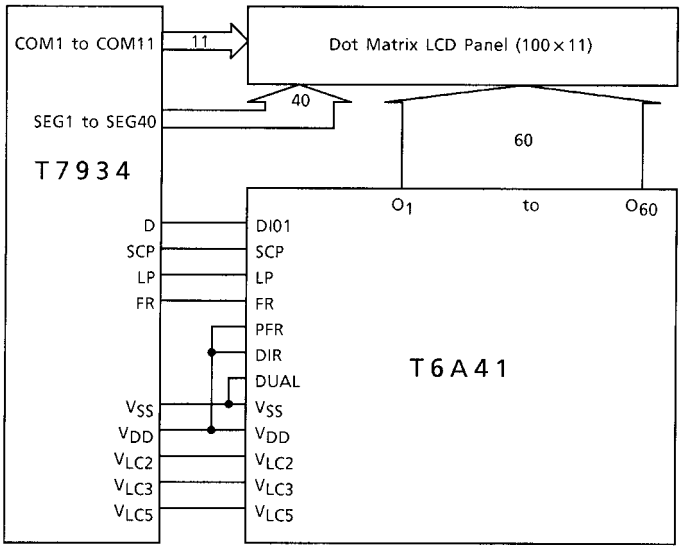


System Application

- **24−character × 1−line display (5 × 7 dots) on the T6A92**

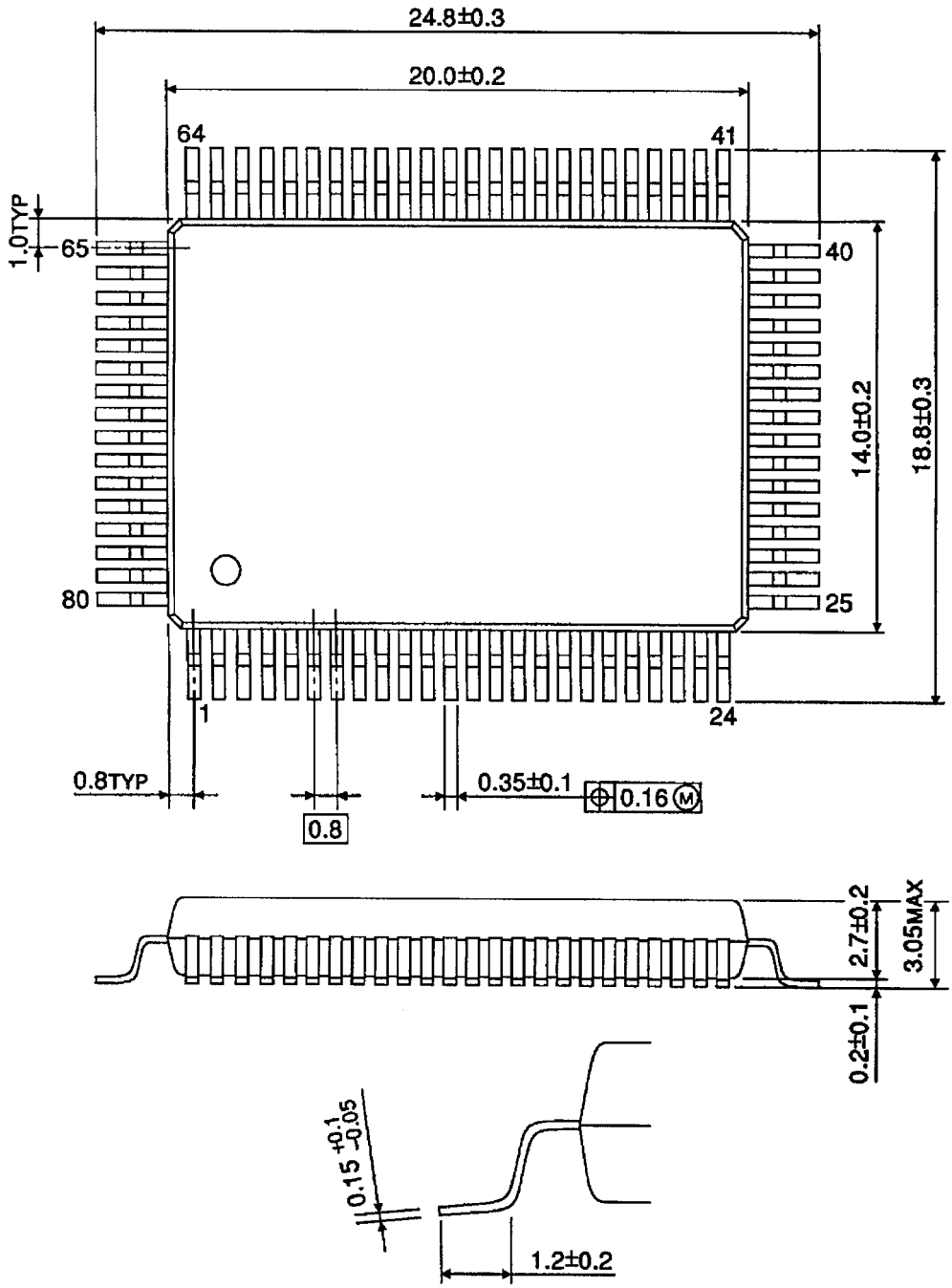


- **24−character × 1−line display (5 × 10 dots) on the T6A41**



Package Dimensions

QFP80-P-1420-0.80A Unit : mm



Weight : 1.5g (Typ.)

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