



## 400mA PCI LDO

### FEATURES

- Glitch-Free Transition Between Input Sources
- Automatic Input Source Selection
- External PMOS Bypass Switch Control
- Built-In 5V Detector
- 1% Regulated Output Voltage Accuracy
- 400mA Load Current Capability
- Kelvin Sense Input
- Low Ground Current, Independent of Load

### APPLICATIONS

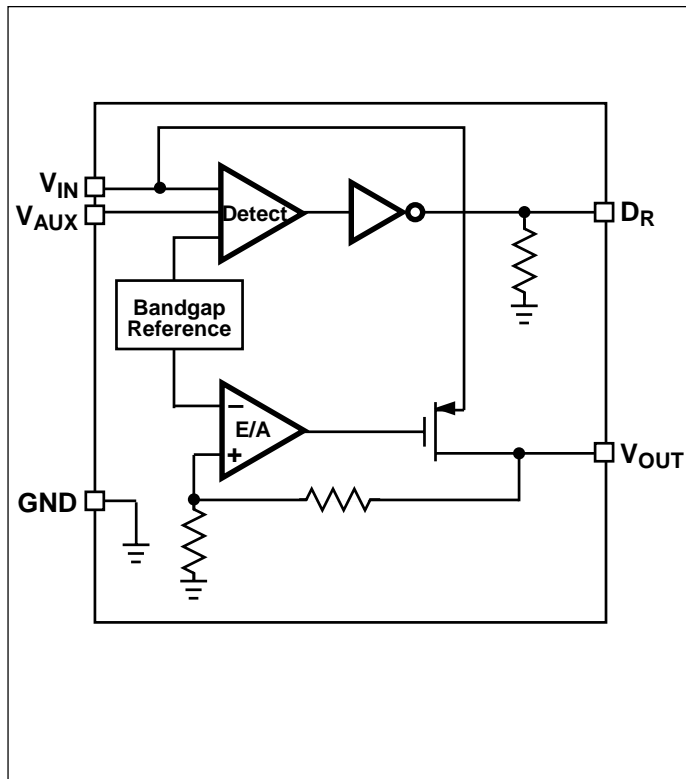
- PCMCIA
- PCI
- Network Interface Cards (NICs)
- Cardbus™ Technology
- Desktop Computers

### GENERAL DESCRIPTION

The TC1267 is an application-specific, low dropout regulator (LDO) specifically intended for use in PCI peripheral card applications complying with PCI Power Management (PCI 2.0). It provides an uninterrupted, 3.3V output voltage when the main (5V) or auxiliary (3.3V) input voltage supplies are present.

The TC1267 consists of an LDO, a voltage threshold detector, external switchover logic and gate drive circuitry. It functions as a conventional LDO as long as the voltage on the main supply input ( $V_{IN}$ ) is above the lower threshold (3.90V typ). Should the voltage on  $V_{IN}$  fall below the lower threshold the LDO is disabled, and an external P-channel MOSFET is automatically turned on, connecting the auxiliary supply input to  $V_{OUT}$ , and ensuring an uninterrupted 3.3V output. The main supply is automatically selected if both the main and auxiliary input supplies are present, and transition from one input supply to the other is guaranteed glitch-free. High integration, automatic secondary supply switchover, Kelvin sensing, and small size make the TC1267 the optimum LDO for PCI 2.0 applications.

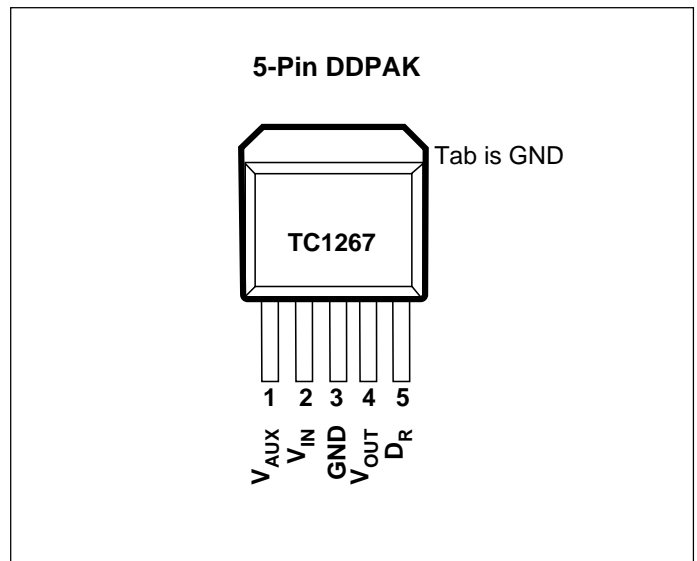
### FUNCTIONAL BLOCK DIAGRAM



### ORDERING INFORMATION

Part No.	Package	Temperature Range
TC1267VET	5-Pin DPAK	-5°C to +95°C

### PIN CONFIGURATION



## TC1267

## ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage ( $V_{IN}$ )	..... -0.5V to + 7V (Max)
Auxiliary Supply Voltage ( $V_{AUX}$ )	..... -0.5V to + 7V (Max)
LDO Output Current ( $I_{OUT}$ )	..... 400mA
Operating Temperature Range ( $T_A$ )	..... -5°C to +70°C
Storage Temperature Range ( $T_{STG}$ )	..... -65°C to +150°C
Lead Temperature (Soldering, 10 Sec)	..... 300 °C
Thermal Impedance Junction-to-Ambient ( $\theta_{JA}$ )	... 27°C/W for DDPAK
ESD Rating	..... 2 KV

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

**ELECTRICAL CHARACTERISTICS:**  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $V_{AUX} = 3.3\text{V}$ ,  $I_{OUT} = 0.1\text{mA}$ ,  $C_{OUT} = 4.7\mu\text{F}$ , unless otherwise specified. Values in **BOLD** apply over full operating temperature range.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{IN}$	Supply Voltage	$V_{AUX} = 0\text{V}$	<b>4.4</b>	<b>5.0</b>	<b>5.5</b>	V
$I_{GND}$	GROUND Current	$V_{AUX} = 0\text{V}$ , (Note 6) $V_{AUX} = 3.3\text{V}$ , (Note 6)	—	230	<b>450</b>	$\mu\text{A}$
$I_{VIN}$	Reverse Leakage from $V_{AUX}$	$V_{AUX} = 3.6\text{V}$ , $V_{IN} = 0\text{V}$ , $I_{OUT} = 0\text{mA}$	—	-0.1	<b>-1.0</b>	$\mu\text{A}$
$V_{AUX}$	Supply Voltage		<b>3.0</b>	<b>3.3</b>	<b>3.6</b>	V
$I_{Q(AUX)}$	Quiescent Current	$V_{IN} = 0\text{V}$ , $I_{OUT} = 0\text{mA}$	—	50	70	$\mu\text{A}$
		$V_{IN} = 5\text{V}$ , $I_{OUT} = 0\text{mA}$	—	60	80	
			—	—	<b>120</b>	
$I_{VAUX}$	Reverse Leakage from $V_{IN}$	$V_{IN} = 5.5\text{V}$ , $V_{AUX} = 0\text{V}$ , $I_{OUT} = 0\text{mA}$	—	-0.1	<b>-1.0</b>	$\mu\text{A}$
$V_{TH(LO)}$	5V Detector Low Threshold Voltage	$V_{IN}$ Falling (Notes 2, 3)	—	3.90	—	V
			<b>3.75</b>	—	<b>4.05</b>	
$V_{HYST}$	5V Detector Hysteresis Voltage	(Notes 2, 3)	—	260	—	mV
			<b>200</b>	—	<b>300</b>	
$V_{TH(HI)}$	5V Detector High Threshold Voltage	$V_{IN}$ Rising (Notes 2, 3)	—	4.15	—	V
			<b>4.0</b>	—	<b>4.30</b>	
$V_{OUT}$	LDO Output Voltage	$I_{OUT} = 20\text{mA}$	—	3.300	—	V
		$4.4\text{V} \leq V_{IN} \leq 5.5\text{V}$ , $0\text{mA} \leq I_O \leq 400\text{mA}$	<b>3.201</b>	—	<b>3.366</b>	
		$3.75\text{V} \leq V_{IN} \leq 4.3\text{V}$ , $0\text{mA} \leq I_{OUT} \leq 400\text{mA}$ (Note 4)	<b>3.000</b>	—	—	
$I_{OUT}$	Output Current		400	—	—	mA
$REG_{(LINE)}$	Line Regulation	$V_{IN} = 4.3\text{V}$ to $5.5\text{V}$	—	0.05	—	%
			<b>-0.5</b>	—	<b>+0.5</b>	
$REG_{(LOAD)}$	Load Regulation	$I_{OUT} = 0.1\text{mA}$ to $400\text{mA}$	—	-0.1	—	%
			<b>-1.5</b>	—	<b>+0.5</b>	

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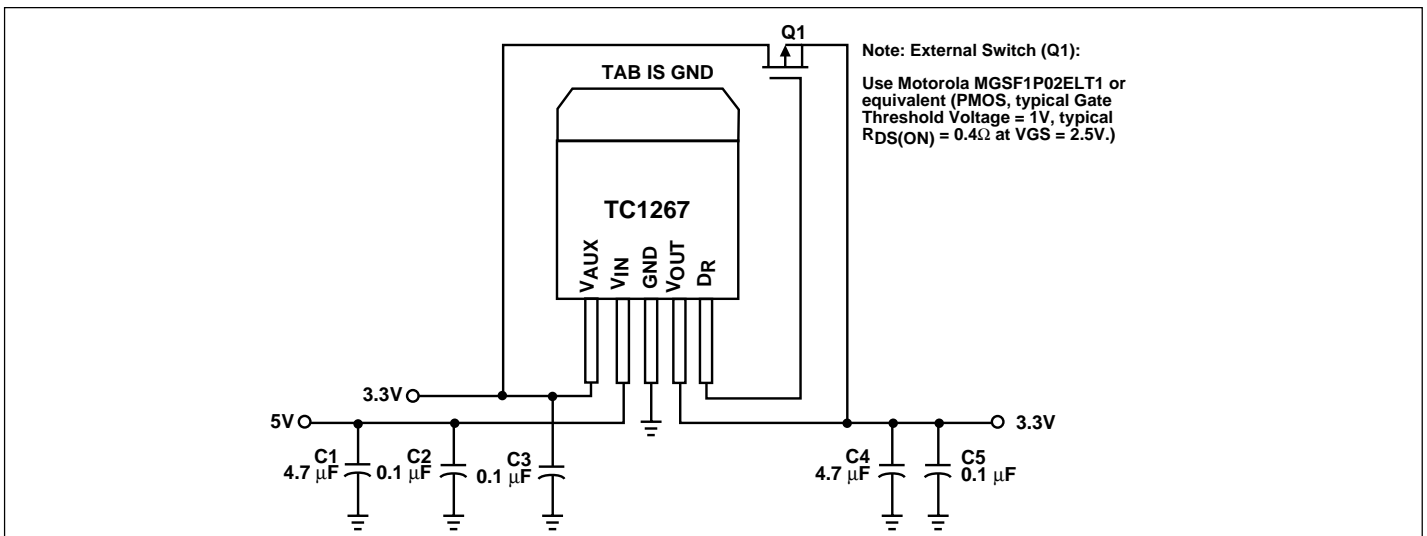
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{DR}$	Drive Voltage	$4.3\text{V} \leq V_{IN} \leq 5.5\text{V}$ , $I_{DR}=200\mu\text{A}$	$V_{IN} - 0.2$	$V_{IN} - 0.1$	—	V
			<b><math>V_{IN} - 0.3</math></b>	—	—	
		$V_{IN} < V_{TH(LO)}$ , $I_{DR} = 200\mu\text{A}$	—	35	150	mV
$I_{DR(PK)}$	Peak Drive Current	Sinking: $V_{IN} = 3.75\text{V}$ , $V_{DR} = 1\text{V}$ ; Sourcing: $V_{IN} = 4.3\text{V}$ , $V_{IN}-V_{DR} = 2\text{V}$	7	—	—	mA
			<b>6</b>	—	—	
$t_{DH}$	Drive High Delay (Notes 1,5)	$C_{DR} = 1.2\text{ nF}$ , $V_{IN}$ ramping up, measured from $V_{IN} = V_{TH(HI)}$ to $V_{DR} = 2\text{V}$	—	4	—	$\mu\text{sec}$
			—	—	<b>8</b>	
$t_{DL}$	Drive Low Delay (Notes 1,5)	$C_{DR} = 1.2\text{ nF}$ , $V_{IN}$ ramping down, measured from $V_{IN} = V_{TH(LO)}$ to $V_{DR} = 2\text{V}$	—	0.6	1.5	$\mu\text{sec}$
			—	—	<b>3.0</b>	

- NOTES:**
1. Guaranteed by design.
  2. See 5V Detect Thresholds on page 4.
  3. Recommended source impedance for 5V supply;  $\leq 0.25\Omega$ . This will ensure that  $I_{OUT} \times R_{SOURCE} < V_{HYST}$ , thus avoiding  $D_R$  toggling during 5V detect threshold transitions.
  4. In application circuit below.
  5. See timing diagram on page 4.
  6. Ground current is independent of  $I_{LOAD}$ .

### PIN DESCRIPTION

Pin Number	Name	Description
1	$V_{IN}$	Main Input Supply for the TC1267, nominally 5V.
2	NC	Not connected.
3	$V_{AUX}$	Auxiliary Input Supply, nominally 3.3V.
4	GND	Logic and power ground.
5	NC	Not connected.
6	SENSE	Sense Pin for $V_{OUT}$ . Connect to $V_{OUT}$ at the load to minimize voltage drop across PCB traces.
7	$V_{OUT}$	LDO 3.3V output.
8	$D_R$	Driver output for external P-channel MOSFET pass element.

### APPLICATION CIRCUIT



TC1267

**Thermal Considerations**

**Thermal Shutdown**

Integrated thermal protection circuitry shuts the regulator off when die temperature exceeds 160°C. The regulator remains off until the die temperature drops to approximately 150°C.

**Power Dissipation**

The amount of power the regulator dissipates is primarily a function of input and output voltage, and output current. The following equation is used to calculate worst case *actual* power dissipation:

$$P_D \approx (V_{INMAX} - V_{OUTMIN}) I_{LOADMAX}$$

Where:  $P_D$  = worst case actual power dissipation  
 $V_{INMAX}$  = maximum voltage on  $V_{IN}$   
 $V_{OUTMIN}$  = minimum regulator output voltage  
 $I_{LOADMAX}$  = maximum output (load) current

Equation 1.

The maximum *allowable* power dissipation (Equation 2) is a function of the maximum ambient temperature ( $T_{AMAX}$ ), the maximum allowable die temperature (95°C) and the thermal resistance from junction-to-air ( $\theta_{JA}$ ).

$$P_{DMAX} = \frac{(T_{JMAX} - T_{AMAX})}{\theta_{JA}}$$

Where all terms are previously defined.

Equation 2.

GIVEN:  $V_{INMAX} = 5V \pm 5\%$   
 $V_{OUTMIN} = 3.217$   
 $I_{LOADMAX} = 400mA$   
 $T_{JMAX} = 95^\circ C$   
 $T_{AMAX} = 70^\circ C$   
 $\theta_{JA} = 27^\circ C/W$  (DDPAK mounted on 1000 sq mm topside copper area)

- FIND: 1. Actual power dissipation  
 2. Maximum allowable dissipation

Actual power dissipation:

$$P_D \approx (V_{INMAX} - V_{OUTMIN}) I_{LOADMAX}$$

$$= (5.25V - 3.217V) 400mA$$

$$= \underline{813 \text{ mW}}$$

Maximum allowable power dissipation:

$$P_{DMAX} = \frac{(T_{JMAX} - T_{AMAX})}{\theta_{JA}}$$

$$= \frac{(95^\circ C - 70^\circ C)}{27^\circ C/W}$$

$$= \underline{926 \text{ mW}}$$

In this example, the TC1267 dissipates a maximum of only 813 mW; below the allowable limit of 926 mW.

**Table 1. Thermal Resistance Guidelines for TC1267 in 5-Pin DDPAK**

Copper Area (Topside)*	Copper Area (Backside)	Board Area	Thermal Resistance ( $\theta_{JA}$ )
2500 sq mm	2500 sq mm	2500 sq mm	25°C/W
1000 sq mm	2500 sq mm	2500 sq mm	27°C/W
125 sq mm	2500 sq mm	2500 sq mm	35°C/W

NOTES: \*Tab of device attached to topside copper

Equation 1 can be used in conjunction with Equation 2 to ensure regulator thermal operation is within limits. For example:

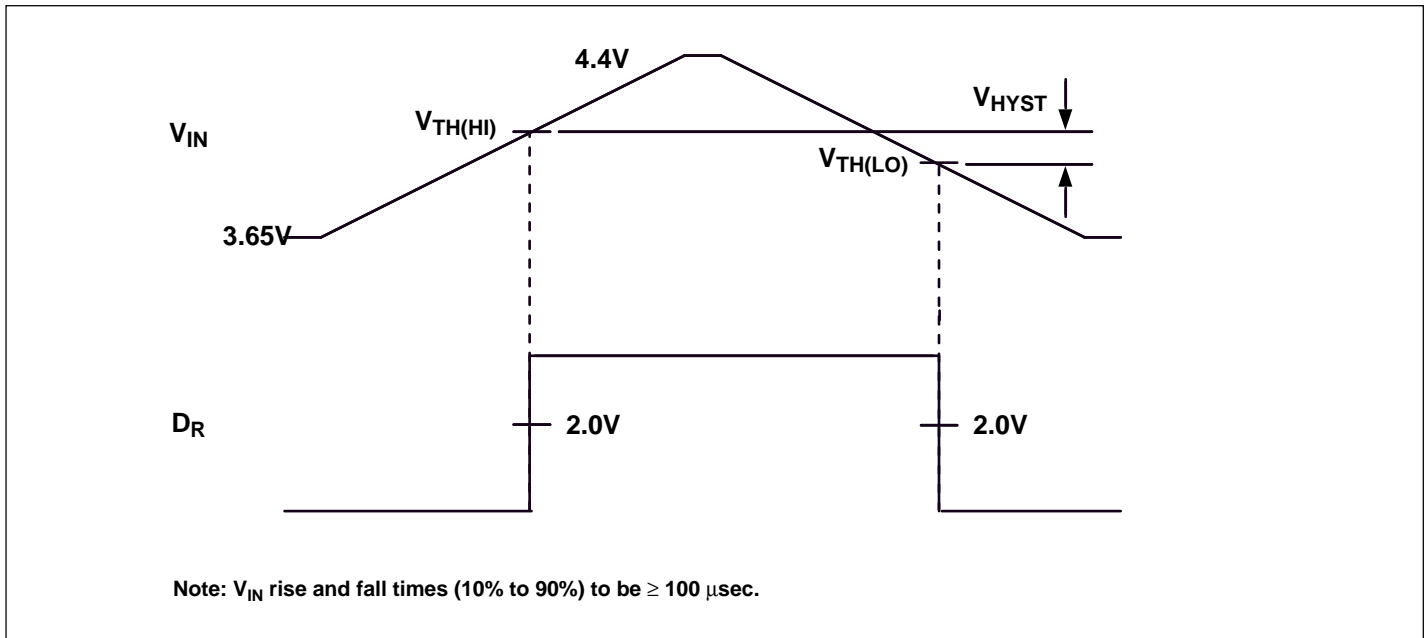


Figure 1. 5V Detect Threshold

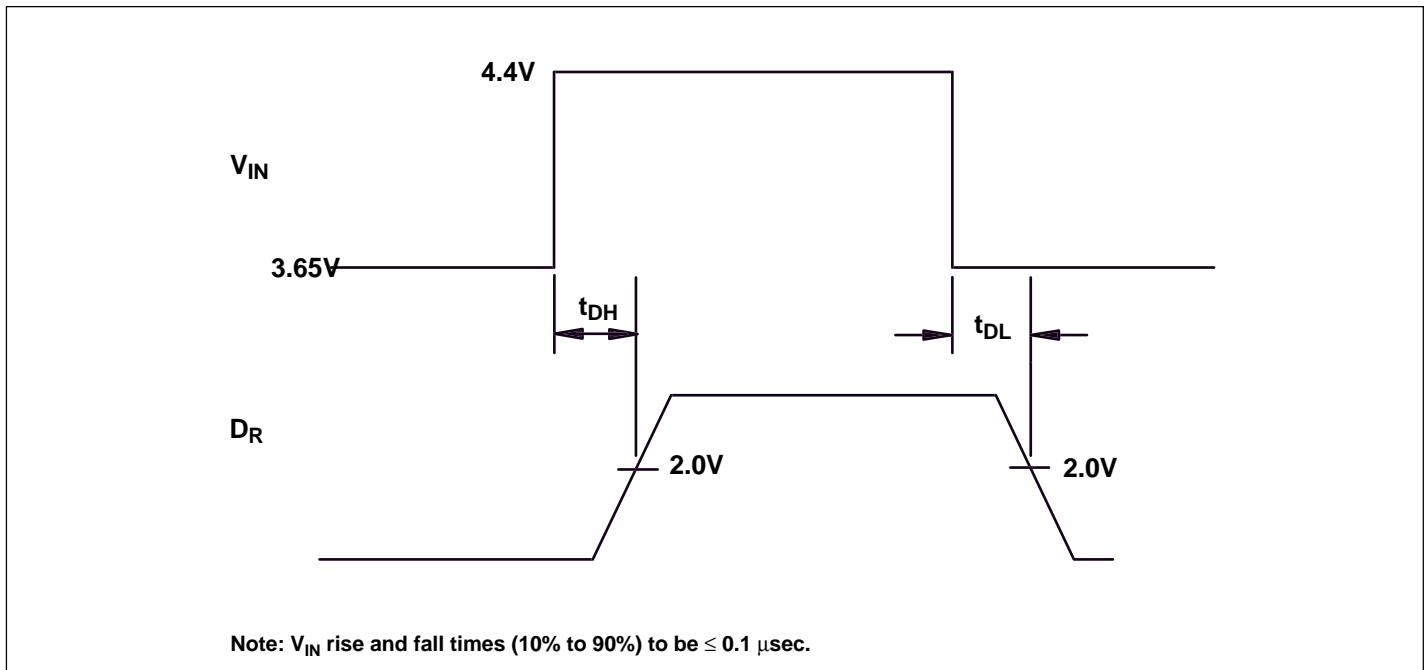
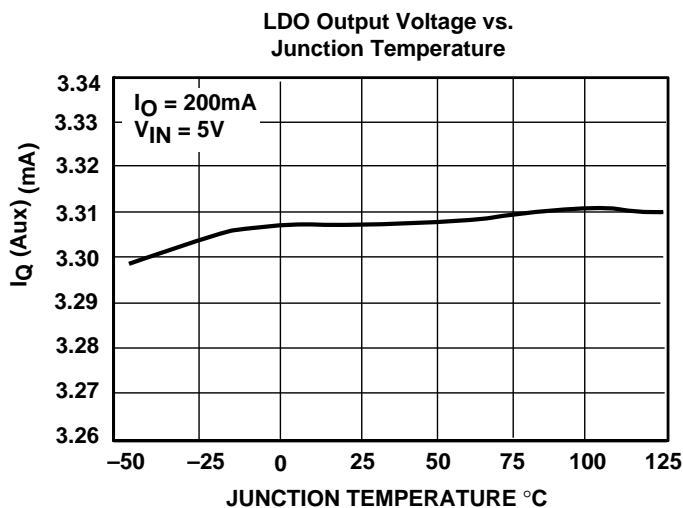
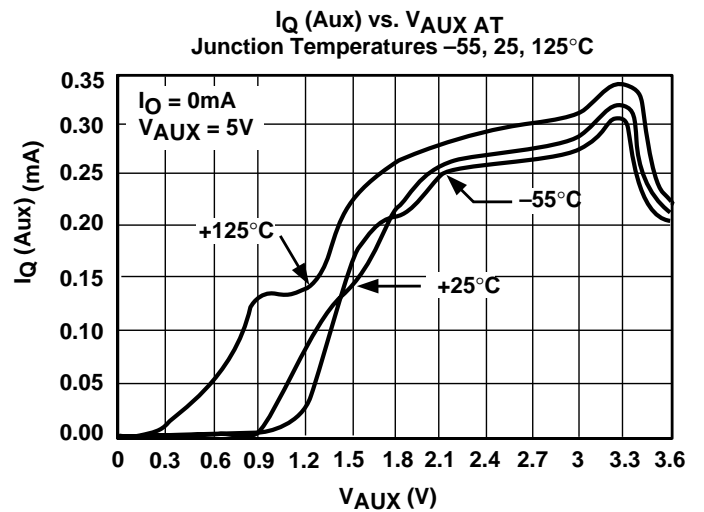
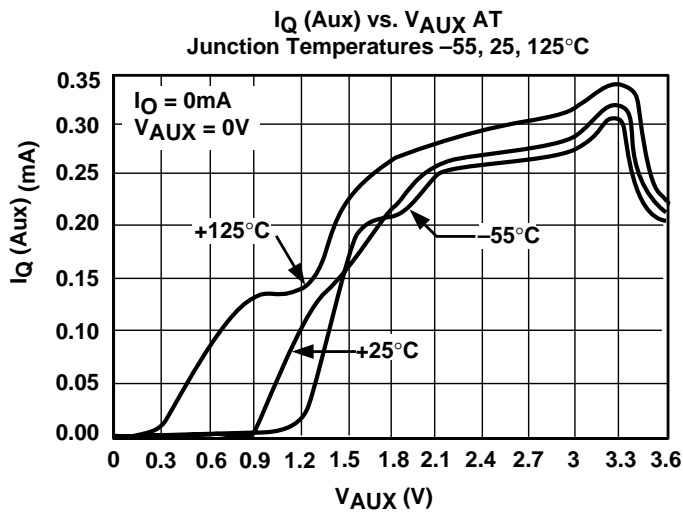
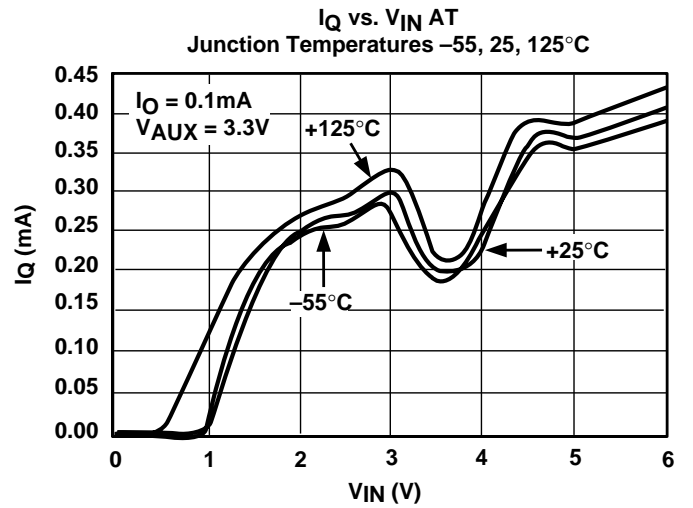
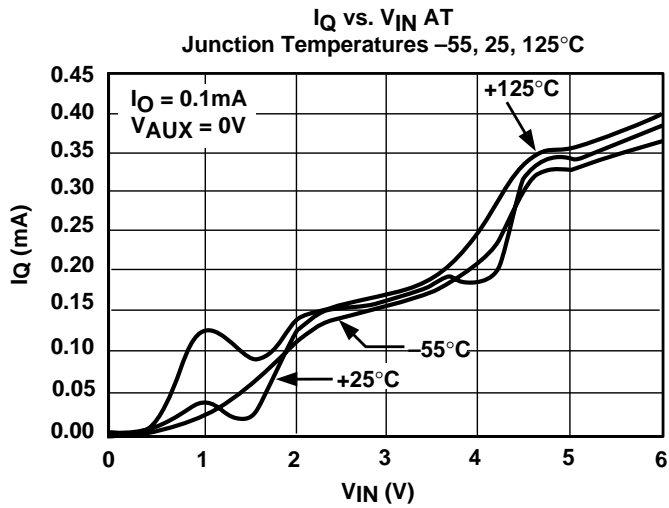


Figure 2. Timing Diagram

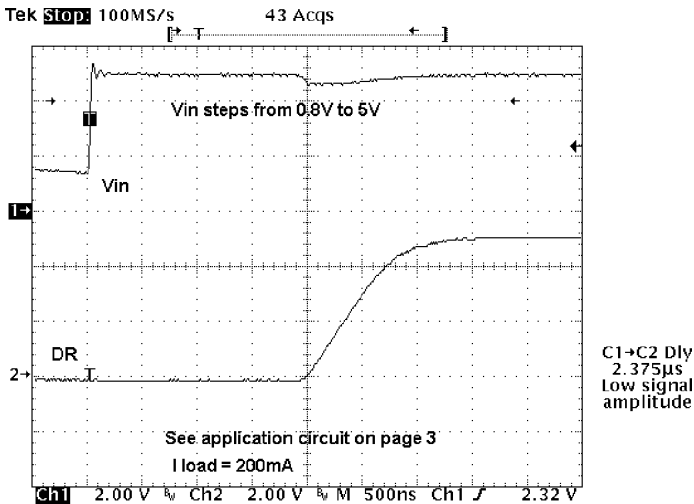
TC1267

TYPICAL CHARACTERISTICS



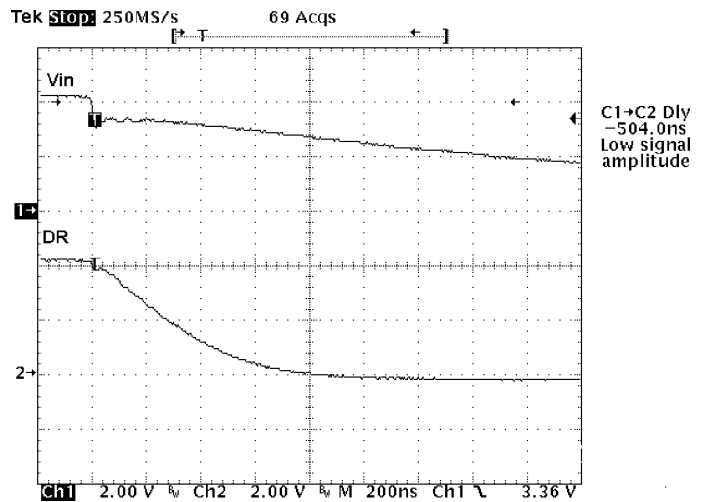
TYPICAL CHARACTERISTICS (CONT.)

Drive High Delay



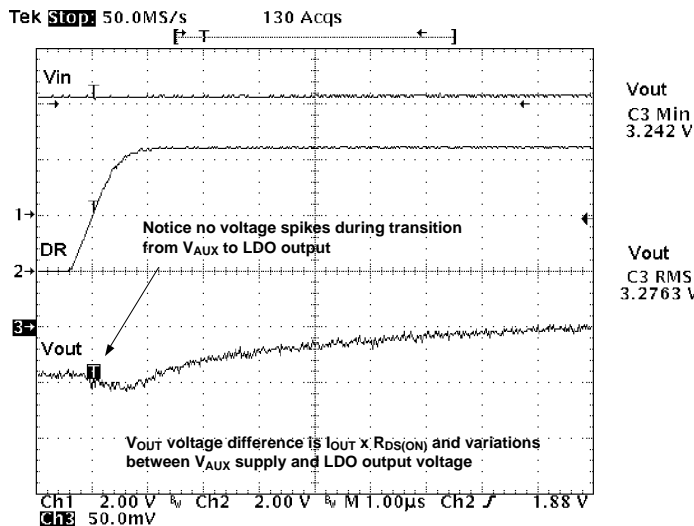
Trace 1:  $V_{IN}$  stepping for 0.8V to 5V  
Trace 2:  $D_R$  going high at  $V_{TH}(HI)$   
 $T_{dH} = < 4\mu S$

Drive Low Delay



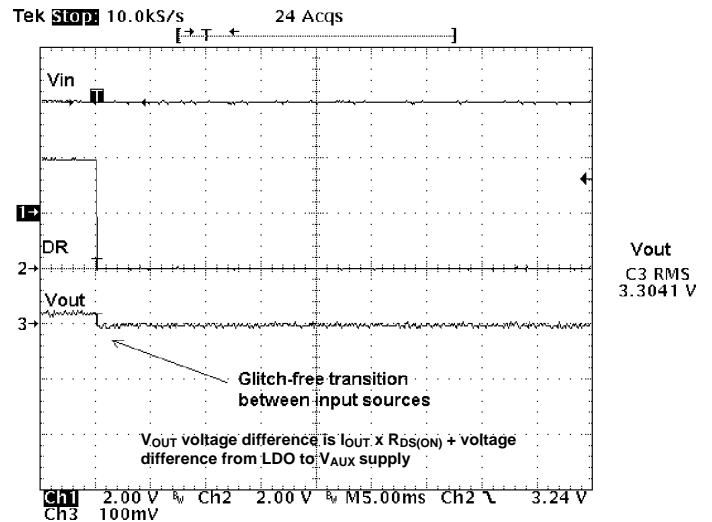
Trace 1:  $V_{IN}$  stepping for 5.5V to 0V  
Trace 2:  $D_R$  going low  
 $T_{dL} = < 600nS$

$V_O$  (min) with  $V_{IN}$  Rising



Trace 1:  $V_{IN}$  – 3A charging a 1500 $\mu F$  capacitor  
Trace 2:  $D_R$  going high at  $V_{TH}(HI)$   
Trace 3:  $V_{OUT}$ , offset 3.3V.  $V_{OUT}(min) = 3.24V$   
 $I_{LOAD} = 200\mu A$

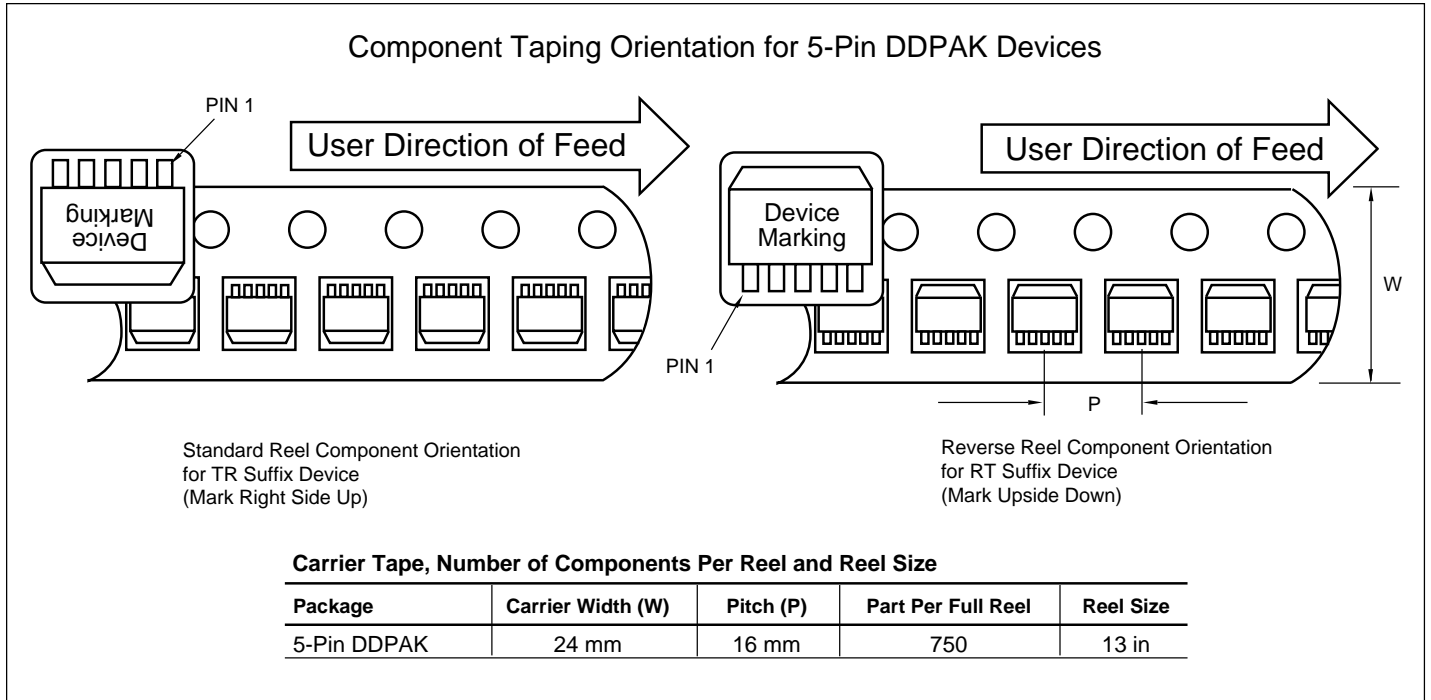
$V_O$  (min) with  $V_{IN}$  Falling



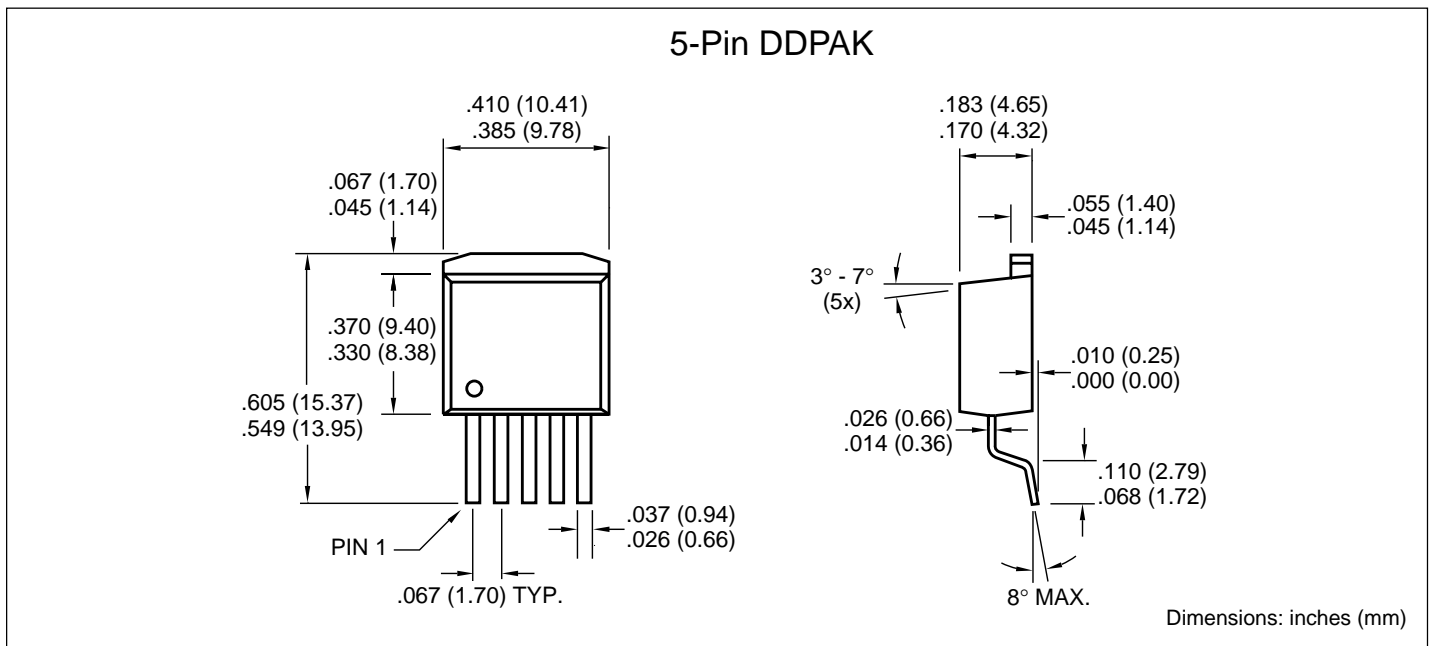
Trace 1:  $V_{in}$  – discharging a 1500 $\mu F$  capacitor  
Trace 2:  $D_R$  going low at  $V_{TH}(LO)$   
Trace 3:  $V_{OUT}$ , offset 3.3V.  $V_{OUT}(min) = 3.14V$   
 $I_{LOAD} = 200\mu A$

TC1267

TAPING FORM



PACKAGE DIMENSIONS







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