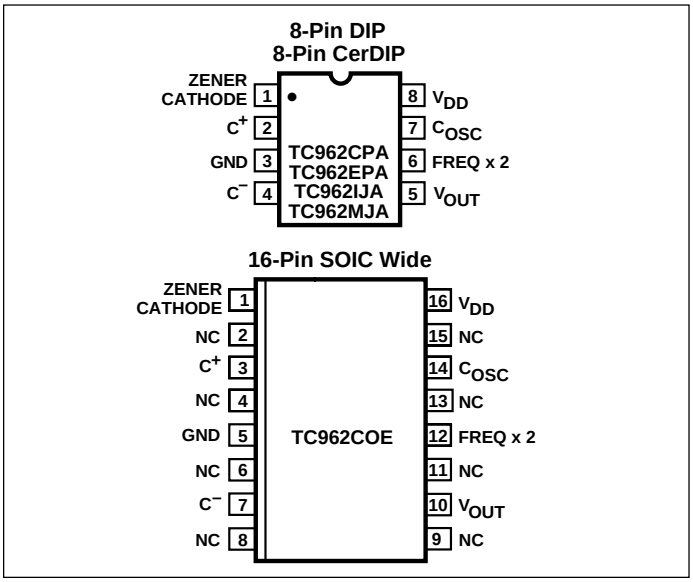
HIGH CURRENT CHARGE PUMP DC-TO-DC CONVERTER

FEATURES

- **Pin Compatible With TC7662/ICL7662/SI7661**
- **High Output Current 80mA**
- **No External Diodes Required**
- **Wide Operating Range ..... 3V to 18V**
- **Low Output Impedance ..... 28Ω Typ.**
- **No Low Voltage Terminal Required**
- **Application Zener On Chip**
- **OSC Frequency Doubling Pin Option for Smaller Output Capacitors**

PIN CONFIGURATIONS (DIP and SOIC)



GENERAL DESCRIPTION

The TC962 is an advanced version of the industry-standard 7662 high-voltage DC-to-DC converter. Using improved design techniques and CMOS construction, the TC962 can source as much as 80mA versus the 7662's 20mA capability.

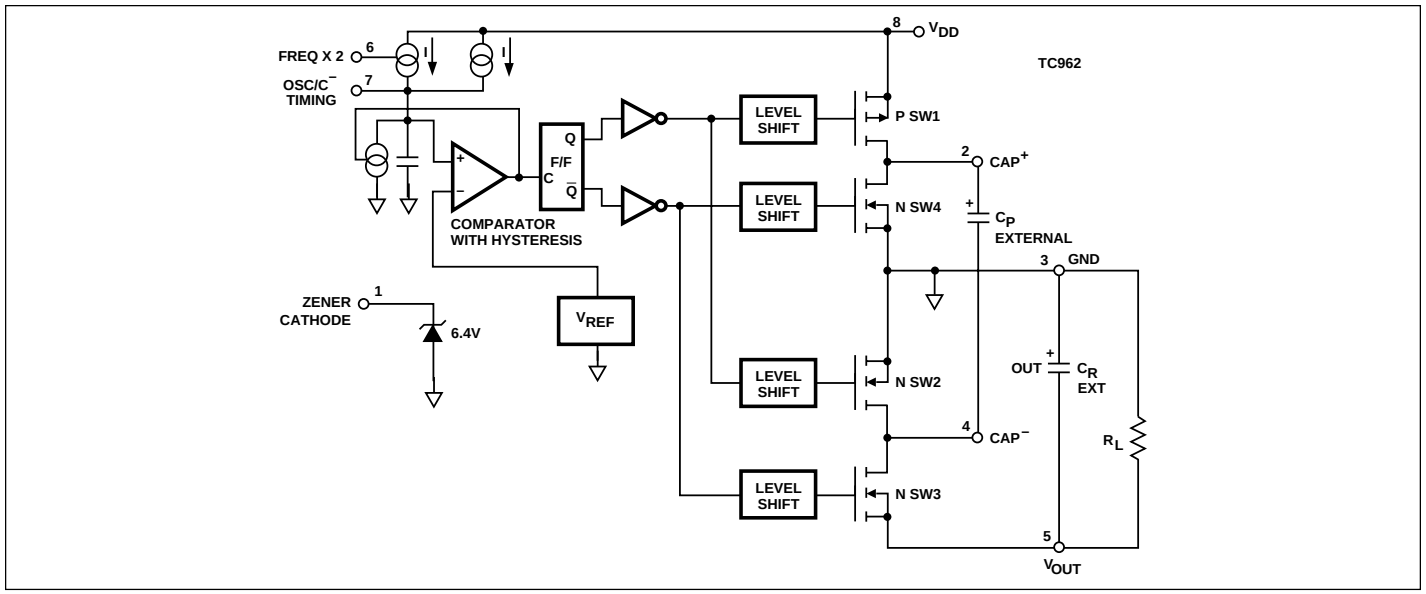
As an inverter, the TC962 can put out voltages as high as 18V and as low as 3V without the need for external diodes. The output impedance of the device is a low 28Ω (with the proper capacitors), voltage conversion efficiency is 99.9%, and power conversion efficiency is 97%.

The low voltage terminal (pin 6) required in some 7662 applications has been eliminated. Grounding this terminal will double the oscillator frequency from 12kHz to 24kHz. This will allow the use of smaller capacitors for the same output current and ripple, in most applications. Only two external capacitors are required for inverter applications. In the event an external clock is needed to drive the TC962 (such as paralleling), driving this pin directly will cause the internal oscillator to sync to the external clock.

ORDERING INFORMATION

Part No.	Package	Temp. Range
TC962COE	16-Pin SOIC Wide	0°C to +70°C
TC962CPA	8-Pin Plastic DIP	0°C to +70°C
TC962EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC962IJA	8-Pin CerDIP	– 25°C to +85°C
TC962MJA	8-Pin CerDIP	– 55°C to +125°C
TC7660EV	***Evaluation Kit for Charge Pump Family***	

FUNCTIONAL BLOCK DIAGRAM



TC962

Pin 1, which is used as a test pin on the 7662, is a voltage reference zener on the TC962. This zener (6.4V at 5 mA) has a dynamic impedance of 12Ω and is intended for use where the TC962 is supplying current to external regulator circuitry and a reference is needed for the regulator circuit. (See applications section.)

The TC962 is compatible with the LTC1044, SI7661, and ICL7662. It should be used in designs that require greater power and/or less input to output voltage drop. It offers superior performance over the ICL7660S.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{DD} to GND) ..... +18V
Input Voltage Any Pin ..... (V_{DD} + 0.3) to (V_{SS} – 0.3)
Current Into Any Pin 10mA
ESD Protection ..... ±2000V
Output Short Circuit ..... Continuous (at 5.5V Input)
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Operating Temperature Range
- CPA, COE ..... 0°C to +70°C
- IJA ..... – 25°C to +85°C
- EPA ..... – 40°C to +85°C
- MJA ..... – 55°C to +125°C

Package Power Dissipation ($T_A \leq 70°C$)
- SOIC 760mW
- PDIP 730mW
- CerDIP 800mW

Package Thermal Resistance
- CerDIP, $R_{\theta J-A}$ ..... 90°C/W
- PDIP, $R_{\theta J-A}$ ..... 140°C/W

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_{DD} = 15V, T_A = +25°C (See Test Circuit), unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		3		18	V
I_S	Supply Current	$R_L = \infty$	—	—	—	—
	V_{DD} = 15V	T_A = +25°C		510	700	µA
		$0 \leq T_A \leq +70°C$		560		µA
		$–55 \leq T_A \leq +125°C$		650		µA
	V_{DD} = 5V	T_A = +25°C		190		µA
		$0 \leq T_A < +70°C$		210		µA
		$–55 \leq T_A \leq +125°C$		210		µA
R_O	Output Source Resistance	I_L = 20mA, V_{DD} = 15V	—	32	37	Ω
		I_L = 80mA, V_{DD} = 15V		35	40	Ω
		I_L = 3mA, V_{DD} = 5V		—	50	Ω
C_{OSC}	Oscillator Frequency	Pin 6 Open	—	12	—	kHz
		Pin 6 GND		24		kHz
P_{EFF}	Power Efficiency	V_{DD} = 15V R_L = 2kΩ	93	97	—	%
V_{DEF}	Voltage Efficiency	V_{DD} = 15V $R_L = \infty$	99	99.9	—	%
		Over Temperature Range	96	—		%
V_Z	Zener Voltage	I_Z = 5mA	6.0	6.2	6.4	V
Z_{ZT}	Zener Impedance	I_L = 2.5mA to 7.5mA	—	12		Ω

APPLICATIONS INFORMATION

Theory of Operation

The TC962 is a capacitive pump (sometimes called a switched capacitor circuit), where four MOSFET switches control the charge and discharge of a capacitor.

The functional diagram (page 1) shows how the switching action works. SW1 and SW2 are turned on simultaneously, charging C_P to the supply voltage, V_{IN}. This assumes that the on resistance of the MOSFETs in series with the capacitor results in a charging time (3 time constants) that is less than the on time provided by the oscillator frequency as shown:

$$3\ (R_{DS(ON)}\ C_P) < C_P/(0.5\ f_{OSC})$$

In the next cycle, SW1 and SW2 are turned off and after a very short interval of all switches being off (this prevents large currents from occurring due to cross conduction), SW3 and SW4 are turned on. The charge in C_P is then transferred to C_R, BUT WITH THE POLARITY INVERTED. In this way, a negative voltage is now derived.

Page 1 shows a functional diagram of the TC962. An oscillator supplies pulses to a flip-flop that is then fed to a set of level shifters. These level shifters then drive each set of switches at one-half the oscillator frequency.

The oscillator has two pins that control the frequency of oscillation. Pin 7 can have a capacitor added that is returned to ground. This will lower the frequency of the oscillator by adding capacitance to the timing capacitor internal to the TC962. Grounding pin 6 will turn on a current source and double the frequency. This will double the charge current going into the internal capacitor, as well as any capacitor added to pin 7.

A zener diode has been added to the TC962 for use as a reference in building external regulators. This zener runs from pin 1 to ground.

Capacitors

In early charge pump converters, the capacitors were not considered critical due to the high $R_{DS(ON)}$ of the MOSFET switches. In order to understand this, let's look at a model of a typical electrolytic capacitor (Figure 1).

Note that one of its characteristics is ESR (equivalent series resistance). This parasitic resistance winds up in series with the load. Thus, both voltage conversion efficiency and power conversion efficiency are compromised if a low ESR capacitor is not used.

In the test circuit, for example, just changing two capacitors, C_P and C_R, from capacitors with unspecified ESR to low ESR-type output, impedance changes from 36Ω to 28Ω, an improvement of 23%!

This applies to all types of capacitors, including film types (polyester, polycarbonate, etc.).

Some applications information suggest that the capacitor is not critical and attribute the limiting factor of the capacitor to its reactive value. Let's examine this:

$$X_C = \frac{1}{2\pi f\ C} \quad \text{and} \quad Z_C = \frac{X_C}{DS},$$

where DS (duty cycle) = 50%.

Thus, $Z_C \approx 2.6\Omega$ at f = 12kHz, where C = 10µF.

For the TC962, f = 12,000Hz, and a typical value of C would be 10µF. This is a reactive impedance of ≈ 2.6Ω. If the ESR is as great as 5Ω, the reactive value is not as critical as it would first appear, as the ESR would predominate. The 5Ω value is typical of a general-purpose electrolytic capacitor.

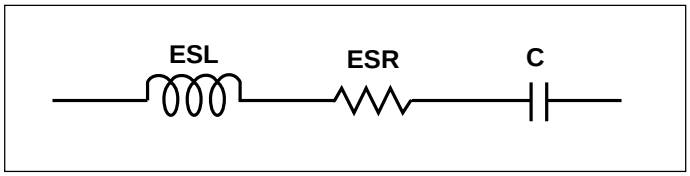
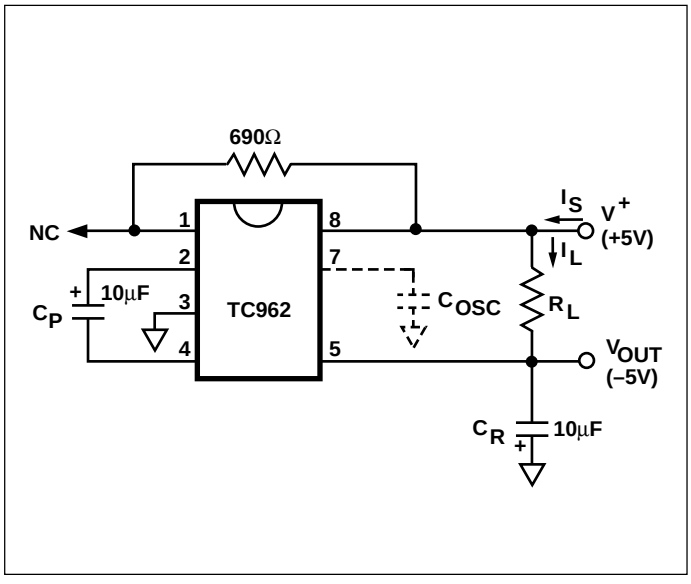


Figure 1. Typical Electrolytic Capacitor

Latch Up

All CMOS structures contain a parasitic SCR. Care must be taken to prevent any input from going above or below the supply rail, or latch up will occur. The result of latch up is an effective short between V_{DD} and V_{SS}. Unless the power supply input has a current limit, this latch-up phenomena will result in damage to the device. (See Application Note 31 for additional information.)

TEST CIRCUIT



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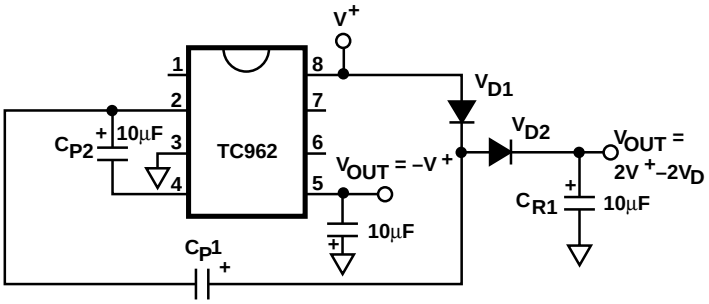
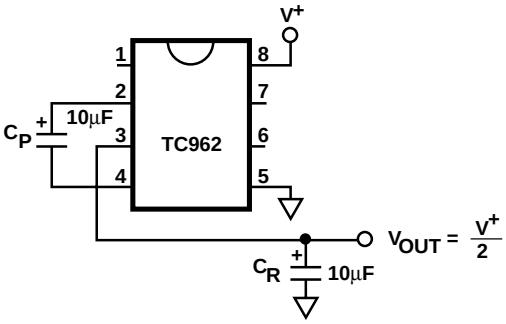
TYPICAL APPLICATIONS

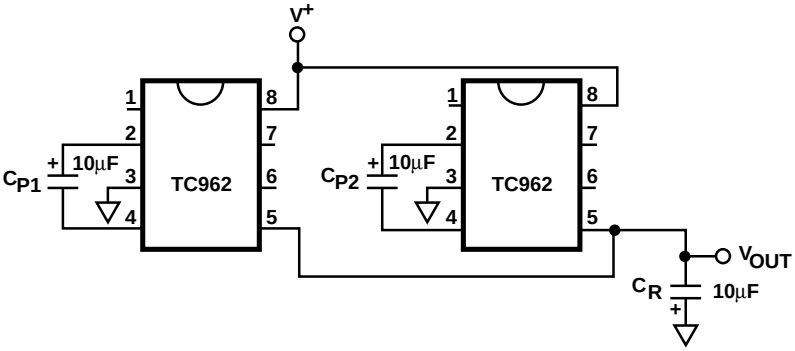
Combined Negative Converter and Positive Multiplier



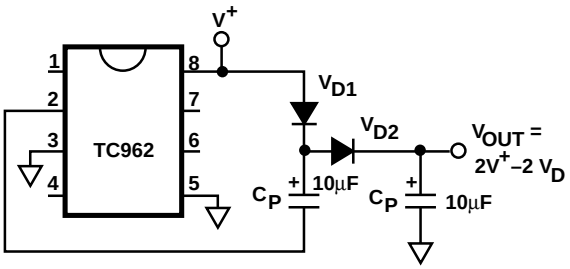
Split V^+ In Half



Lowering Output Resistance by Paralleling Devices

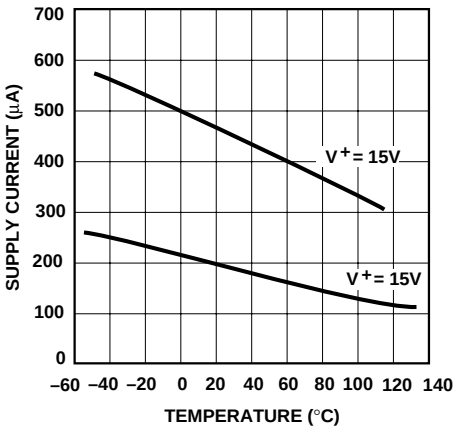


Positive Voltage Multiplier

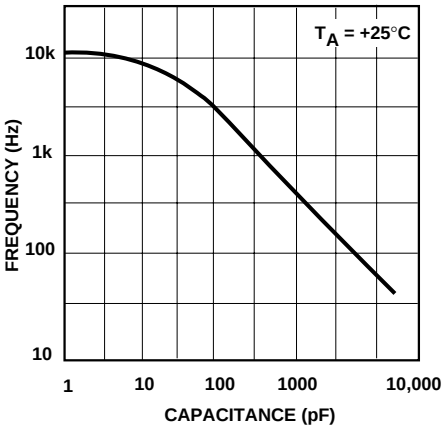


TYPICAL CHARACTERISTICS

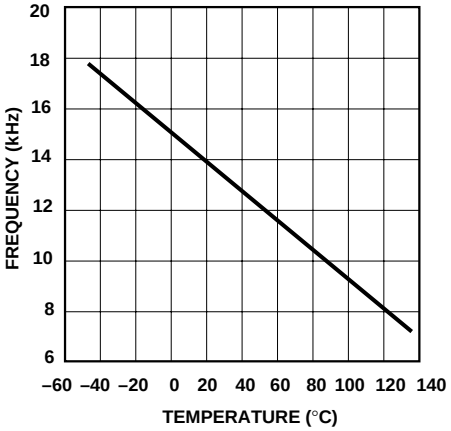
Supply Current vs. Temperature



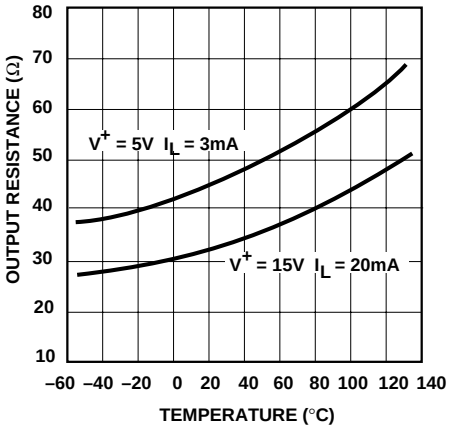
Oscillator Frequency vs. C_{EXT}



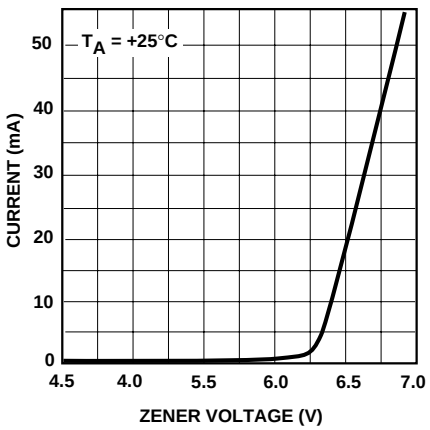
Frequency vs. Temperature



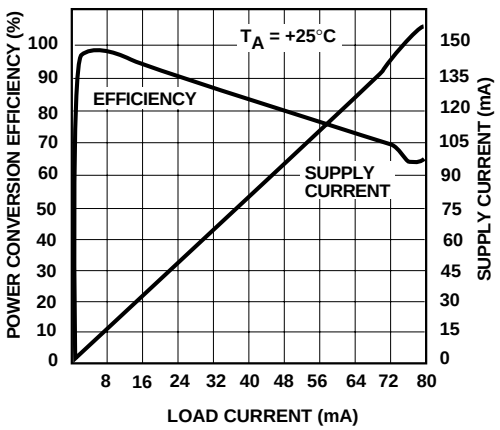
Output Resistance vs. Temperature



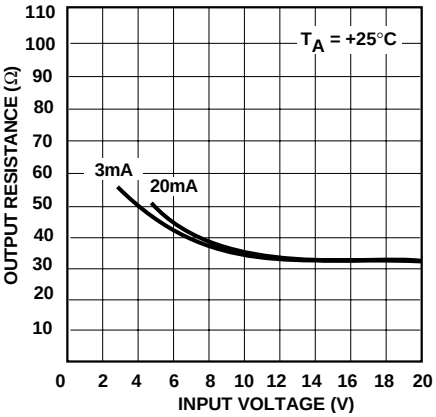
Current vs. Zener Voltage



Power Conversion Efficiency vs. I_{LOAD}



Output Resistance vs. Input Voltage



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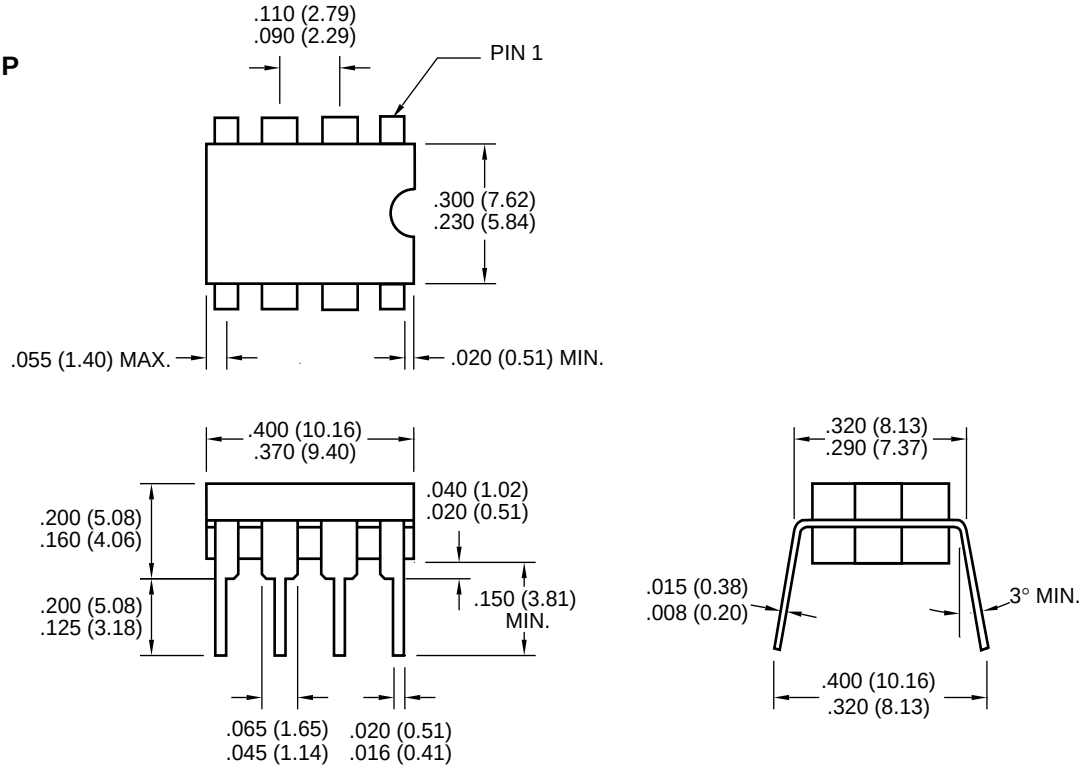
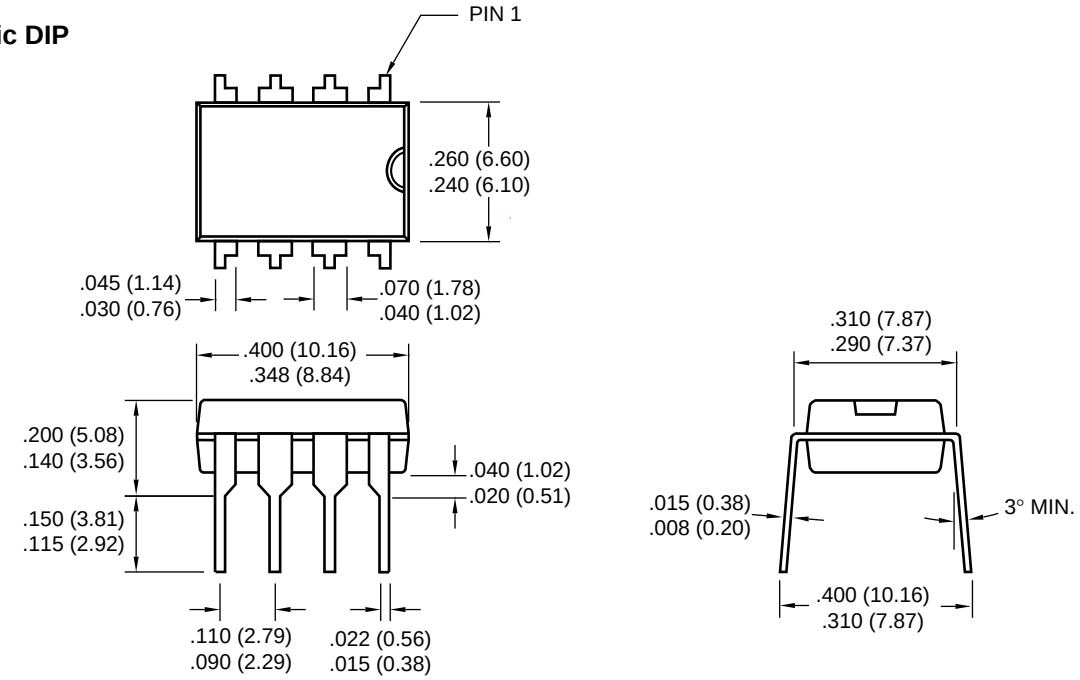
PACKAGE DIMENSIONS

8-Pin CerDIP



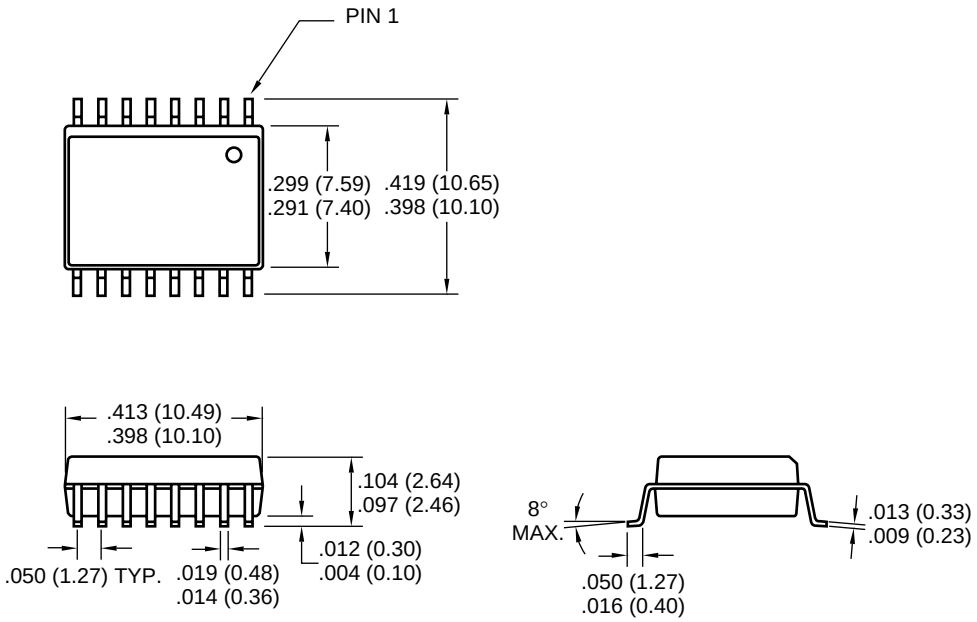
8-Pin Plastic DIP



Dimensions: inches (mm)

PACKAGE DIMENSIONS (Cont.)

16-Pin SOIC Wide



Dimensions: inches (mm)

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