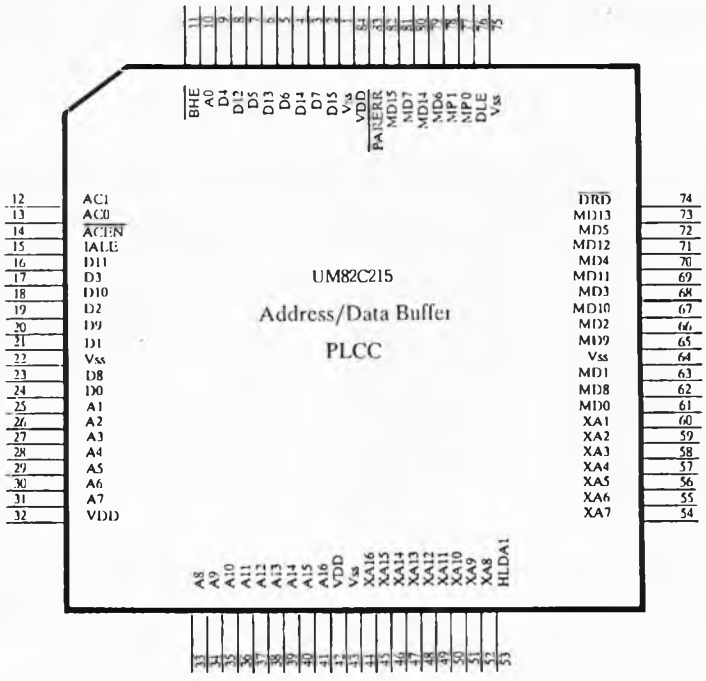
3. UM82C215 Data / Address Buffer

The UM82C215 Data/Address buffer, basically, provides the functions of buffering and latching among several buses. The 16 bit to 8 bit bus conversion is also performed by the UM82C215 when the conversion is needed. The parity checking will be performed when the UM82C215 receives data and the parity bit will be generated when the UM82C215 sends data out. The major functions of the UM82C215 are address buffering and latching, data buffering and latching, bus conversion, parity checking and parity bit generation.



3.1 Address Buffers and Latches

The address buffering between the CPU address lines A16-A1 and the X bus address lines XA16-XA1 is provided by the UM82C215. The IALE is used to latch the CPU address lines.

3.2 Data Buffers and Latches

The UM82C215 provides the buffering between the CPU data bus D15-D0 and the memory data bus MD15-MD0. The memory data bus can be latched. However, the latch enable is controlled by the DRD, ACEN, and action codes.

3.3 Bus Conversion

When the 16 bit CPU accesses data from/to 8 bit devices, the function of bus conversion is needed. The UM82C215 provides the bus conversion for the CPU 80286 to read/write data from/to 8 bit devices. The bus conversion for DMA cycles is also provided. All of these conversions are controlled by the action codes.

AC1	AC0	Cycle	Operation
0	0	CPU	Write - 16 Bits
0	1	CPU	Read - 16 Bits
0	0	CPU	Write - 8 Bits (low byte)
0	1	CPU	Read - 8 Bits (low byte)
1	0	CPU	Write - 8 Bits (high byte)
1	1	CPU	Read - 8 Bits (high byte)
1	0	DMA/MASTER	Write - 8 Bits (high byte)
1	1	DMA/MASTER	Read - 8 Bits (high byte)

3.4 Parity Checking and Generation

The UM82C215 checks the parity for each data byte read from local memory. If any parity error is detected, the UM82C215 then activates PARERR. In addition, the UM82C215 generates a parity bit for each data byte which is going to be written to local memory.