I General Description

The UM82C382 Address Buffer is in UMC's 82C380 series High End AT (HEAT) Chip Set. It provides address interface to processor address, system address, DMA address XA and Latched Bus. A 10-bit refresh counter is built in for both 256K and 1M DRAM refresh. Two address decoders are included for ROM space and on-board I/O port.

II Features

- 24 bit address line buffer
- Supports 256Kx1 and 1Mx1 DRAM refresh
- Advanced 1.2μ CMOS Technology
- 120 pin flat package

III Block Diagram

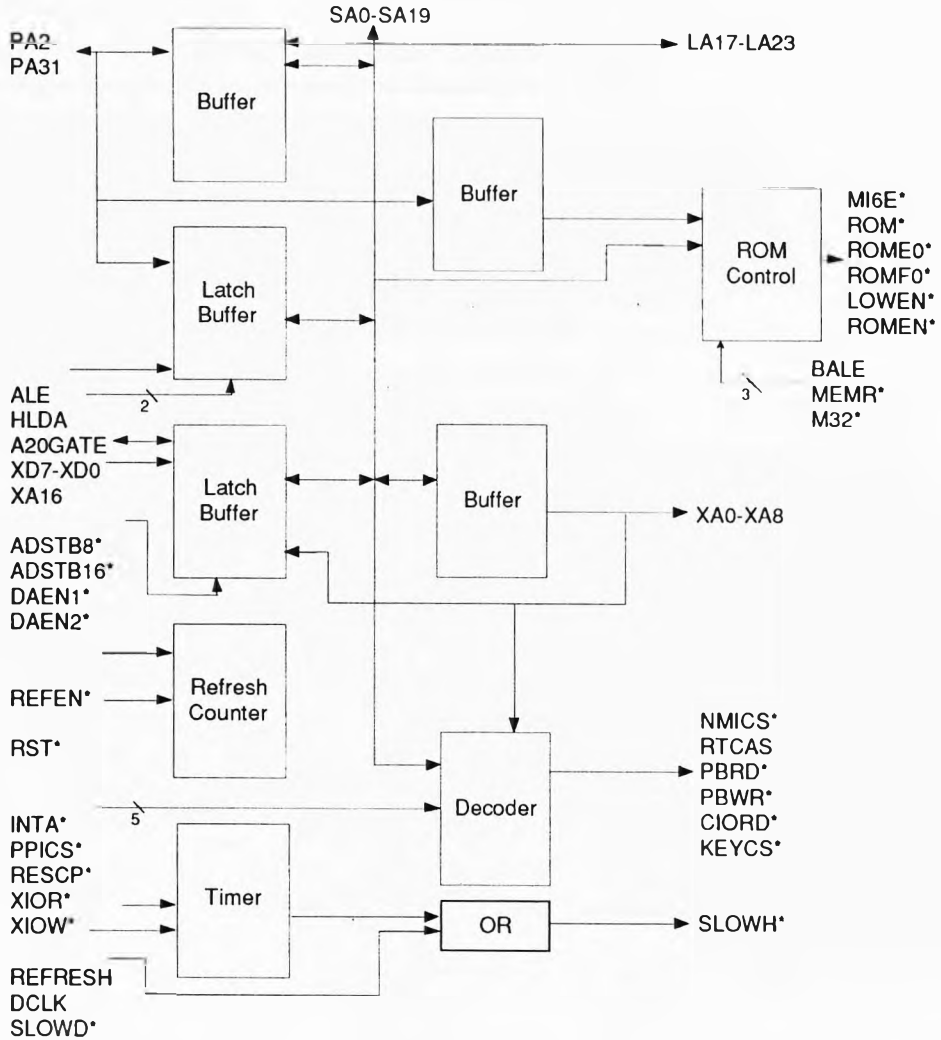

Figure 1. UM82C382 Block Diagram

IV Pin Configuration

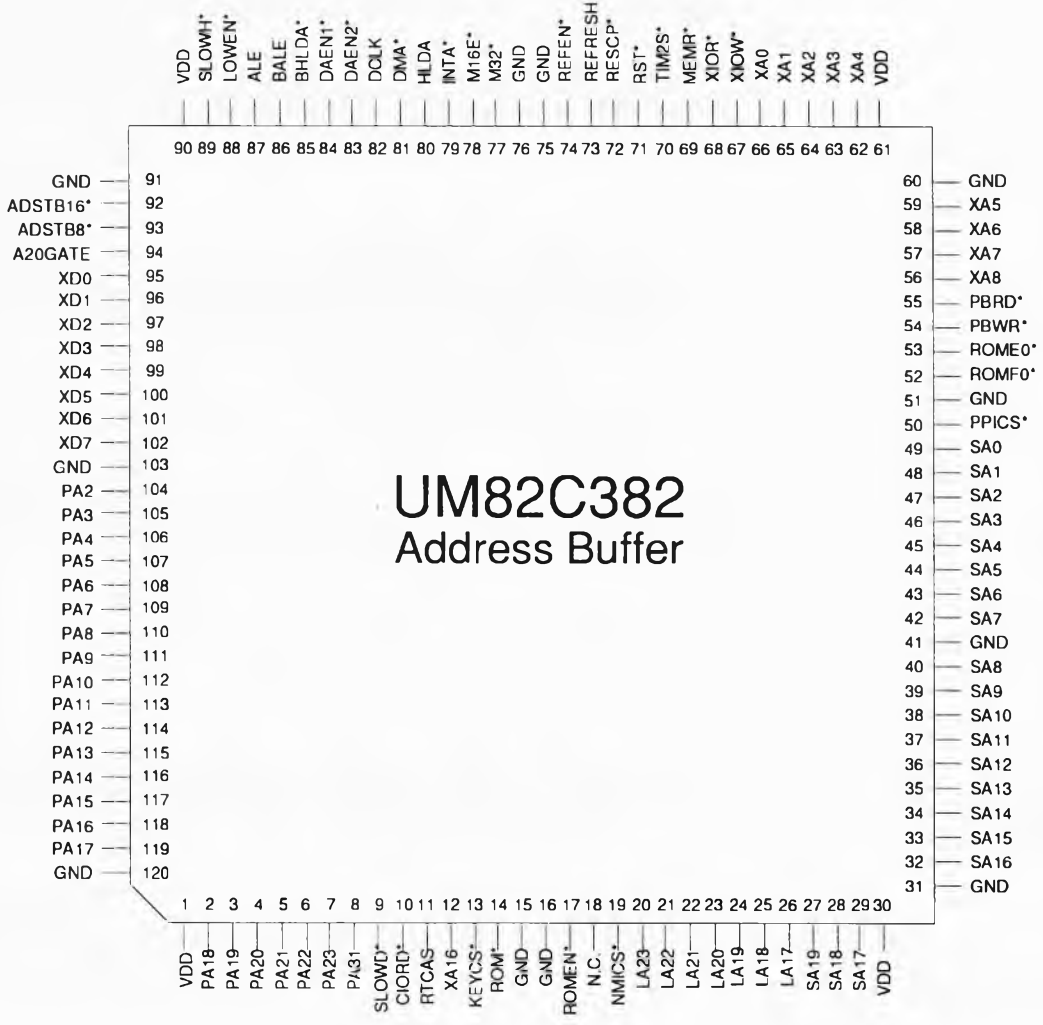

Figure 2. Pin Configuration

VI Functional Description

The UM82C382 is an address interface between processor bus, system bus and peripheral bus (X-bus).

During the CPU cycle, address PA2-PA19 from CPU bus will be linked to system bus and X-bus, while PA17-PA23 will be linked to LA17-LA23 of the system bus. If the ROM address space is selected during this period, the ROM control unit will generate the signals to access the ROM address, the decoder will also generate signals to access I/O port data.

During the DMA cycle, address LA17-LA23 from the system bus will be linked to PA17-PA23 of CPU bus, and SA2-SA19 will be linked to PA2-PA19. During this cycle, system address is generated from DMA controller or refresh counter. When REFEN* is active, the refresh counter will issue refresh address to the system bus. The refresh counter will be incremented by one automatically after the refresh cycle.

The DMA controller will dominate the system bus during the DMA cycle, both 8-bit and 16-bit data transfer types can be generated as DMA transfer. For 8-bit data transfer, with the negative transition of ADSTB8*, XA0-XA7 will be linked to SA0-SA7, XD7-XD0 will be linked to SA15-SA8, while the contents of SA15-SA8 will be latched in the latch buffer. For 16-bit data transfer, with the negative transition of ADSTB16*, XA8-XA0 will be linked to SA8-SA0, XD7-XD0 will be linked to SA16-SA9, while the contents of SA16-SA9 will be latched in the latch buffer.

A timer is also designed in UM82C382 to provide the necessary clock timing to be compatible with standard PC/AT 8-MHz bus. The user is able to slow down the system speed by enabling SLOWD* to keep the system timing compatible with PC/AT.