

SILICON TRANSISTOR ARRAY

μ PA1458

NPN SILICON POWER TRANSISTOR ARRAY

LOW SPEED SWITCHING USE (DARLINGTON TRANSISTOR)

INDUSTRIAL USE

DESCRIPTION

The μ PA1458 is NPN silicon epitaxial Darlington Power Transistor Array that built in Surge Absorber and 4 circuits designed for driving solenoid, relay, lamp and so on.

FEATURES

- Surge Absorber (C - B) built in.
- Easy mount by 0.1 inch of terminal interval.
- High h_{FE} for Darlington Transistor.

ORDERING INFORMATION

Part Number	Package	Quality Grade
μ PA1458H	10 Pin SIP	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25\text{ }^\circ\text{C}$)

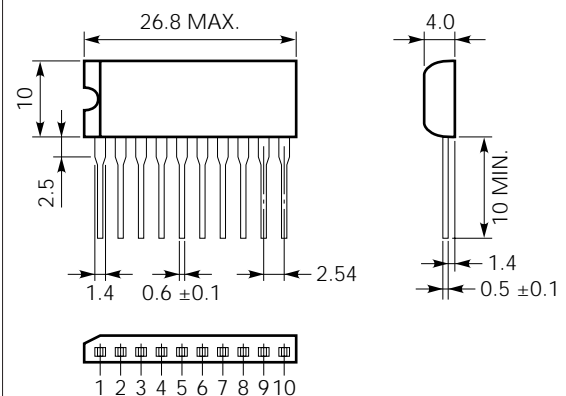
Collector to Base Voltage	V_{CBO}	60 ± 10	V
Collector to Emitter Voltage	V_{CEO}	60 ± 10	V
Emitter to Base Voltage	V_{EBO}	7	V
Surge Sustaining Energy	$E_{CEO(sus)}$	25	mJ/unit
Collector Current (DC)	$I_{C(DC)}$	± 5	A/unit
Collector Current (pulse)	$I_{C(pulse)^*}$	± 10	A/unit
Collector Current	$I_{CBS(DC)}$	5	mA/unit
Base Current (DC)	$I_{B(DC)}$	0.5	A/unit
Total Power Dissipation	P_{T1}^{**}	3.5	W
Total Power Dissipation	P_{T2}^{***}	28	W
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

* $PW \leq 300\ \mu s$, Duty Cycle $\leq 10\%$

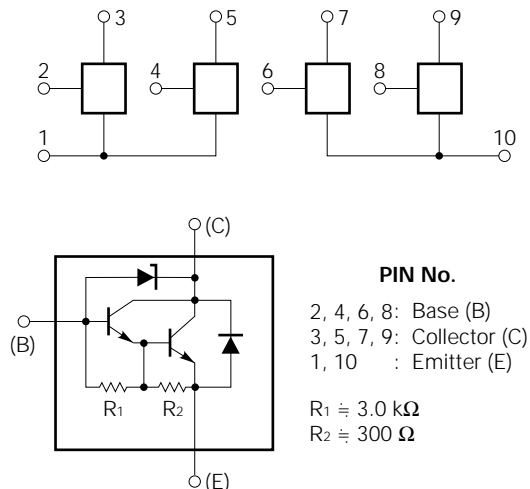
** 4 Circuits, $T_a = 25\text{ }^\circ\text{C}$

*** 4 Circuits, $T_c = 25\text{ }^\circ\text{C}$

PACKAGE DIMENSION (in millimeters)



CONNECTION DIAGRAM



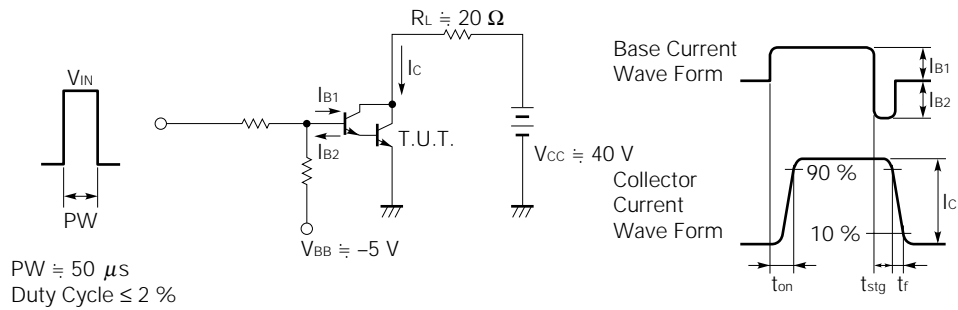
The information in this document is subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Collector Leakage Current	I _{CEs}			10	μA	V _{CE} = 40 V
Emitter Leakage Current	I _{EBO}			10	mA	V _{EB} = 5 V, I _C = 0
Collector to Emitter Sustaining Voltage	V _{CEO(sus)}	50	60	70	V	I _C = 3 A, L = 1 mH
DC Current Gain	h _{FE1} *	2000	7000	20000	—	V _{CE} = 2 V, I _C = 2 A
DC Current Gain	h _{FE2} *	500	3000		—	V _{CE} = 2 V, I _C = 4 A
Collector Saturation Voltage	V _{CE(sat)} *		0.9	1.5	V	I _C = 2 A, I _B = 2 mA
Base Saturation Voltage	V _{BE(sat)} *		1.6	2	V	I _C = 2 A, I _B = 2 mA
Turn On Time	t _{on}		1		μs	I _C = 2 A
Storage Time	t _{stg}		7		μs	I _{B1} = -I _{B2} = 2 mA V _{CC} ≅ 40 V, R _L ≅ 20 Ω
Fall Time	t _f		2		μs	See test circuit

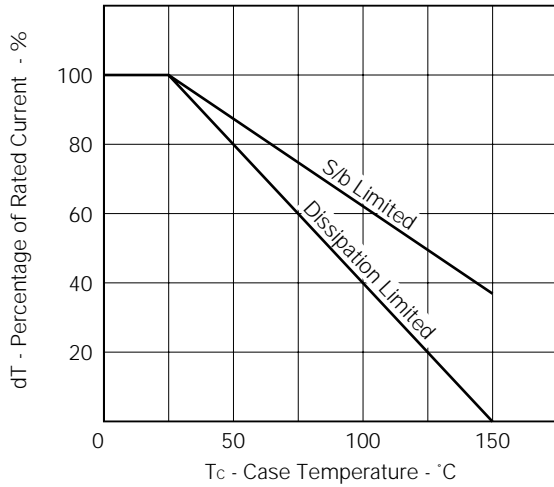
* PW ≤ 350 μs, Duty Cycle ≤ 2 % / pulsed

SWITCHING TIME TEST CIRCUIT

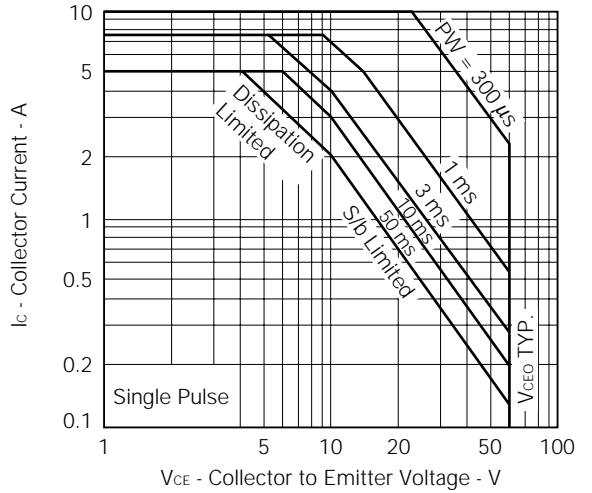


TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

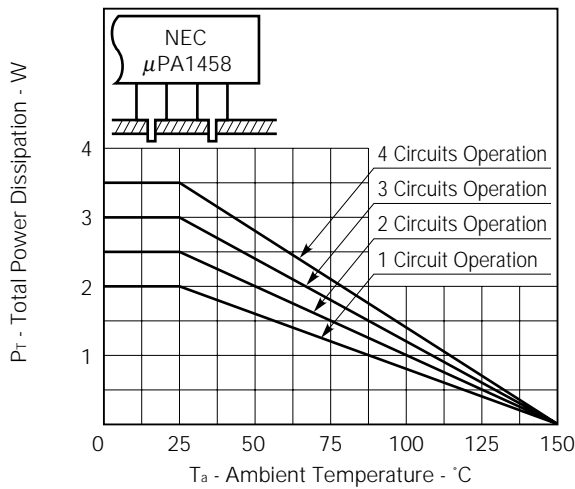
DERATING CURVE OF SAFE OPERATING AREA



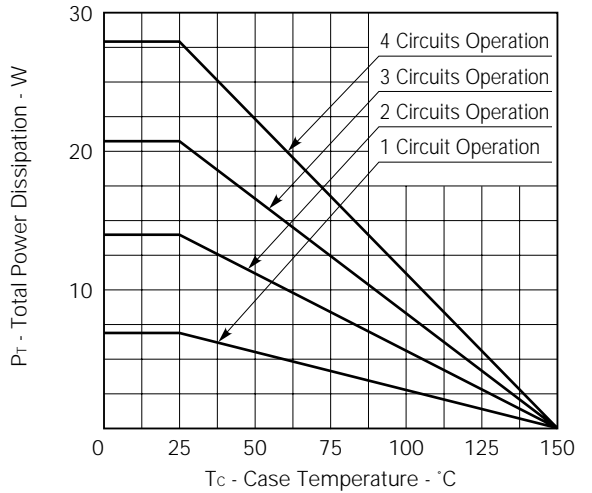
SAFE OPERATING AREA



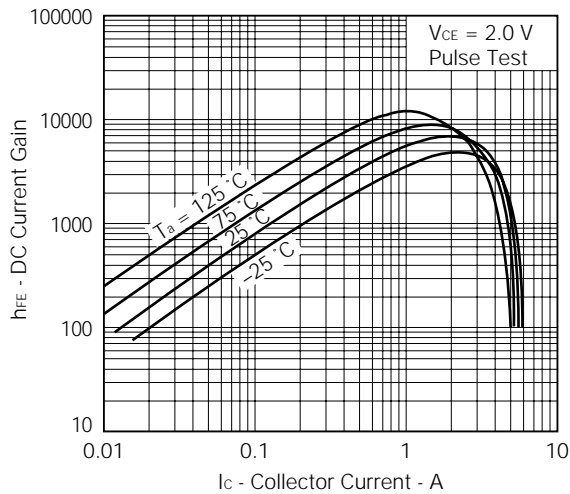
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



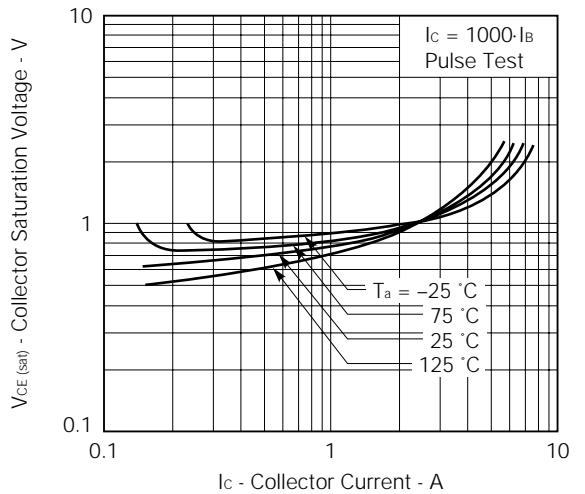
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

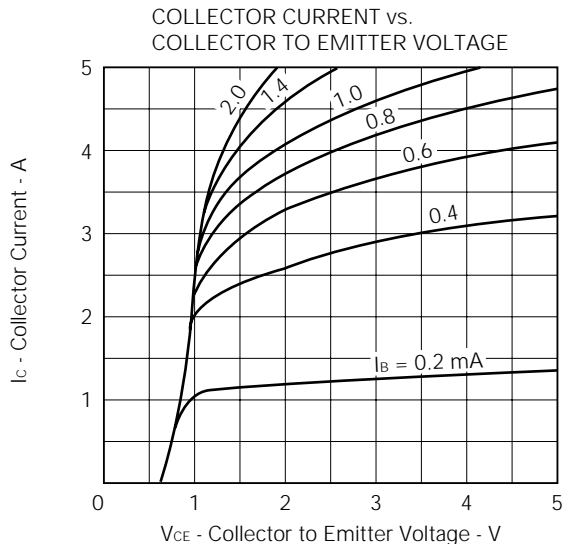
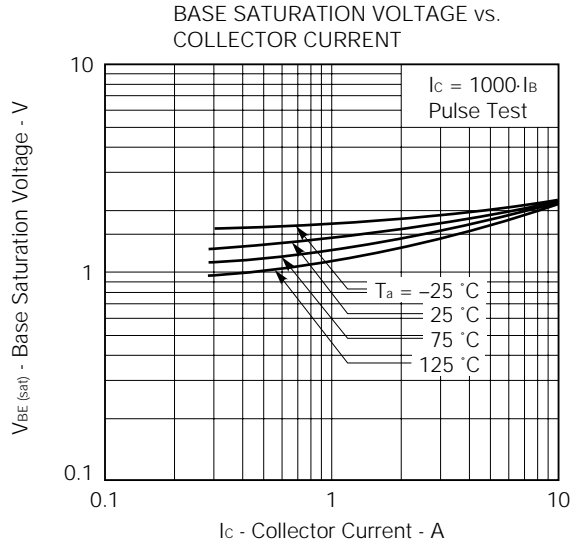
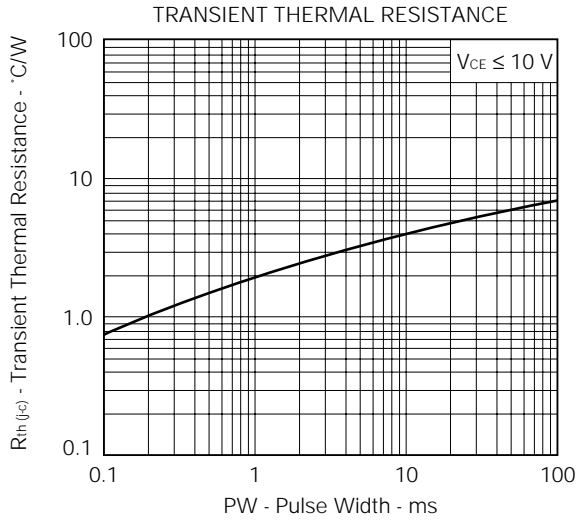


DC CURRENT GAIN vs. COLLECTOR CURRENT



COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT





REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134

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