

## MOS FIELD EFFECT TRANSISTOR $\mu$ PA1708

### SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

### **DESCRIPTION**

This product is N-Channel MOS Field Effect Transistor designed for DC/DC converters and power management switch.

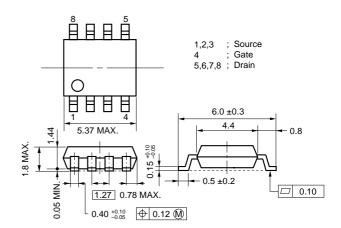
### **FEATURES**

- · Low on-resistance
  - $R_{DS(on)1} = 18.0 \text{ m}\Omega$  (TYP.) (Vgs = 10 V, ID = 3.5 A)  $R_{DS(on)2} = 28.0 \text{ m}\Omega$  (TYP.) (Vgs = 4.5 V, ID = 3.5 A)
- Low Ciss : Ciss = 730 pF (TYP.)
- · Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

### ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1708G	Power SOP8

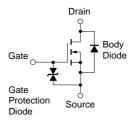
### PACKAGE DRAWINGS (Unit: mm)



### **EQUIVALENT CIRCUIT**

### ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected)

Drain to Source Voltage Note1	VDSS	40	V
Gate to Source Voltage Note2	Vgss	±25	V
Drain Current (DC)	$I_{D(DC)}$	±7.0	Α
Drain Current (pulse) Note3	ID(pulse)	±28	Α
Total Power Dissipation ( $T_A = 25^{\circ}C$ ) Note4	Рт	2.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	$T_{stg}$	-55 to + 150	°C



- Notes 1. Vgs = 0 V
  - 2. VDS = 0 V
  - **3.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1 %
  - 4. Mounted on ceramic substrate of 1200 mm<sup>2</sup> x 1.7mm

**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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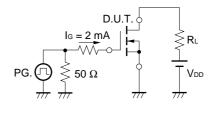
### ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	RDS(on)1	Vgs = 10 V, lb = 3.5 A		18.0	24.0	mΩ
	RDS(on)2	Vgs = 4.5 V, ID = 3.5 A		28.0	40.0	mΩ
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	yfs	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 3.5 A	4.0	8.4		S
Drain Leakage Current	Ipss	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V			10	μΑ
Gate to Source Leakage Current	Igss	Vgs = ±25 V, Vps = 0 V			±10	μΑ
Input Capacitance	Ciss	V <sub>DS</sub> = 10 V		730		pF
Output Capacitance	Coss	V <sub>G</sub> S = 0 V		340		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		150		pF
Turn-on Delay Time	td(on)	ID = 3.5 A		16		ns
Rise Time	tr	$V_{GS(on)} = 10 \text{ V}$		96		ns
Turn-off Delay Time	td(off)	V <sub>DD</sub> = 20 V		49		ns
Fall Time	t <sub>f</sub>	$R_G = 10 \Omega$		30		ns
Total Gate Charge	QG	ID = 7.0 A		20		nC
Gate to Source Charge	Qgs	VDD = 32 V		2.5		nC
Gate to Drain Charge	Q <sub>GD</sub>	Vgs = 10 V		6.8		nC
Body Diode Forward Voltage	V <sub>F</sub> (S-D)	IF = 7.0 A, VGS = 0 V		0.8		V
Reverse Recovery Time	trr	IF = 7.0 A, VGS = 0 V		32		ns
Reverse Recovery Charge	Qır	di/dt = 100 A/ μs		25		nC

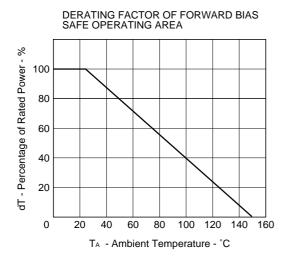
### **TEST CIRCUIT 1 SWITCHING TIME**

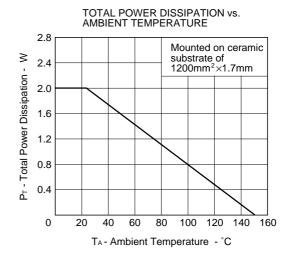
# PG. $\bigcap_{RG} R_G = 10 \ \Omega$ $V_{GS} \bigvee_{Wave Form} V_{DD} \bigvee_{Wave Form} V_{GS} \bigvee_{Wave Form} V_{GS} \bigvee_{Wave Form} V_{GS} \bigvee_{Wave Form} V_{GS} \bigvee_{UD} \bigvee_{Wave Form} V_{GS} \bigvee_{UD} \bigvee_{Wave Form} V_{GS} \bigvee_{UD} \bigvee_{UD} \bigvee_{UD} V_{GS} \bigvee_{UD} \bigvee_{UD} V_{GS} \bigvee_{UD} V_$

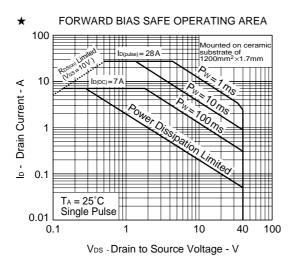
### **TEST CIRCUIT 2 GATE CHARGE**

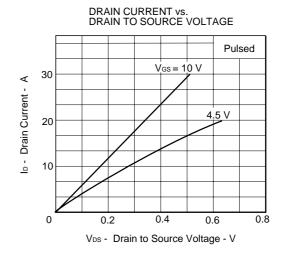


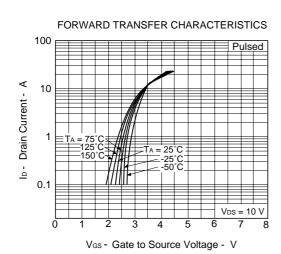
### TYPICAL CHARACTERISTICS (TA = 25 °C)

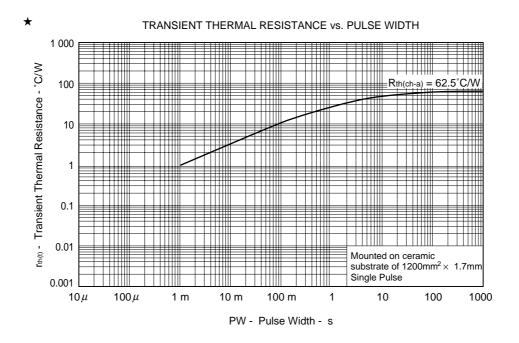




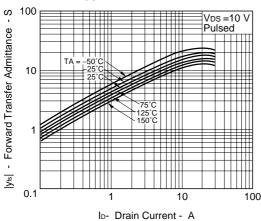




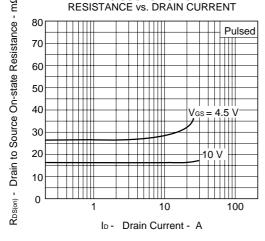




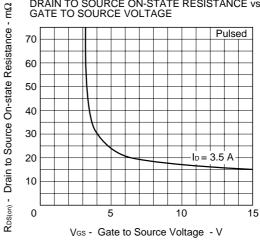


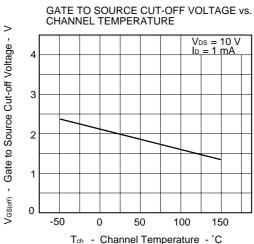


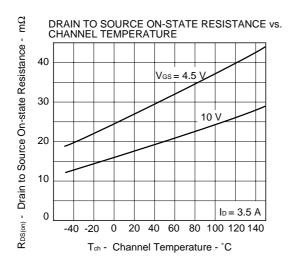
DRAIN TO SOURCE ON-STATE

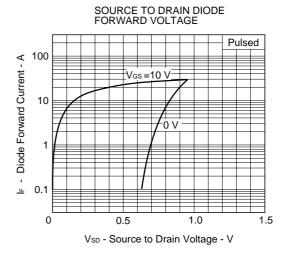


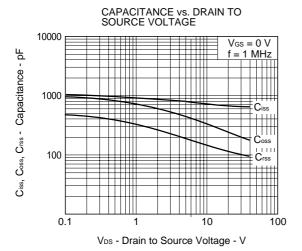
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

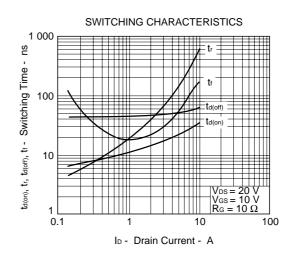


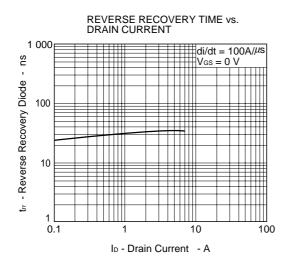


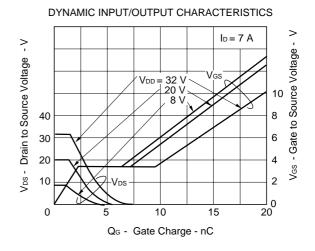












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