

SWITCHING

N-CHANNEL POWER MOS FET

INDUSTRIAL USE

DESCRIPTION

This product is N-Channel MOS Field Effect Transistor designed for DC/DC converters and power management switch.

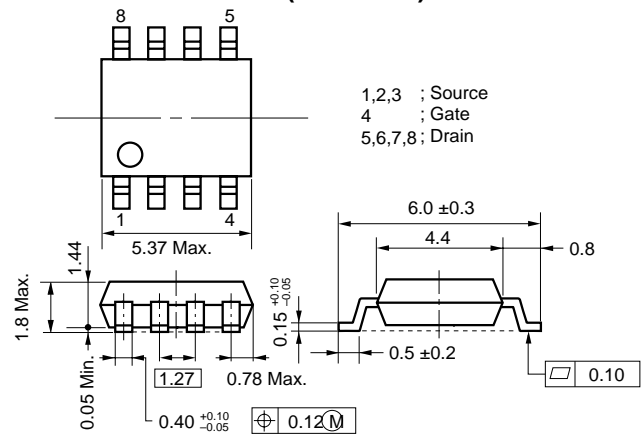
FEATURES

- Low on-resistance
 $R_{DS(on)1} = 9.3 \text{ m}\Omega$ (TYP.) ($V_{GS} = 10 \text{ V}$, $I_D = 4.5 \text{ A}$)
 $R_{DS(on)2} = 13.8 \text{ m}\Omega$ (TYP.) ($V_{GS} = 4.5 \text{ V}$, $I_D = 4.5 \text{ A}$)
- Low C_{iss} : $C_{iss} = 1850 \text{ pF}$ (TYP.)
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1709G	Power SOP8

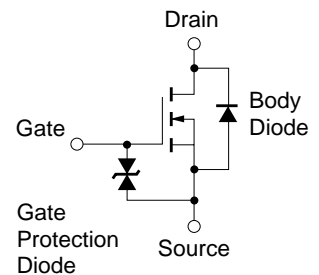
PACKAGE DRAWING (Unit : mm)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, All terminals are connected.)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	40	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 25	V
Drain Current (DC)	$I_{D(DC)}$	± 9.0	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 36	A
Total Power Dissipation ($T_A = 25^\circ\text{C}$) ^{Note2}	P_T	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to + 150	$^\circ\text{C}$

EQUIVALENT CIRCUIT



Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1 \%$

2. Mounted on ceramic substrate of $1200 \text{ mm}^2 \times 0.7 \text{ mm}$

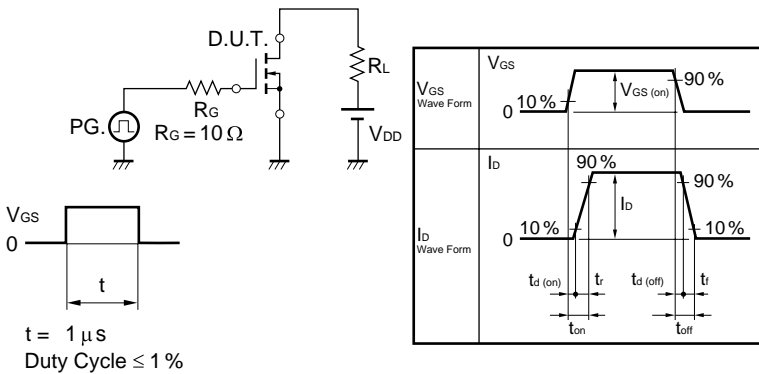
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

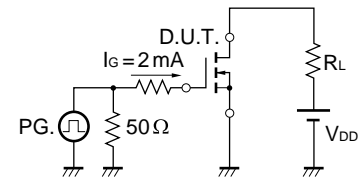
ELECTRICAL CHARACTERISTICS (T_A = 25 °C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 4.5 A		9.3	12.5	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 4.5 A		13.8	20.0	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 4.5 A	8.0	14		S
Drain Leakage Current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±25 V, V _{DS} = 0 V			±10	μA
Input Capacitance	C _{iss}	V _{DS} = 10 V		1850		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		790		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		330		pF
Turn-on Delay Time	t _{d(on)}	I _D = 4.5 A		27		ns
Rise Time	t _r	V _{GS(on)} = 10 V		95		ns
Turn-off Delay Time	t _{d(off)}	V _{DD} = 20 V		110		ns
Fall Time	t _f	R _G = 10 Ω		70		ns
Total Gate Charge	Q _G	I _D = 9.0 A		43.0		nC
Gate to Source Charge	Q _{GS}	V _{DD} = 32 V		6.0		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = 10 V		14.0		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 9.0 A, V _{GS} = 0 V		0.78		V
Reverse Recovery Time	t _{rr}	I _F = 9.0 A, V _{GS} = 0 V		47		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		44		nC

TEST CIRCUIT 1 SWITCHING TIME

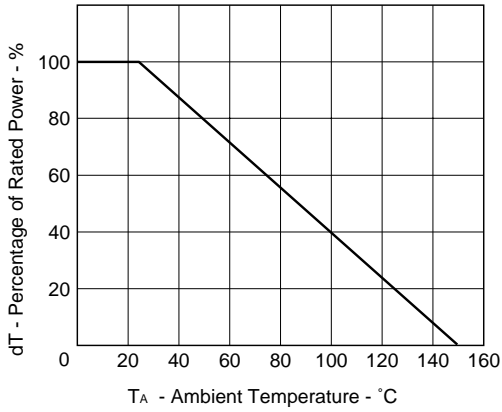


TEST CIRCUIT 2 GATE CHARGE

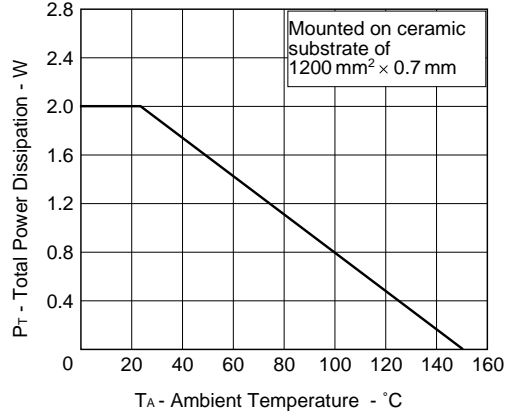


TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

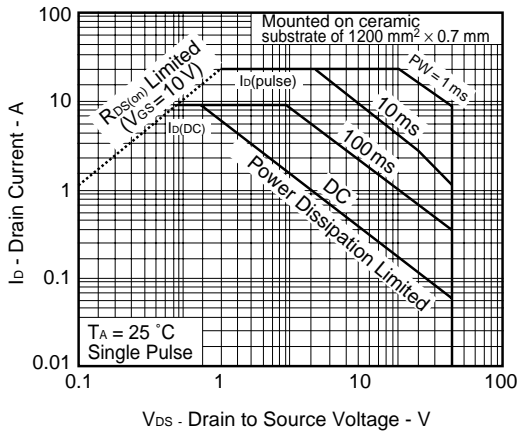


TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE

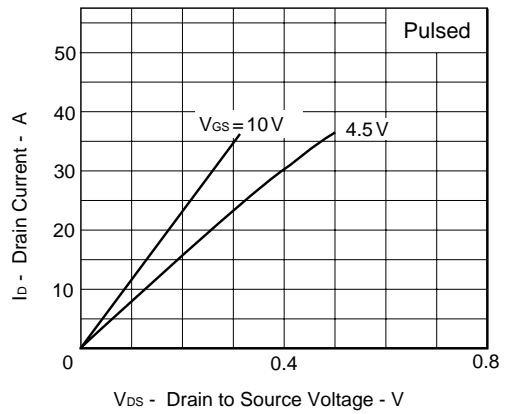


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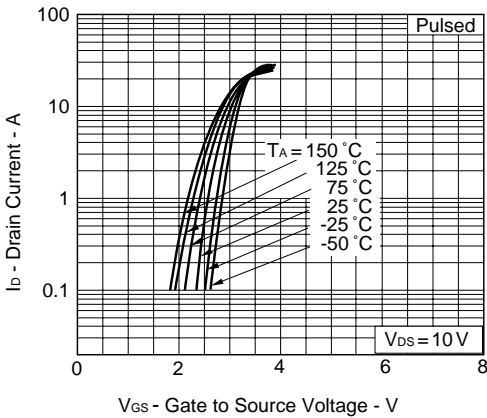
FORWARD BIAS SAFE OPERATING AREA



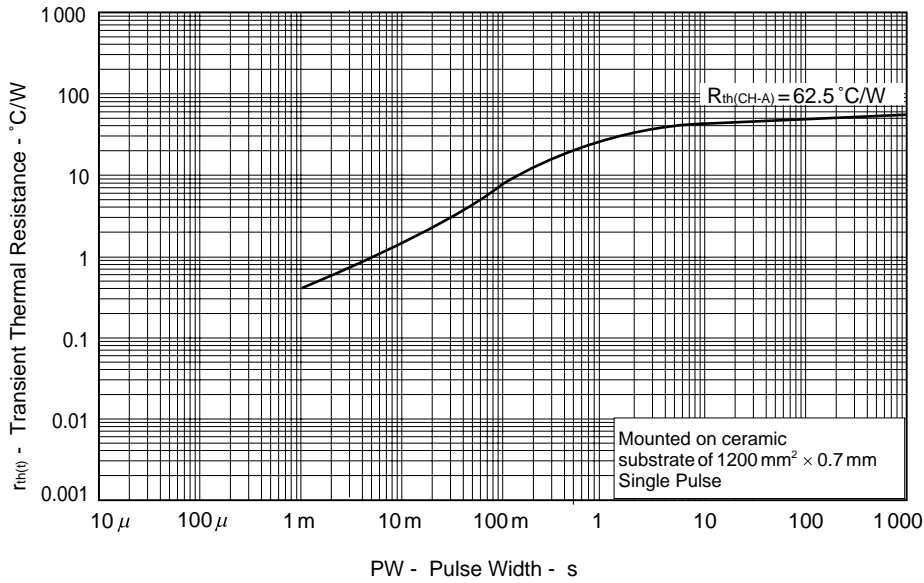
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



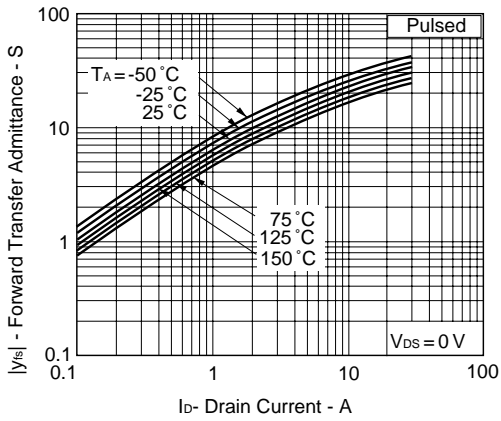
FORWARD TRANSFER CHARACTERISTICS



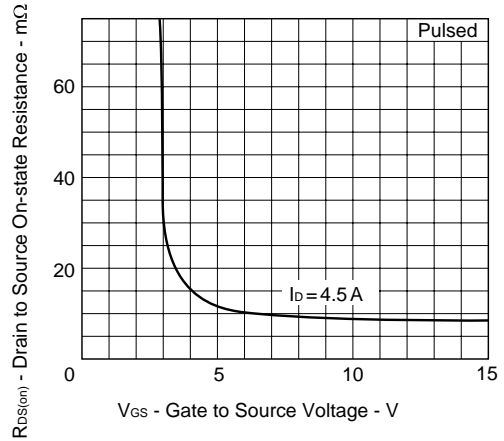
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



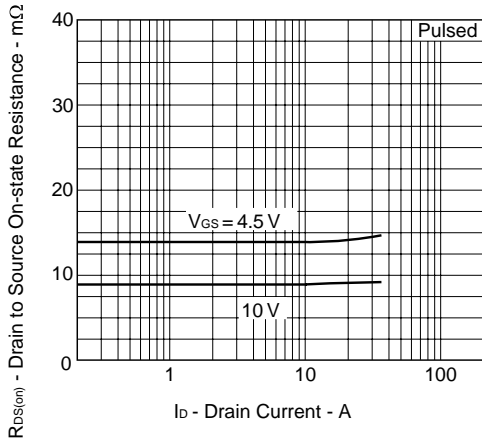
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



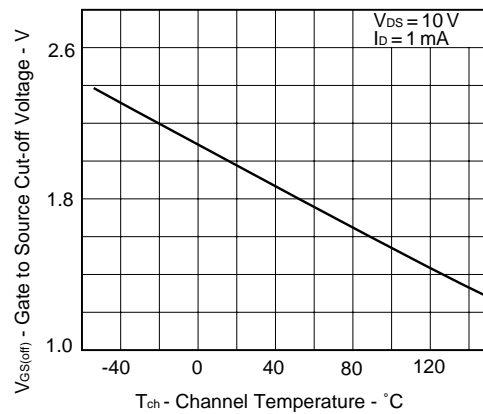
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

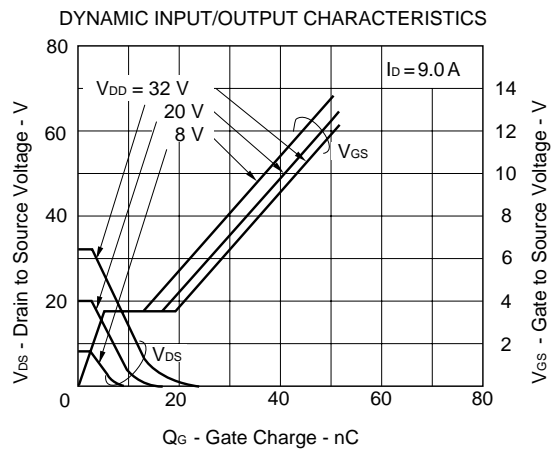
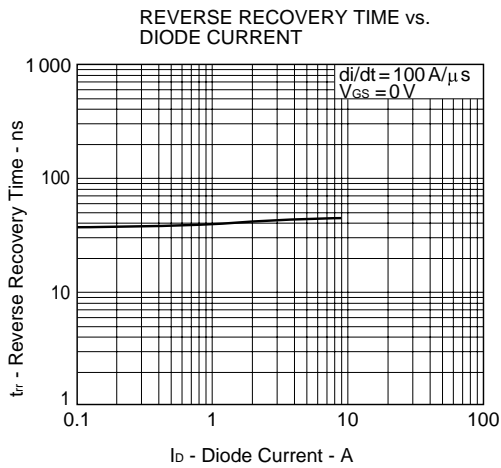
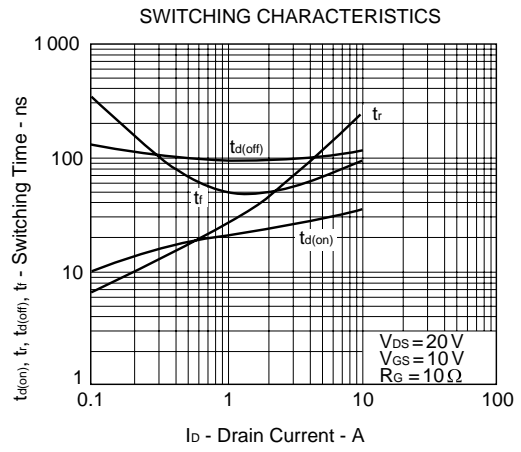
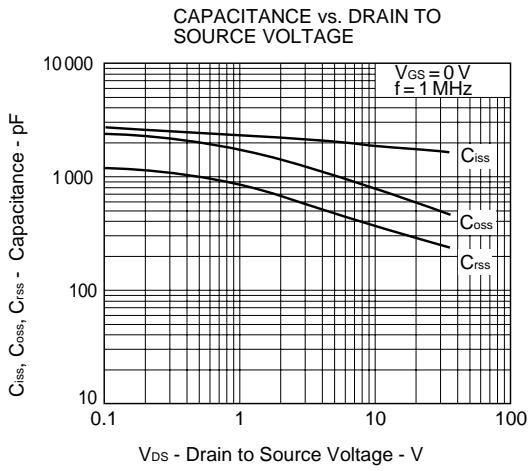
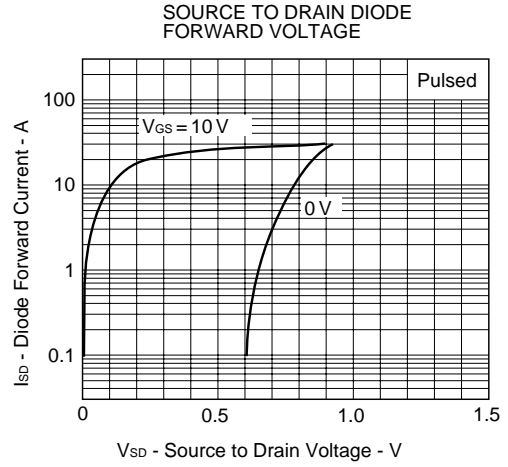
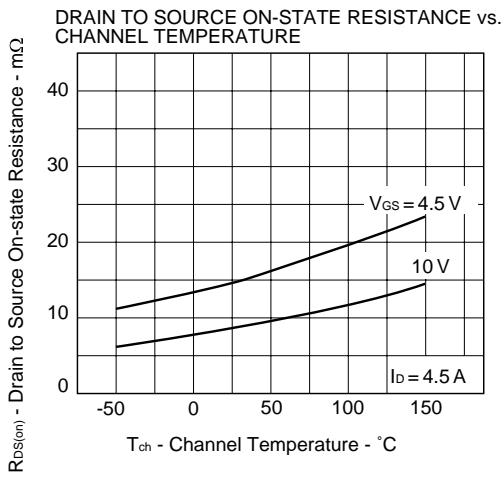


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE





[MEMO]

[MEMO]

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