

MOS FIELD EFFECT TRANSISTOR μ PA1758

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

This product is Dual N-Channel MOS Field Effect Transistor designed for power management application of notebook computers, and Li-ion battery application.

FEATURES

- Dual MOS FET chips in small package
- 2.5 V gate drive type low on-state resistance $R_{DS(on)1} = 30 \text{ m}\Omega \text{ (MAX.)} \text{ (Vgs} = 4.5 \text{ V, I}_D = 3.0 \text{ A)}$ $R_{DS(on)2} = 40 \text{ m}\Omega \text{ (MAX.)} \text{ (Vgs} = 2.5 \text{ V, I}_D = 3.0 \text{ A)}$
- Low C_{iss} : C_{iss} = 1100 pF (TYP.)
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

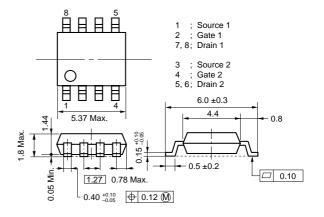
ORDERING INFORMATION

PART NUMBER	PACKAGE
μΡΑ1758G	Power SOP8

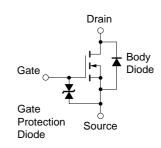
ABSOLUTE MAXIMUM RATINGS (TA = 25 °C)

Drain to Source Voltage (Vgs = 0)	Vdss	30	
Gate to Source Voltage ($V_{DS} = 0$)	Vgss	±12.0	
Drain Current (DC)	D(DC)	±6.0	
Drain Current (Pulse) Note1	D(pulse)	±24	
Total Power Dissipation (1 unit) Note2	Ρτ	1.7	
Total Power Dissipation (2 unit) Note2	Ρτ	2.0	
Channel Temperature	Tch	150	
Storage Temperature	Tstg	–55 to + 150	

PACKAGE DRAWING (Unit : mm)



EQUIVALENT CIRCUIT



Notes 1. PW \leq 10 μ s, Duty cycle \leq 1 %

- 2. Mounted on ceramic substrate of 2000 mm² x 1.1 mm
- **Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

v v

Α

А

w w

°С

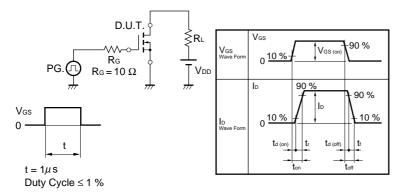
°C

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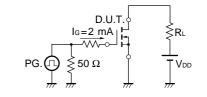
ELECTRICAL CHARACTERISTICS (TA = 25 °C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	RDS(on)1	Vgs = 4.5 V, Id = 3.5 A		20	30	mΩ
	RDS(on)2	Vgs = 2.5 V, Id = 3.5 A		25	40	mΩ
Gate to Source Cutoff Voltage	VGS(off)	V _{DS} = 10 V, I _D = 1.0 mA	0.5	0.8	1.5	V
Forward Transfer Admittance	y fs	VDS = 10 V, ID = 3.5 A	5.0	13		S
Drain Leakage Current	ldss	Vds = 30 V, Vgs = 0			10	μA
Gate to Source Leakage Current	lgss	$V_{GS} = \pm 12.0 \text{ V}, \text{ V}_{DS} = 0$			±10	μA
Input Capacitance	Ciss	V _{DS} = 10 V, V _{GS} = 0, f = 1 MHz		1100		pF
Output Capacitance	Coss			370		pF
Reverse Transfer Capacitance	Crss			170		pF
Turn-on Delay Time	td(on)	$I_D = 3.0 \text{ A}, V_{GS(on)} = 4.0 \text{ V}, V_{DD} = 15 \text{ V}$		50		ns
Rise Time	tr	R _G = 10 Ω		190		ns
Turn-off Delay Time	td(off)			550		ns
Fall Time	tr			490		ns
Total Gate Charge	QG	ID = 6.0 A, VDD = 24 V, VGS = 4.0 V		15.0		nC
Gate to Source Charge	QGS]		2.0		nC
Gate to Drain Charge	Qgd			6.5		nC
Body Diode forward Voltage	VF(S-D)	IF = 6.0 A, VGS = 0		0.8		V

TEST CIRCUIT 1 SWITCHING TIME

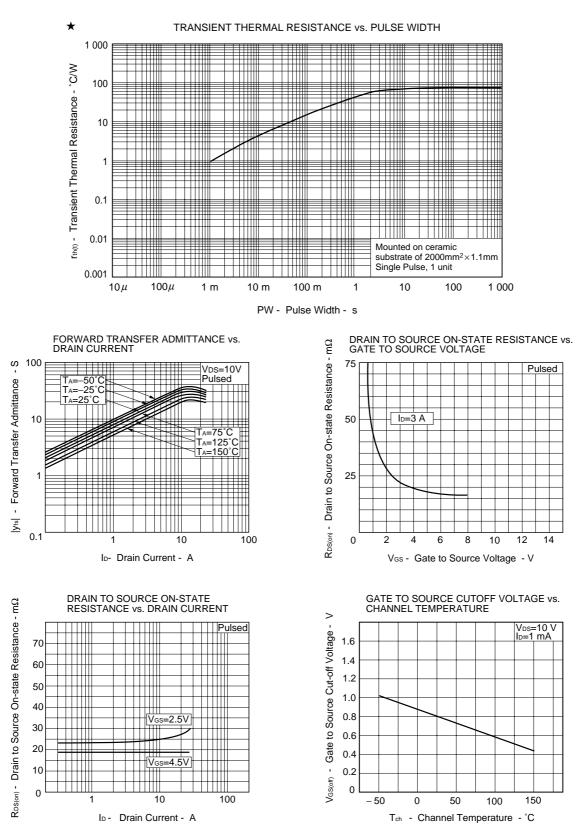


TEST CIRCUIT 2 GATE CHARGE

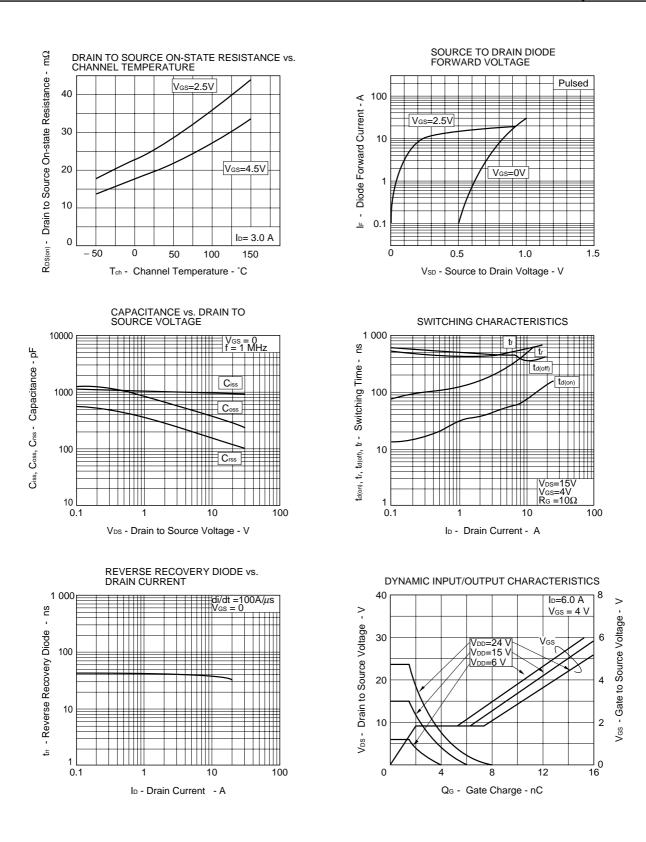


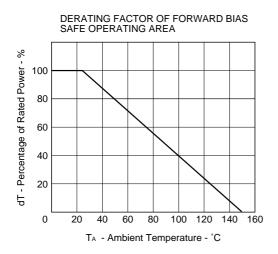
TYPICAL CHARACTERISTICS (TA = 25 °C)

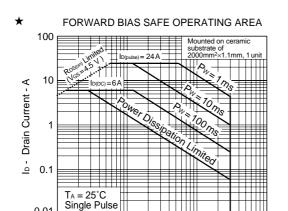
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VDS - Drain to Source Voltage - V

10

30

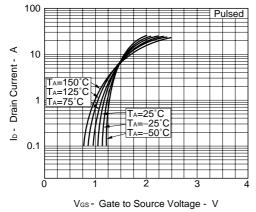
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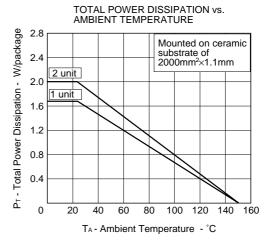
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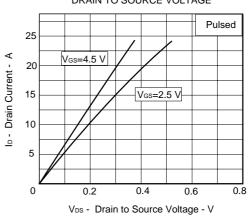
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