### DATA SHEET

## MOS FIELD EFFECT TRANSISTOR

# μ**PA2781GR**

#### SWITCHING N-CHANNEL POWER MOS FET/SCHOTTKY BARRIER DIODE

#### DESCRIPTION

The  $\mu$ PA2781GR is N-channel Power MOSFET, which built a Schottky Barrier Diode inside.

This product is designed for synchronous DC/DC converter application.

#### FEATURES

- Built a Schottky Barrier Diode
- Low on-state resistance

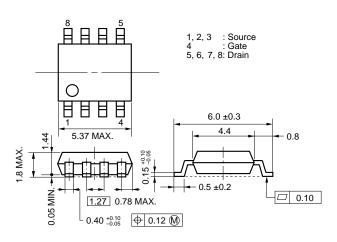
 $R_{DS(on)1} = 7.6 \text{ m}\Omega \text{ TYP.} (V_{GS} = 10 \text{ V}, \text{ ID} = 7 \text{ A})$ 

- $R_{DS(on)2} = 11.3 \text{ m}\Omega \text{ TYP.} (V_{GS} = 4.5 \text{ V}, \text{ ID} = 7 \text{ A})$
- $R_{DS(on)3} = 12.9 \text{ m}\Omega \text{ TYP.} (V_{GS} = 4.0 \text{ V}, \text{ ID} = 7 \text{ A})$
- Low Ciss: Ciss = 900 pF TYP.
- Small and surface mount package (Power SOP8)

#### ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA2781GR	Power SOP8

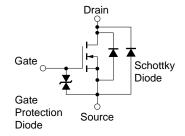
#### PACKAGE DRAWING (Unit: mm)



#### EQUIVALENT CIRCUIT

#### ABSOLUTE MAXIMUM RATINGS (TA = 25°C. All terminals are connected.)

Drain to Source Voltage (Vgs = 0 V)	Vdss	30	V
Gate to Source Voltage (Vps = 0 V)	Vgss	±20	V
Drain Current (DC) [MOSFET]	D(DC)	±13	А
Drain Current (pulse) <sup>Note1</sup>	D(pulse)	±52	А
Average Forward Current <sup>Note2</sup> [SCHOTTKY]	F(AV)	2.5	А
Total Power Dissipation Note3 [MOSFET]	Рт	2	W
Total Power Dissipation Note3 [SCHOTTKY]	Рт	1	W
Channel & Junction Temperature	Tch, Tj	150	°C
Storage Temperature	Tstg	–55 to + 150	°C
Notes 1 $DM < 10$ up $Duty Cycle < 10/$			



**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

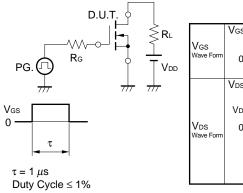
- 2. Rectangle wave, 50% Duty Cycle
- 3. Mounted on ceramic substrate of 1200 mm<sup>2</sup> x 2.2 mm
- **Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

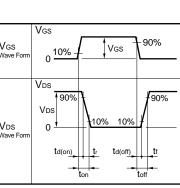
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	LECTRICAL CHARACTERISTICS (TA = 25 C, unless otherwise noted. All terminals are connected.)						
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Zero Gate Voltage Drain Current Note	IDSS	VDS = 24 V, VGS = 0 V			50	μA	
		VDS = 24 V, VGS = 0 V, TA = 125°C			10	mA	
Gate Leakage Current	lgss	$V_{GS} = \pm 20 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$			±10	μA	
Gate Cut-off Voltage	V <sub>GS(off)</sub>	Vbs = 10 V, Ib = 1 mA	1.0		2.5	V	
Drain to Source On-state Resistance Note	RDS(on)1	Vgs = 10 V, Id = 7 A		7.6	9.5	mΩ	
	RDS(on)2	Vgs = 4.5 V, Id = 7 A		11.3	15.1	mΩ	
	RDS(on)3	Vgs = 4.0 V, Id = 7 A		12.9	17.2	mΩ	
Input Capacitance	Ciss	V <sub>DS</sub> = 10 V		900		pF	
Output Capacitance	Coss	Vgs = 0 V		450		pF	
Reverse Transfer Capacitance	Crss	f = 1 MHz		120		pF	
Turn-on Delay Time	td(on)	Vdd = 15 V, Id = 7 A		9		ns	
Rise Time	tr	V <sub>G</sub> s = 10 V		5		ns	
Turn-off Delay Time	td(off)	R <sub>G</sub> = 10 Ω		35		ns	
Fall Time	tr			8		ns	
Total Gate Charge	QG	Vdd = 15 V		9		nC	
Gate to Source Charge	QGS	V <sub>GS</sub> = 5 V		3		nC	
Gate to Drain Charge	Qgd	ID = 13 A		4		nC	
Body Diode Forward Voltage Note	VF(S-D)	IF = 1 A, VGS = 0 V		0.45	0.5	V	
		IF = 1 A, VGS = 0 V, TA = 125°C		0.37		V	
Reverse Recovery Time	trr	IF = 7 A, VGS = 0 V		28		ns	
Reverse Recovery Charge	Qrr	di/dt = 100 A/µs		18		nC	

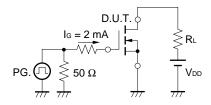
**Note** Pulsed: PW  $\leq$  350  $\mu$ s, Duty Cycle  $\leq$  2%

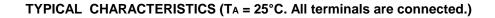
#### **TEST CIRCUIT 1 SWITCHING TIME**

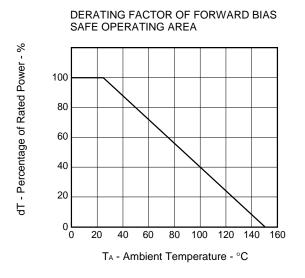




#### TEST CIRCUIT 2 GATE CHARGE

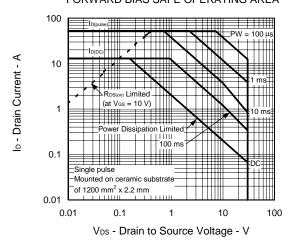


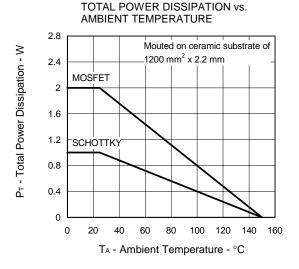




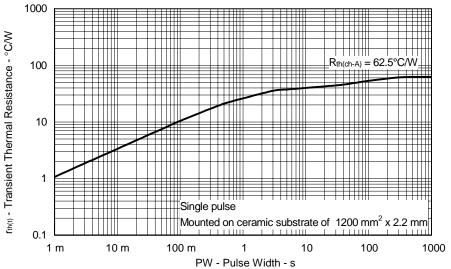
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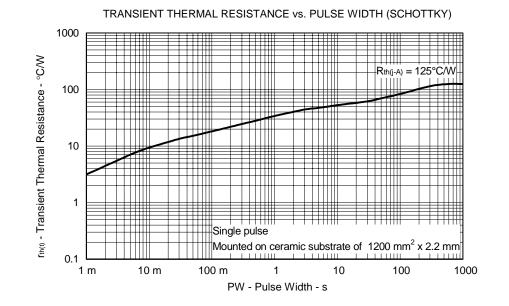




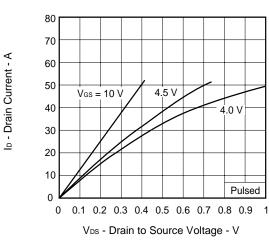


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH (MOSFET)

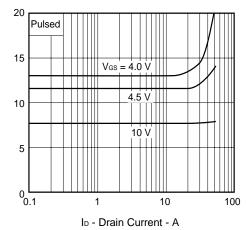




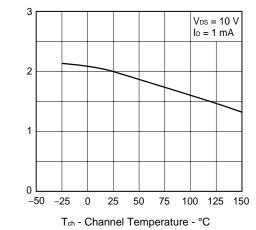
#### DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



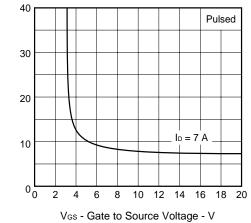
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



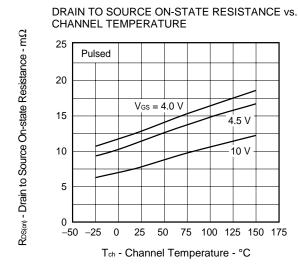
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



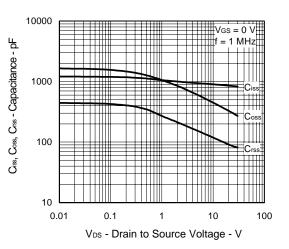
Rtss(or) - Drain to Source On-state Resistance - m0 0 0 0 0

Vgs(off) - Gate Cut-off Voltage - V

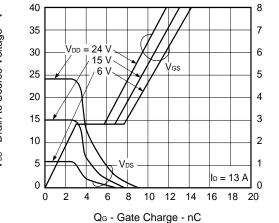
 $R_{\text{DS}(m)}$  - Drain to Source On-state Resistance -  $m\Omega$ 



CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

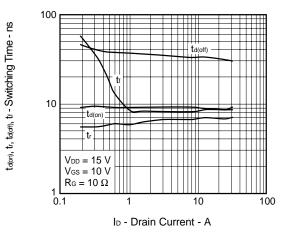


DYNAMIC INPUT/OUTPUT CHARACTERISTICS

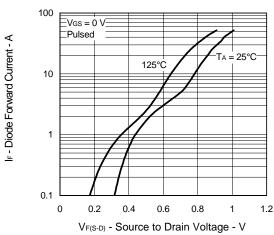


Vps - Drain to Source Voltage - V

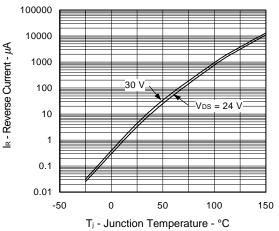
SWITCHING CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



SOURCE TO DRAIN DIODE REVERSE CURRENT



V<sub>GS</sub> - Gate to Source Voltage - V

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