NEC

MOS INTEGRATED CIRCUIT

μPD16430A

1/2, 1/3, 1/4 DUTY LCD CONTROLLER/DRIVER

The μPD16430A is an LCD controller/driver that enables the display of LCDs of 1/2 duty, 1/3 duty and 1/4 duty cycle.

The LCD controller contained in the μPD16430A employs serial data transfer and uses an automatic increment function for data addresses which eliminates the need to set addresses newly each time.

The LCD driver uses a medium voltage output (14 V max.), which enables higher contrast and a wider viewing angle even with a 1/3 or 1/4 duty cycle.

By using an on-chip drive bias circuit, it is possible to eliminate the need for external resistors.

FEATURES

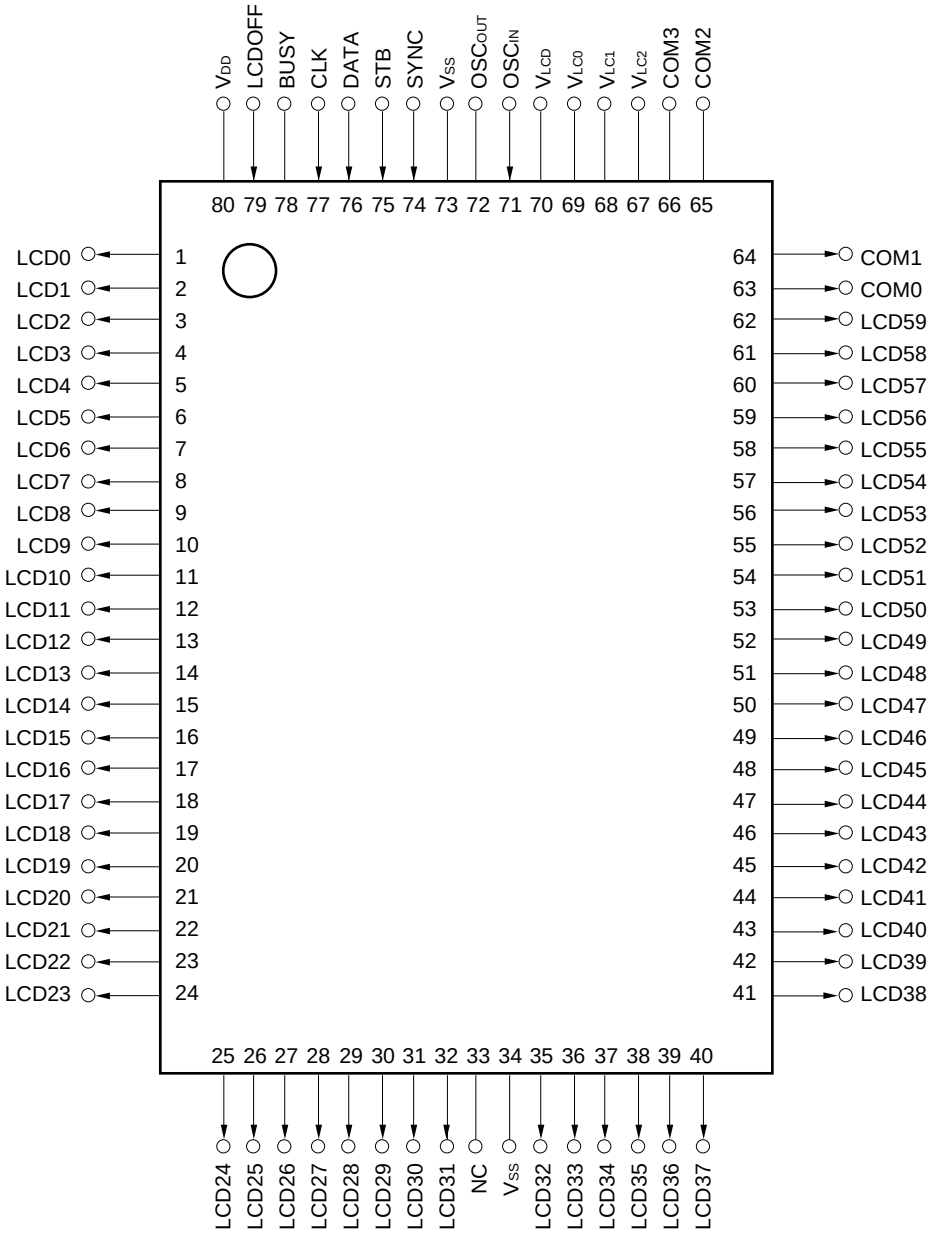
- LCD direct drive (medium voltage output: 14 V MAX.)
- Choice of 3 duty cycles
  - 1/2 duty, 1/3 duty, 1/4 duty
- Display dot number:
  - 1/2 duty: 120
  - 1/3 duty: 160
  - 1/4 duty: 240
- 2 types of drive bias
  - 1/2 bias, 1/3 bias
- Choice of 4 types of frame frequency
- Multi-chip configuration possible
- Control through 8-bit serial interface
- On-chip power-on reset circuit
- Low-power dissipation CMOS
- 3.5 to 6.0 V logic supply voltage

ORDERING INFORMATION

Part number	Package
μPD16430AGF-3B9	80-pin plastic QFP (14 × 20)

Document No. IC-2776 (1st edition)
(O.D. No. IC-8302)
Date Published March 1997 N
Printed in Japan

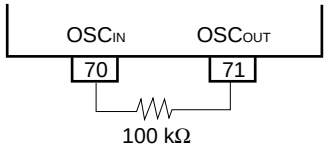
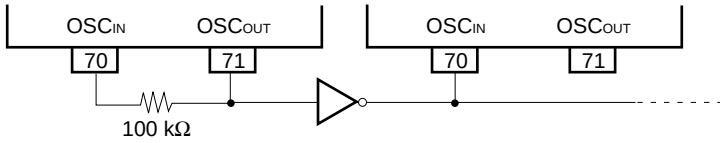
PIN CONFIGURATION (Top View)



Remark Be sure to leave Pin 33 open since it is connected to the lead frame.

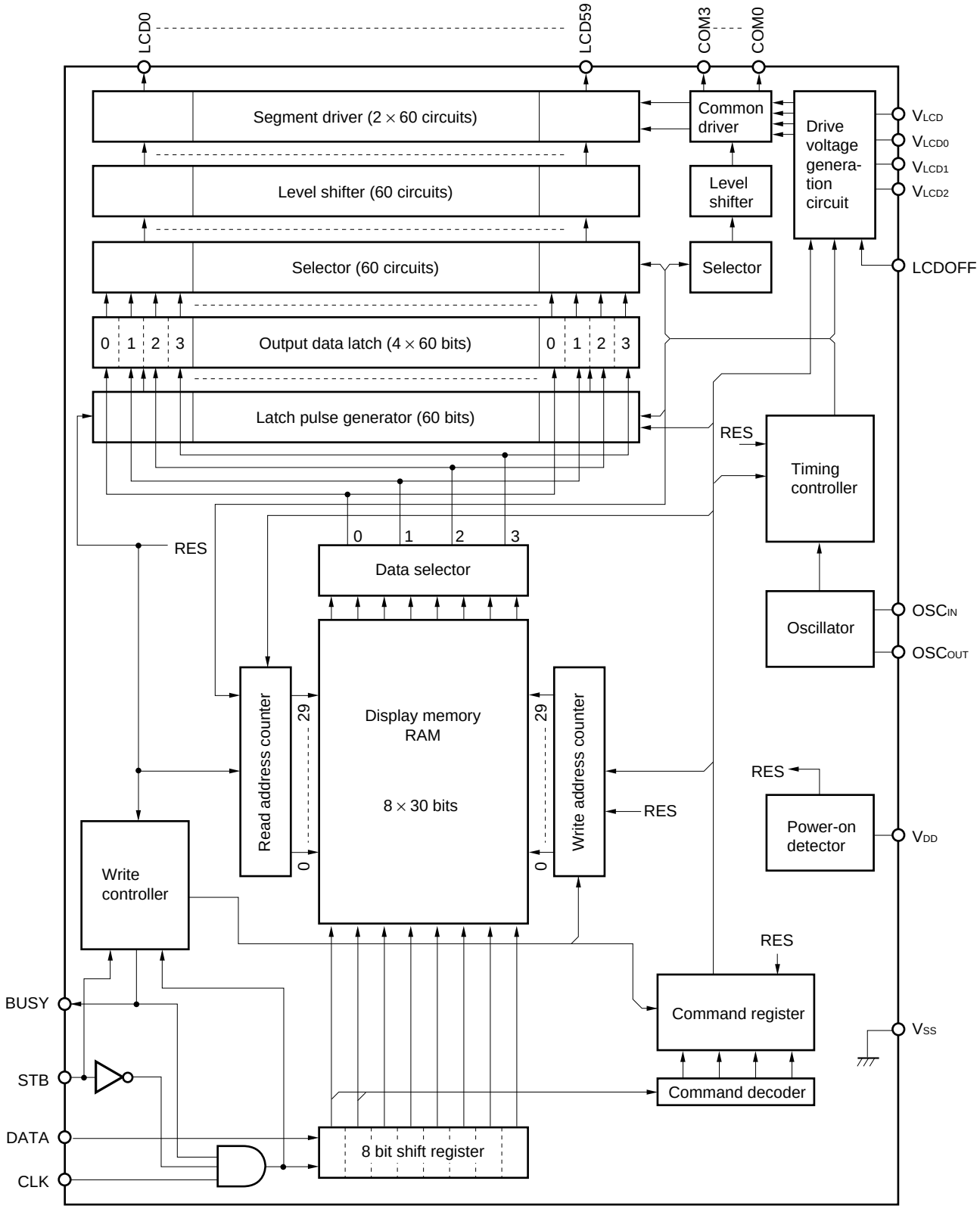
PIN FUNCTIONS

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Output Type</th><th>Description</th></tr>
<tr><td>1
to
32
35
to
62</td><td>LCD0
to
LCD31
LCD32
to
LCD59</td><td>Output</td><td>CMOS</td><td>These pins serve as the LCD driver's segment signal output pins.
The following display modes can be selected for the LCD driver.
<table>
<tr><th>Duty</th><th>Bias</th><th>Display Dot No.</th><th>Frame frequency (Hz) (fosc = 140 kHz)</th></tr>
<tr><td>1/2</td><td>1/2</td><td>120</td><td>$\frac{fosc}{256}$ (547), $\frac{fosc}{512}$ (273), $\frac{fosc}{1024}$ (137), $\frac{fosc}{2048}$ (68)</td></tr>
<tr><td>1/3</td><td>1/3</td><td>160</td><td>$\frac{fosc}{384}$ (365), $\frac{fosc}{768}$ (182), $\frac{fosc}{1536}$ (91), $\frac{fosc}{3072}$ (46)</td></tr>
<tr><td>1/4</td><td>1/3</td><td>240</td><td>$\frac{fosc}{512}$ (273), $\frac{fosc}{1024}$ (137), $\frac{fosc}{2048}$ (68), $\frac{fosc}{4096}$ (34)</td></tr>
</table>
A matrix of these segment signal output pins and COM3, COM2, COM1 and COM0 pins enables the maximum display of 240 dots (1/4 duty selected).
The output voltage of the segment signal output pins is supplied by the V_{LCD} pin.
The output voltage of the segment signal output pin is supplied by dividing and outputting 0 to V_{LCD} voltage using any driving method (any bias method).
Either internal or external voltage dividing resistor can be selected.</td></tr>
<tr><td>63
to
66</td><td>COM0
to
COM3</td><td>Output</td><td>CMOS</td><td>These pins serve as the LCD driver's common signal output pins.
The LCD driver can select three display modes.
A matrix of these common signal output pins and LCD59 through LCD0 pins enables the maximum display of 240 dots (1/4 duty selected).
The output voltage of the common signal output pins is supplied by the V_{LCD} pin.
V_{DD} to 14 V voltage is supplied by this pin.
The output voltage of the common signal output pins is supplied by dividing and outputting 0 to V_{LCD} voltage using any driving method (any bias method).
Either internal or external dividing resistor can be selected.</td></tr>
<tr><td>67
68
69</td><td>V_{LC2}
V_{LC1}
V_{LC0}</td><td>—</td><td>—</td><td>These pins serve as the LCD driver's drive voltage generation pins.
The drive voltage can be set by using either these pins or the on-chip drive voltage generation circuit, as specified by command data.</td></tr>
<tr><td>70</td><td>V_{LCD}</td><td>—</td><td>—</td><td>This pin supplies the LCD driver's supply voltage.
V_{DD} to 14 V voltage is supplied to this pin.
The output voltage of the segment signal and command signal output pins is supplied by dividing and outputting the voltage applied to these pins using any driving method (any bias method).
Do not supply a voltage exceeding V_{DD} to the V_{LCD} pin before the device's supply voltage reaches 3.5 V, as this may cause incorrect display.</td></tr>
</table>

No.	Symbol	I/O	Output Type	Description
71 72	OSC_{IN} OSC_{OUT}	I/O	CMOS	These pins serve to connect the resistors of the system clock RC oscillator.  When several devices are used, connect as follows: 
34 73	V_{SS}	—	—	GND pin for device.
74	SYNC	I/O	Nch Open drain	Synchronous signal I/O pin. This pin is used to synchronize two or more μPD16430A's. At this time, each chip must be wire-ORed and a pull-up resistor (5 k to 10 kΩ) is required. This pin must be pulled up even when only one μPD16430A is used.
75	STB	Input	—	Strobe signal input pin for device's select signal and serial communications. This pin serves to latch display RAM data outputs, set the command data receive mode and initialize serial communications. Serial communication is enabled when this signal is a logic low. When this pin is a logic high, shift clocks that are input are ignored. (1) Display RAM data output buffer latch function The internal display RAM data output is latched to the output latch circuit at the rising edge of the STB signal when the BUSY pin outputs a logic high. However, latch timing depends on the LATCH MD and LATCH flags. The latch time is 504.5/f_{OSC}. When the BUSY signal is a logic low, latching can cause incorrect display. (2) Command data receive mode setting The command data receive mode is set by the rising edge of the STB signal when the BUSY pin outputs a logic high. Once the command data receive mode is set, the initial byte (8 bits) is processed as a command. The command data processing time is approximately 300 ns. The BUSY signal does not change during this time. (3) Serial communication is initialized by the rising edge or the falling edge of the STB signal when the BUSY pin outputs a logic low. Once serial communication is initialized, the command data receive mode is started. During command data decoding or display data RAM interrupt, the STB signal interrupts processing and initializes serial communications. At this time, all displays are turned off (LCDON flag is reset).
76	DATA	Input	—	This pin inputs serial data for serial communication at the rising edge of the shift clock.
77	CLK	Input	—	This pin inputs a shift clock for serial communication. The signal is output at the rising edge of the shift clock signal.

No.	Symbol	I/O	Output Type	Description
78	BUSY	Output	Nch Open drain	This pin outputs the serial communication status and the internal data processing status. When this signal is a logic high, serial communication is executed. When this signal is a logic low, it indicates that the display RAM data is latched to the output buffer. When the power-on reset circuit is operating, this pin holds a logic low until a rising or falling signal is input to the STB pin.
79	LCDOFF	Input	—	This pin serves to turn off all the LCD displays. When a logic low is input to this pin, all LCD displays are turned off. Display RAM data is maintained. Since displays are turned off only by the output driver, serial communications can be executed as usual. To turn on displays, it is necessary to input a logic high to this pin and reset the LCDON flag.
80	V_{DD}	—	—	This pin is a power supply pin to the device. A voltage of 3.5 to 6.0 V is supplied to this pin. When the supply voltage rises from 0 V to 3 V, or when it reaches a value under 3 V and then rises again, the power-on reset circuit starts operating and the device is set to its initialized state. When the device is in its initialized state, all displays are turned off (segment and common signals are fixed to V_{LCD}). Do not supply a voltage higher than V_{DD} to the V_{LCD} pin before the supply voltage reaches 3.5 V as this will cause incorrect display.

BLOCK DIAGRAM



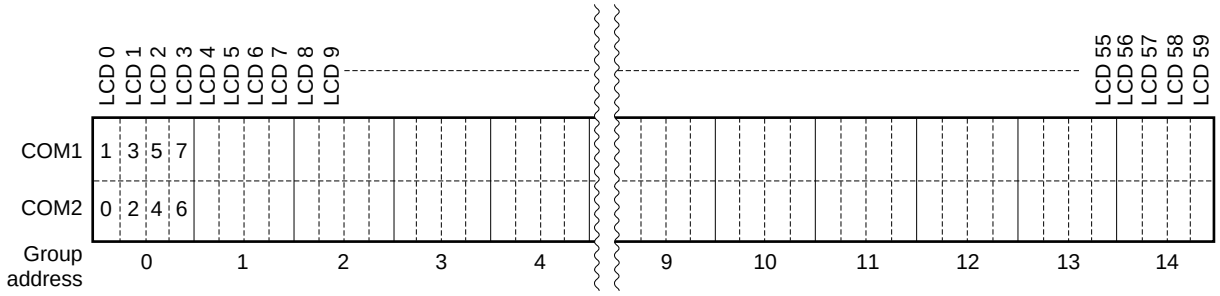
Display RAM Addresses and Display Dots

Display RAM temporarily stores display data that has been sent serially.

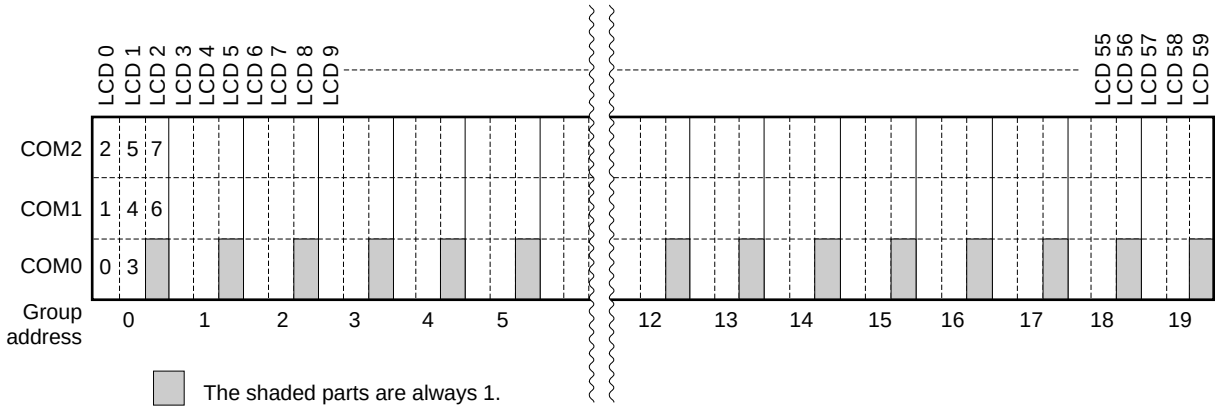
Display RAM addresses are allocated in units of 8 bits (group address), and it is possible to store the display data of a group address transferred at one time.

The relations between group addresses and display dots for the three display modes are shown below.

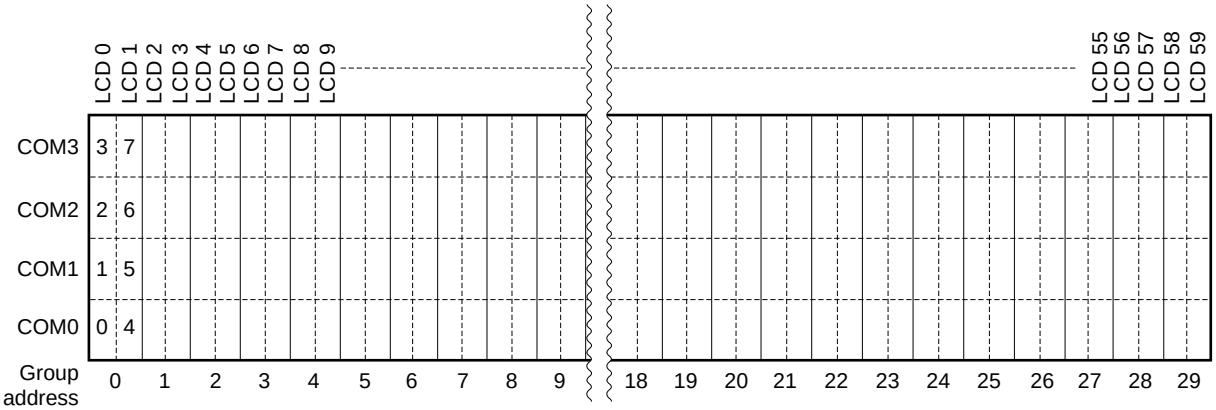
(1) 1/2 duty



(2) 1/3 duty



(3) 1/4 duty



Remark During auto incrementing, incrementing past the last group address of each duty (for example group address 14 in the case of 1/2 duty) brings the counter back to "0."

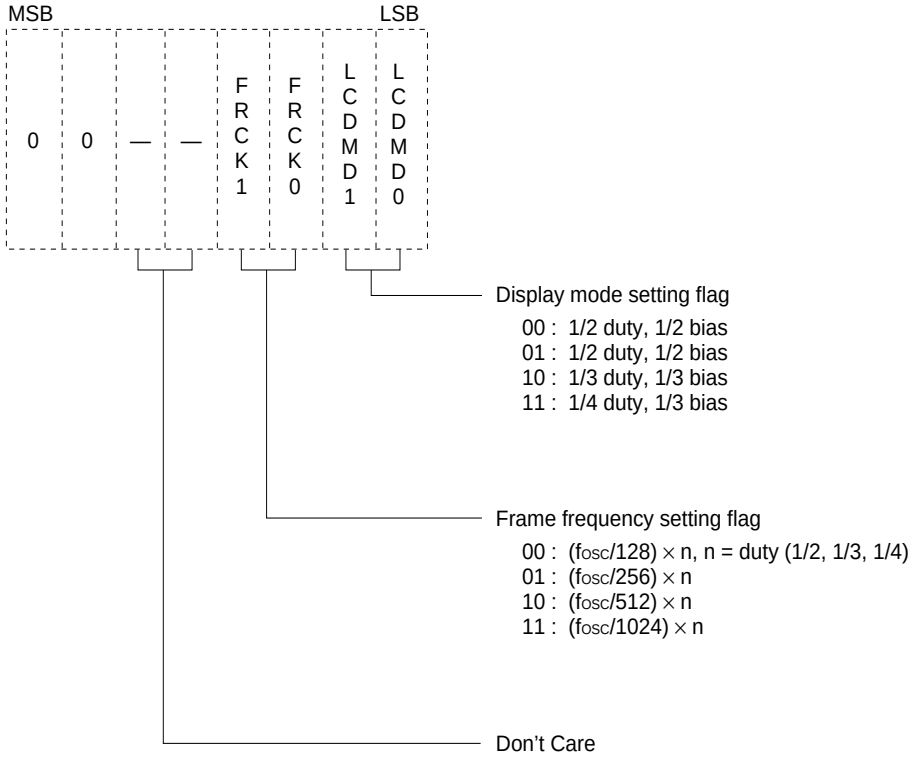
Commands

Commands serve to set the LCD driver's display mode and status.

The first byte (8 bits) after the falling edge input of the STB signal is processed as a command.

The various types of commands are shown below.

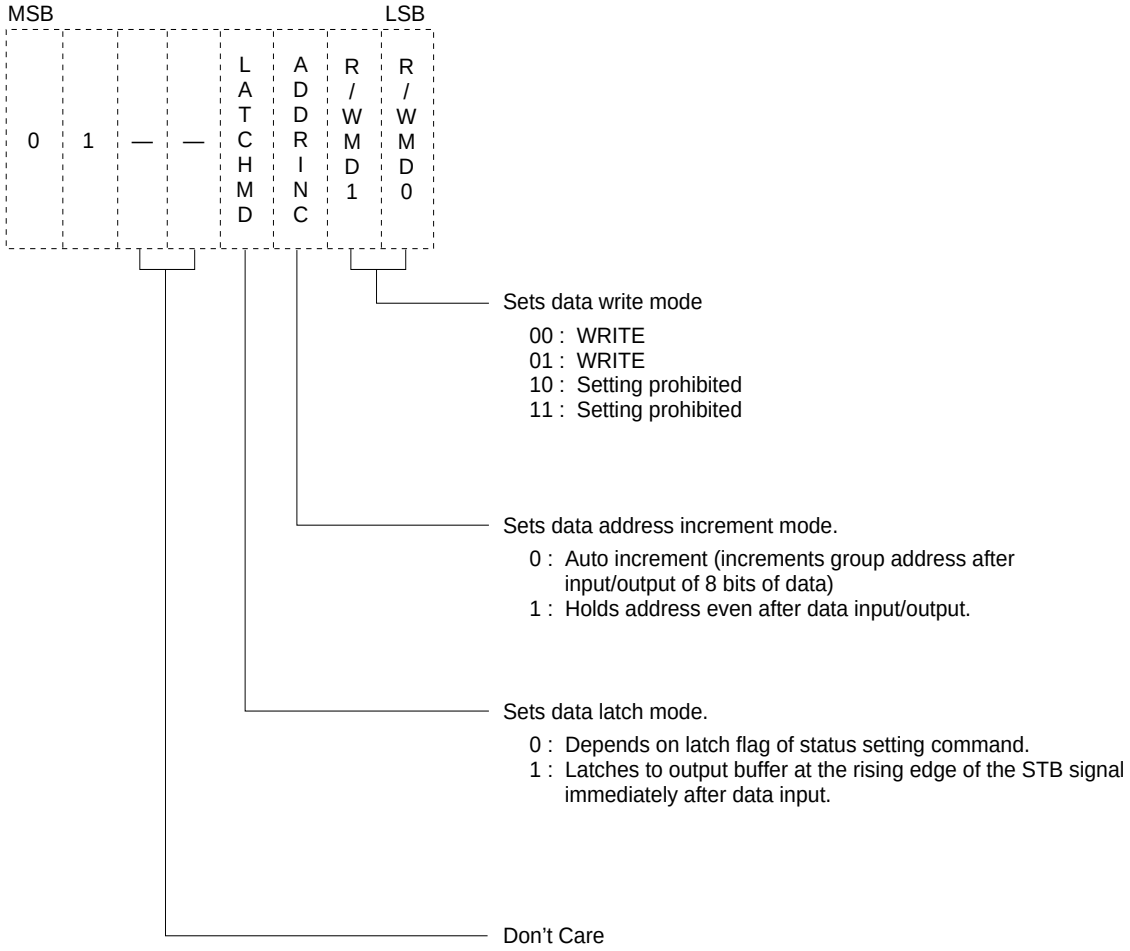
(1) Display Mode Setting Command



Values at power-on reset

		—	—	—	—	—	—

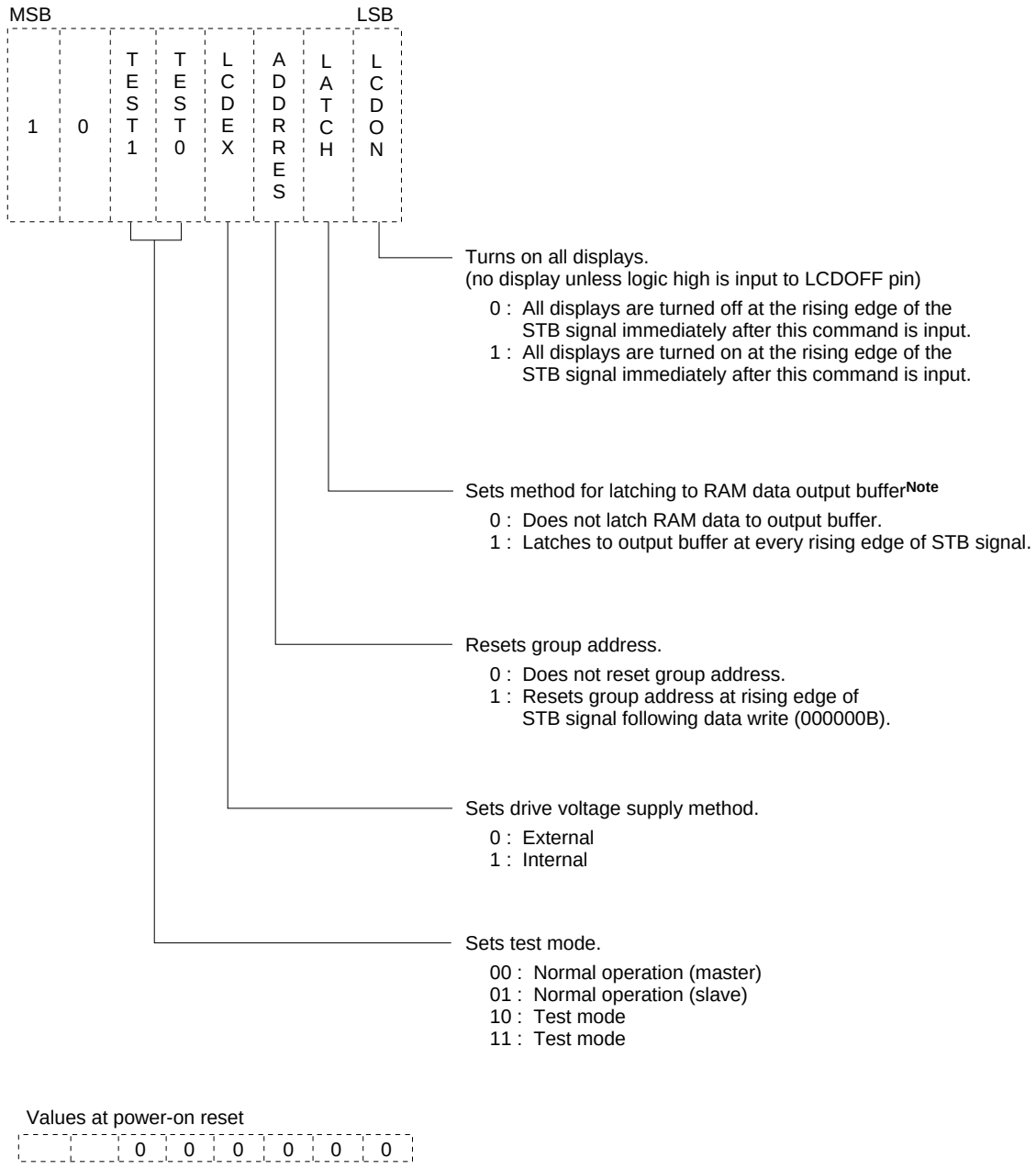
(2) Data Setting Command



Values at power-on reset

		—	—	0	0	0	0

(3) Status setting command



Values at power-on reset

		0	0	0	0	0	0

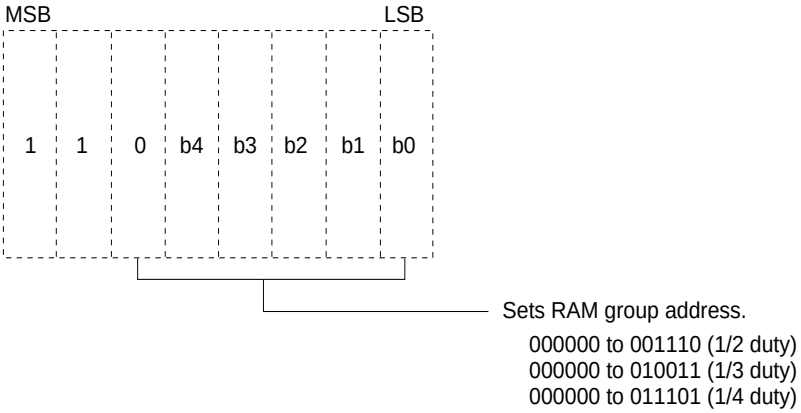
Remark LATCH MD flag and LATCH flag

The relations between the LATCH MD flag and the LATCH flag are shown below.

Mode	LATCH MD	LATCH	Operation
1	0	0	Does not latch RAM data to output buffer.
2	0	1	Latches every time to output buffer at rising edge of STB signal.
3	1	0	Latches to output buffer at rising edge of STB signal immediately after data input.
4	1	1	Latches every time to output buffer at rising edge of STB signal.

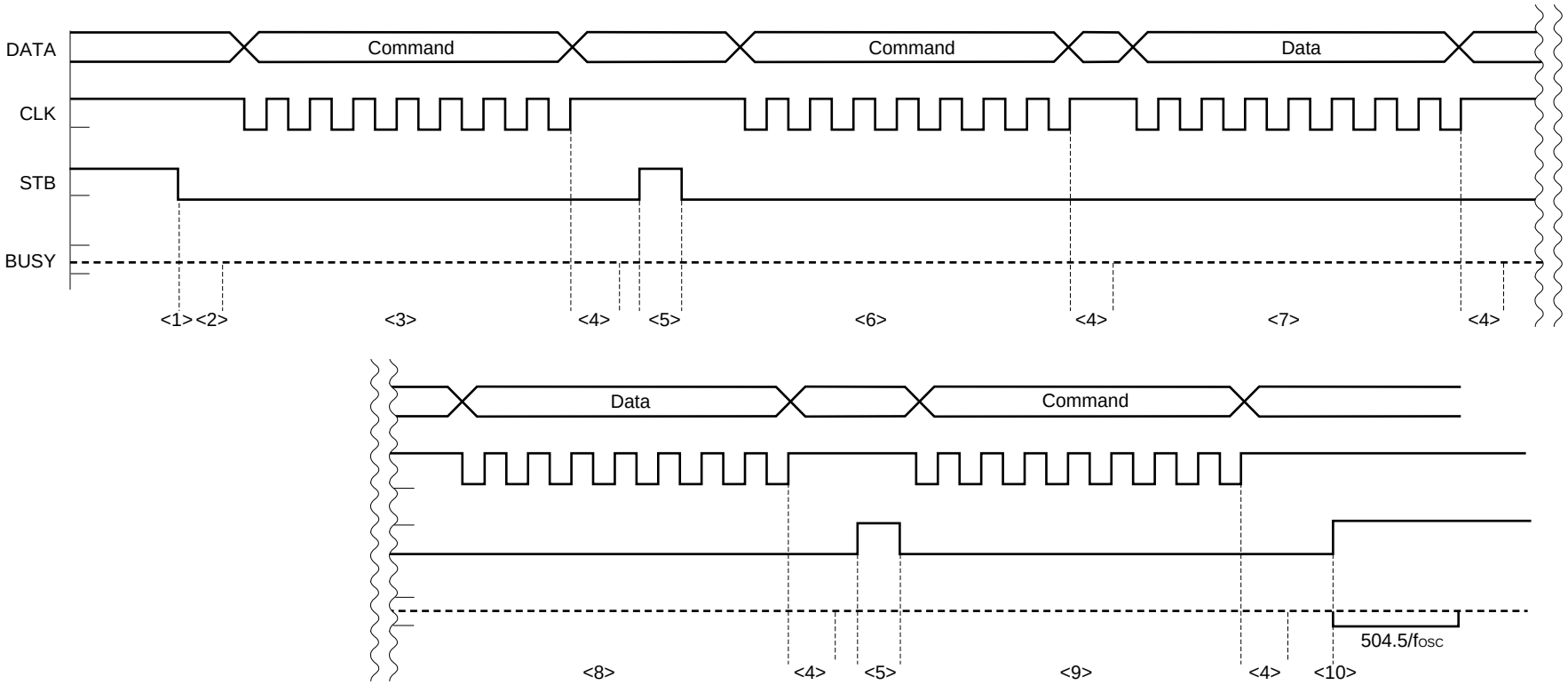
In modes 2 and 4, since latching to the output buffer is executed at the rising edge of the STB signal when only a command has been issued from the STB pin, busy status comes at each rising edge of the STB signal.

(4) Address setting command



Values at power-on reset

		—	0	0	0	0	0



<1> Start serial communications by setting STB signal to logic low

<2> Internal processing time = 300 ns

<3> Transmit mode setting command if initialized (duty cycle and others)

<4> Internal processing time = 300 ns

<5> Wait for command data input after input of STB signal

<6> Input data write method or address setting command

<7> Transmit (receive) RAM data specified by set address

<8> Transmit (receive) RAM data specified by set address

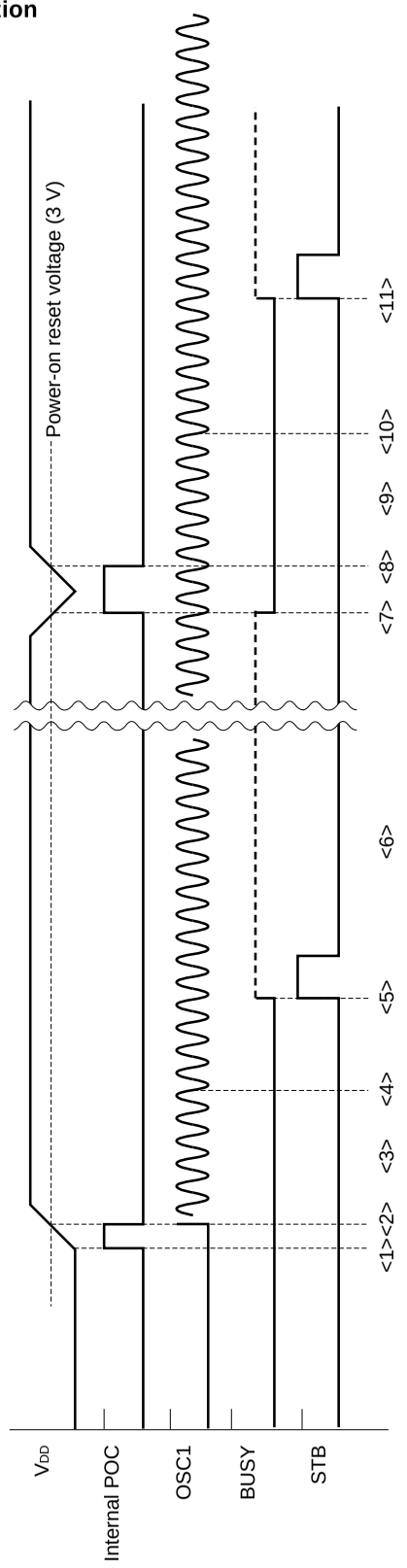
<9> Input data write method or address setting command

<10> Execute RAM data latch or display enable by rising STB pin.

<11> Output logic low from BUSY pin during data latching. The time is 504.5/fosc.

Power-on reset

1) Device operation



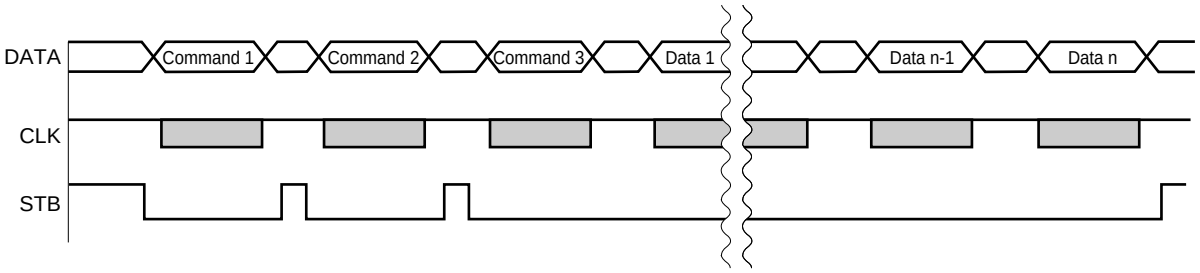
<1> Apply supply voltage V_{DD}.
<2> When V_{DD} becomes higher than power-on reset voltage, device starts operating.
<3> Device stabilization time (less than 10 ms for internal oscillator)
During this time, do not execute STB pin input.
<4> After oscillation stabilization time is over, an STB signal input is waited for.
<5> When a logic high or logic low STB signal is input, a logic high is output from the BUSY pin, and a command input is waited for.
<6> A command input is waited for.
<7> When V_{DD} becomes again a value lower than the power-on reset voltage, device operation stops.
<8> When V_{DD} becomes again a value higher than the power-on reset voltage, device operation starts.
<9> Oscillation stabilization time (less than 10 ms for internal oscillator).
<10> After oscillation stabilization time is over, an STB signal input is waited for.
<11> When a logic high or logic low STB signal is input, a logic high is output from the BUSY pin, and a command input is waited for.
<12> A command input is waited for.

2) Functions of power-on reset

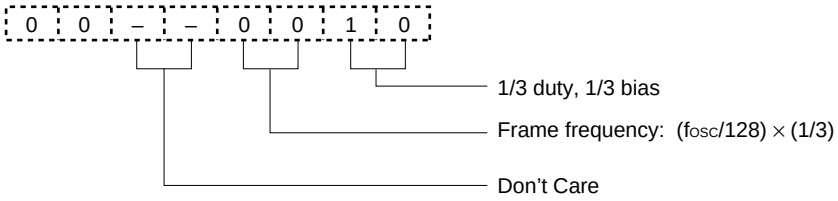
(1) Turns off all displays.
(2) Initializes serial communication.

Application

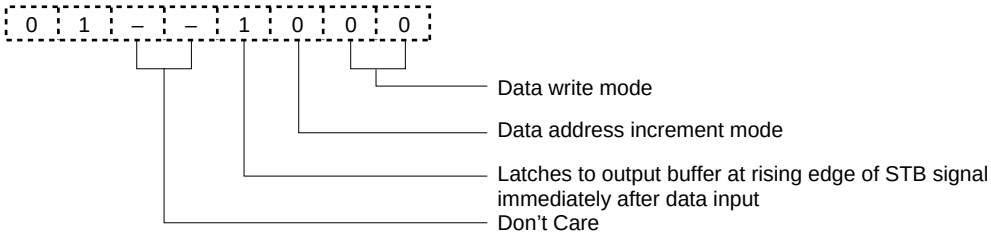
Data transmission examples according to address increment mode



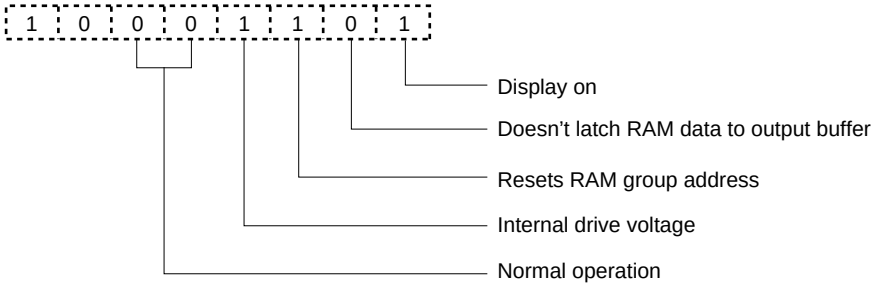
Command 1



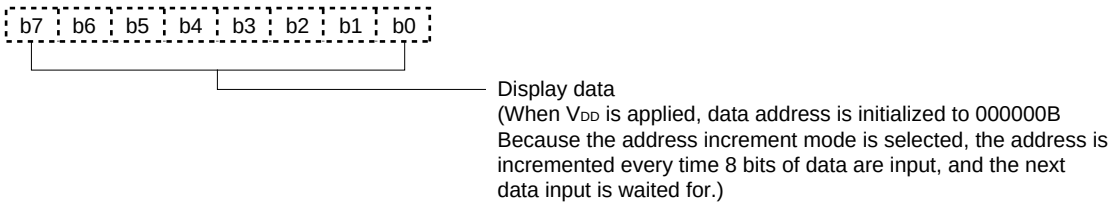
Command 2



Command 3



Data 1 to n



Absolute Maximum Ratings (T_a = 25 °C, GND = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Logic supply voltage	V_{DD}		–0.3 to +7.0	V
Logic input voltage	V_{I1}		–0.3 to V_{DD} +0.3	V
Logic output voltage	V_{O1}		–0.3 to V_{DD} +0.3	V
Driver supply voltage	V_{LCD}		–0.3 to +16	V
Driver input voltage	V_{LC0} - V_{LC2}		–0.3 to V_{LCD} + 0.3	V
Driver output voltage	V_{O2}		–0.3 to V_{LCD} + 0.3	V
Operating temperature range	T_{opt}		–40 to +85	°C
Storage temperature range	T_{stg}		–65 to +150	°C
Permissible package power dissipation	P_d		1000	mW

Recommended Operating Conditions (T_a = –40 to +85 °C, GND = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Logic supply voltage	V_{DD}		3.5		6.0	V
Driver supply voltage	V_{LCD}		V_{DD}		14	V
Driver input voltage	V_{LC0} - V_{LC2}		0		V_{LCD}	V

Electrical Characteristics (T_a = –40 to +85 °C, V_{DD} = 5 V ±10 %, V_{LCD} = 9 to 12 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}		0.7·V_{DD}		V_{DD}	V
Input voltage, low	V_{IL}		0		0.3·V_{DD}	V
Output voltage, high	V_{OH}	OSC_{OUT}, SYNC, BUSY I_{OH} = –1 mA	0.9·V_{DD}			V
Output voltage, low	V_{OL}	OSC_{OUT}, SYNC, BUSY I_{OL} = 1 mA			0.1·V_{DD}	V
Input leak current, high	I_{IH}	V_{IN} = V_{DD}			10	μA
Input leak current, low	I_{IL}	V_{IN} = 0 V	–10			μA
Output leak current, high	I_{LOH}	SYNC, BUSY V_O = V_{DD}			10	μA
Output leak current, low	I_{LOL}	SYNC, BUSY V_O = 0 V	–10			μA
Common output ON resistance	R_{COM}	COM0 - COM3, V_{LCD} = 9 V Ilol = 100 μA		1.2	2.4	kΩ
Segment output ON resistance	R_{SEG}	LCD0 - LCD59, V_{LCD} = 9 V Ilol = 100 μA		2.0	4.0	kΩ
Logic current dissipation	I_{DD}	f_{OSC} = 140 kHz		100	500	μA
Driver current dissipation	I_{LCD}	V_{LCD} = 12 V, without load		500	1000	μA

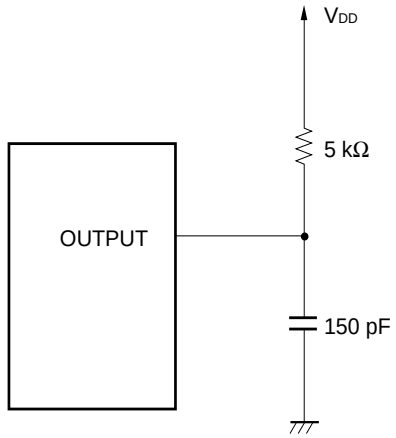
Switching Characteristics (T_a = –40 to +85 °C, V_{DD} = 5 V ±10 %, V_{LCD} = 9 to 12 V, R_L = 5 kΩ, C_L = 150 pF)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Oscillation frequency	f_{SOC}	R = 100 kΩ	98	140	182	kHz
BUSY delay time	t_{DBSY}	STB ↑ → BUSY ↓			1.5	μs
SYNC delay time	t_{DSYNC}				1.5	μs

Timing Requirements (T_a = –40 to +85 °C, V_{DD} = 5 V ±10 %, V_{LCD} = 9 to 12 V, R_L = 5 kΩ, C_L = 150 pF)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock frequency	fc	OSC_{IN} external clock	50		150	kHz
High-level clock pulse width	t_{WHC}	OSC_{IN} external clock	3		16	μs
Low-level clock pulse width	t_{WLC}	OSC_{IN} external clock	3		16	μs
Shift clock cycle	t_{CYK}	CLK	900			ns
High-level shift clock pulse width	t_{WHK}	CLK	400			ns
Low-level shift clock pulse width	t_{WLK}	CLK	400			ns
Data setup time	t_{DS}		100			ns
Data hold time	t_{DH}		200			ns
STB removal time	t_{RSTBK}	STB ↓ → CLK ↑	300			ns
STB hold time	t_{HKSTB}	From the 8th CLK pulse	1			μs
High-level STB pulse width	t_{WHSTB}		1			μs
Low-level STB pulse width	t_{WLSTB}		8.2			μs
SYNC removal time	t_{SREM}		250			ns

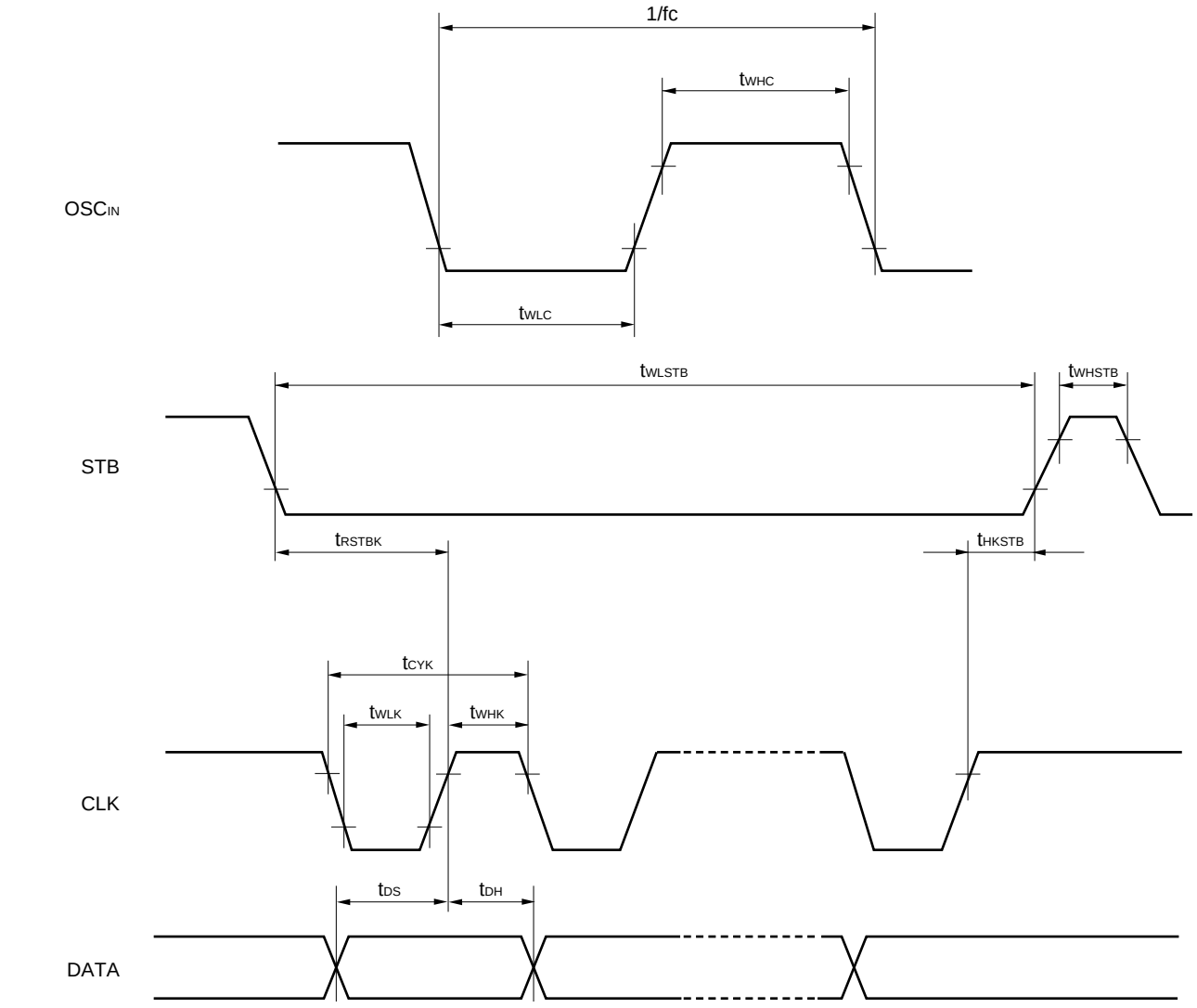
Output Load Circuit

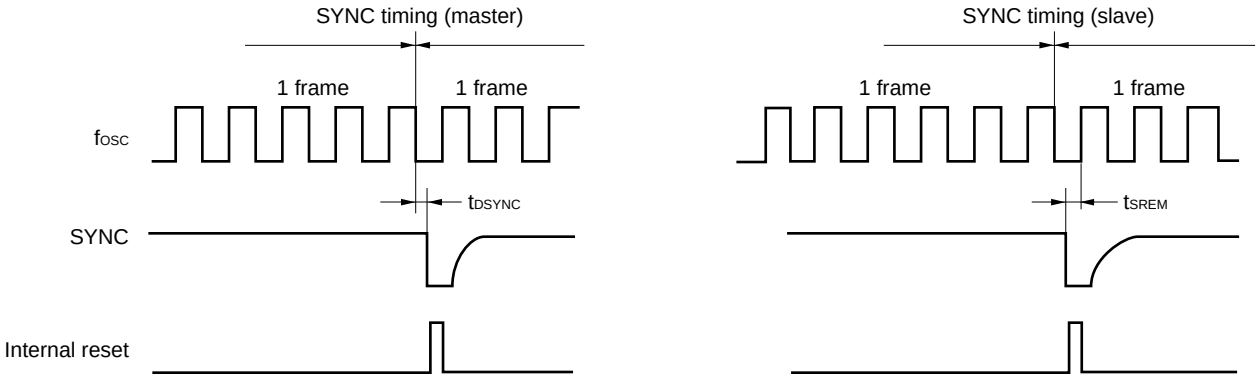


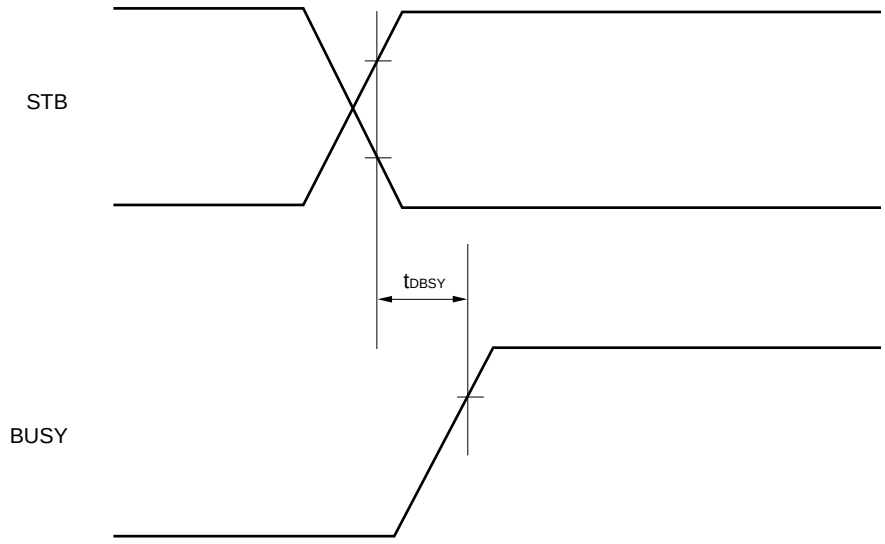
Switching Characteristic Waveform

Measurement points: Input: 0.7 V_{DD}, 0.3 V_{DD}

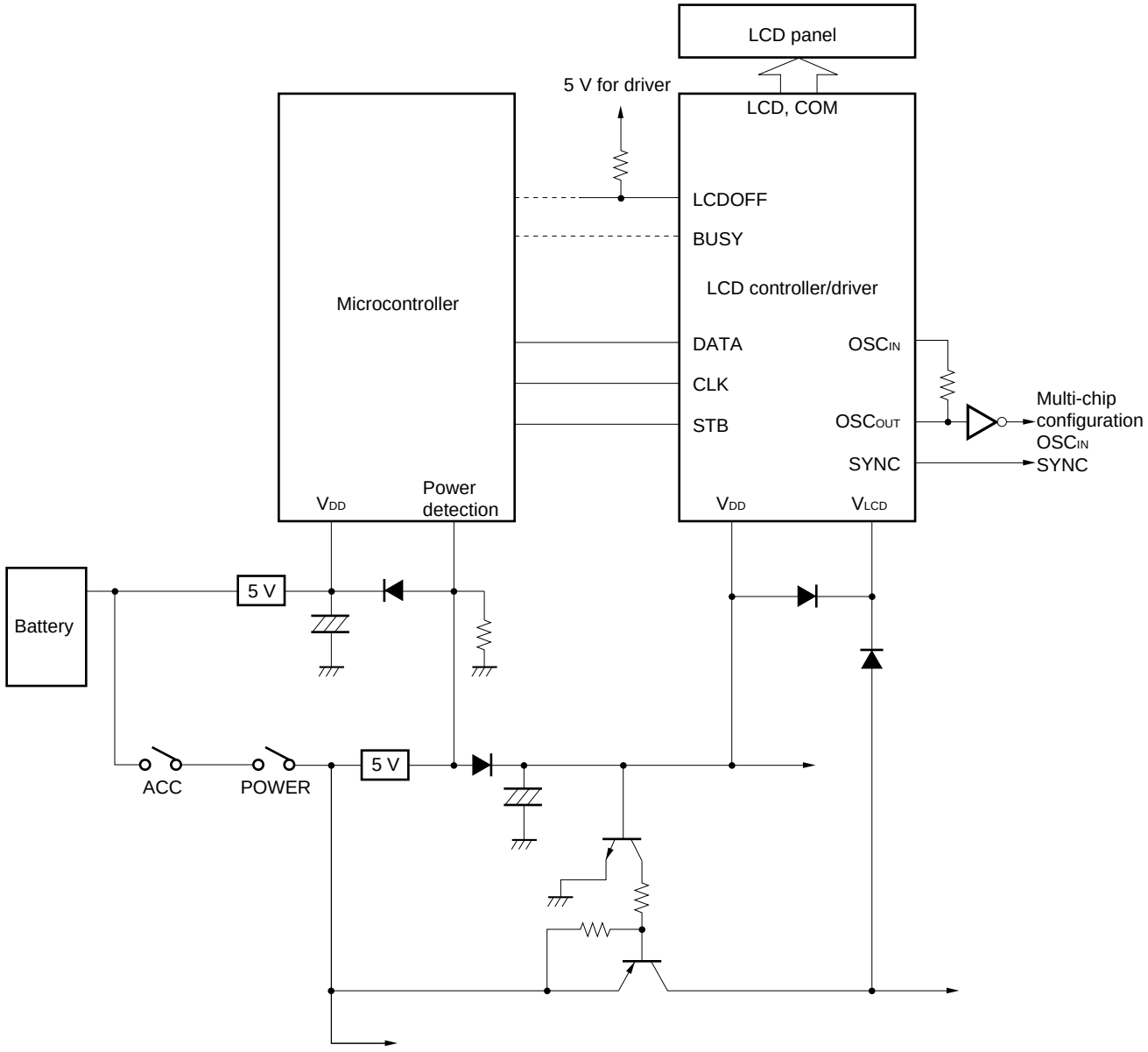
Output: 0.8 V_{DD}, 0.2 V_{DD}






STB
tDBSY
BUSY

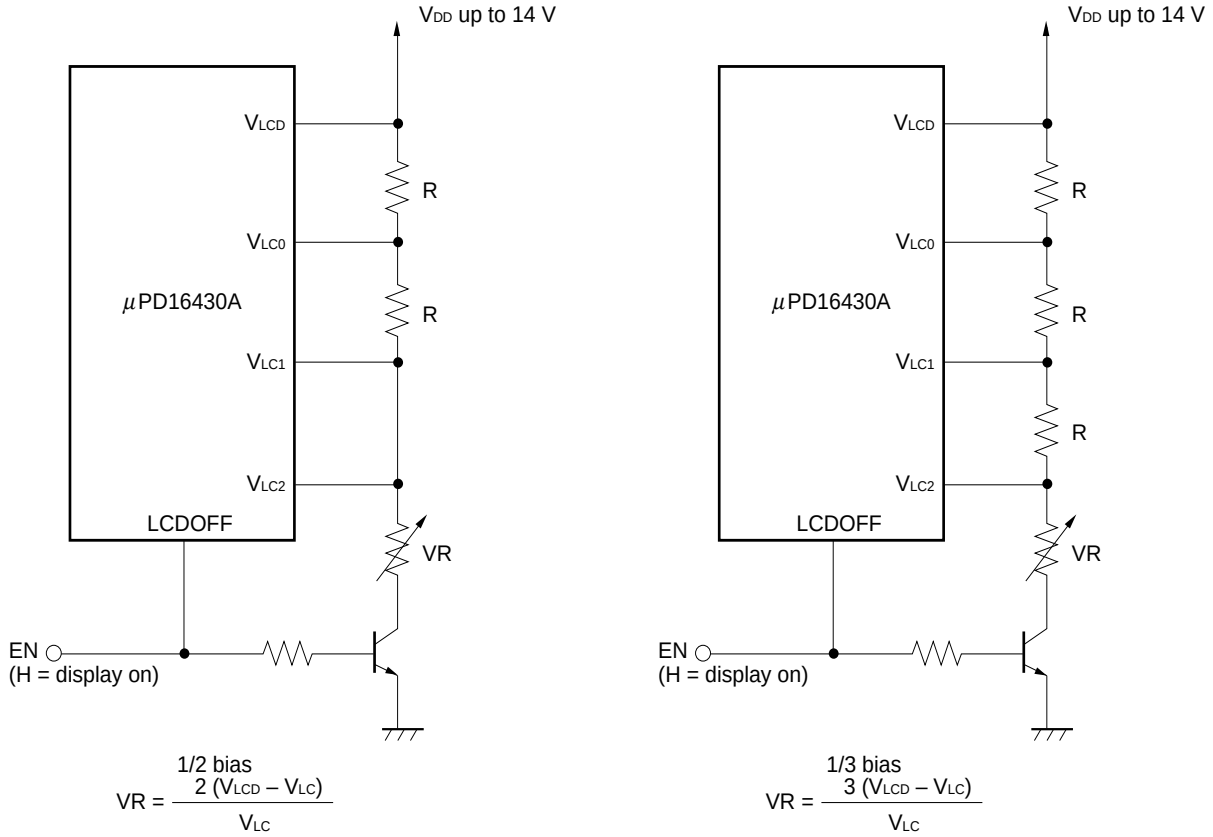
Application Circuit Example



Remark Use low-V_F diodes such as Schottky-barrier diodes, and make sure that V_{DD}, V_{LCD}, V_I, etc. do not exceed absolute maximum ratings of the diodes.

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

1. μPD16430A External Bias Resistor Setting Method



V_{LC} is the peak value of the optimum drive voltage for LCD. (it varies depending on the LCD.)

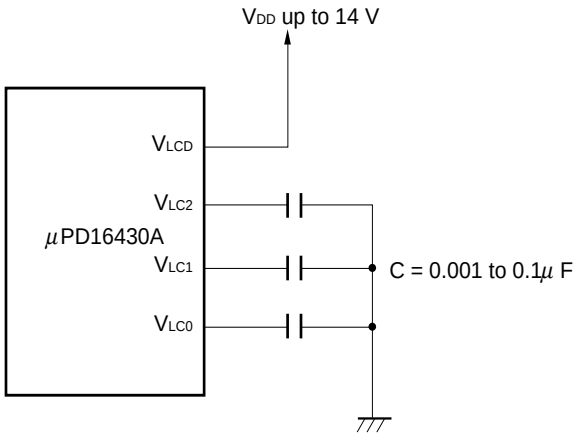
R is a resistance of 1 kΩ to 10 kΩ. Select the resistance value according to the load.

A larger value for R reduces the power dissipation, but causes drive waveform distortions.

Select a largish value for a variable resistor so as to satisfy the equation above.

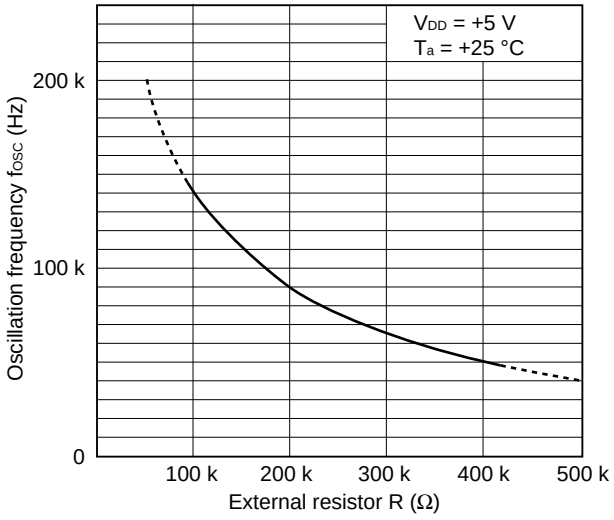
2. When using internal bias

A heavy LCD load may cause distortions in the common waveform. In this case, insert a capacitor for V_{LC0}, V_{LC1} and V_{LC2}.

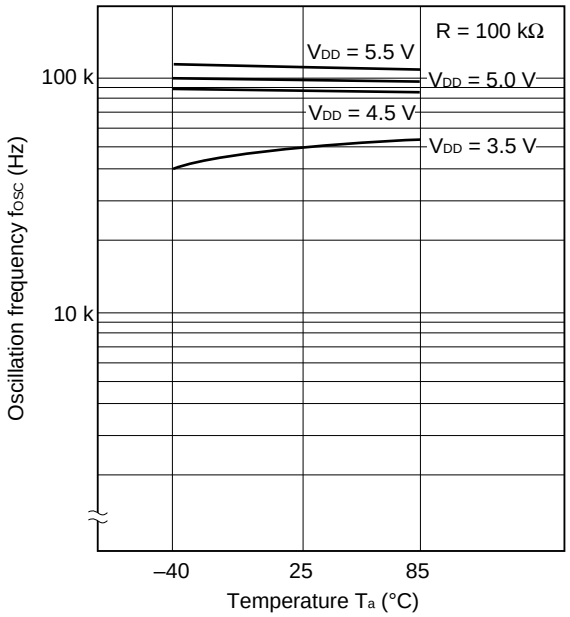


Characteristic Curves

f_{OSC} - R Characteristics



f_{OSC} - V_{DD}, T_a Characteristics



Recommended Soldering Conditions

When soldering on this product, please observe the recommended conditions indicated in the table below.
If planning to solder under different conditions, please consult an NEC sales representative.

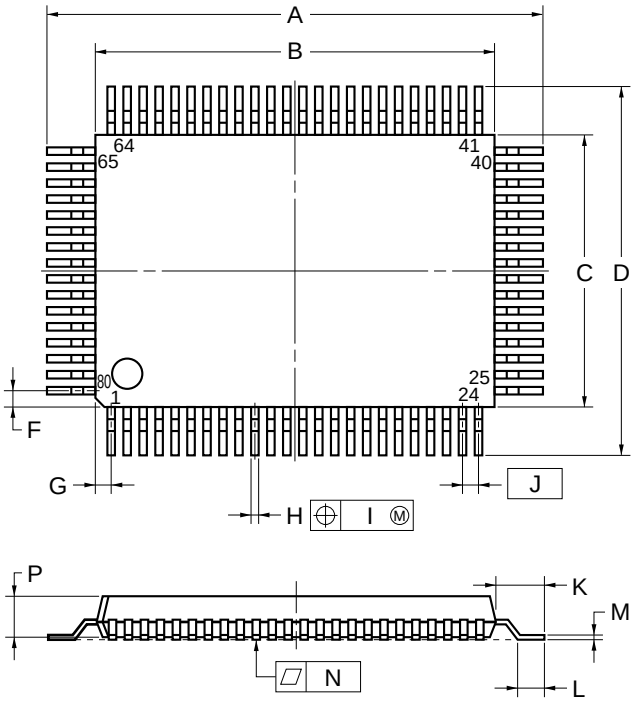
μPD16430AGF-3B9

Soldering method	Soldering conditions	Symbol
Infrared ray reflow	Peak package temperature: 235 °C, time: 30 seconds max. (210 °C min.), number of reflow processes: 2, exposure limit: none **Note**	IR35-00-2
VPS	Peak package temperature: 215 °C, time: 40 seconds max. (200 °C min.), number of reflow processes: 2, exposure limit: none **Note**	VP15-00-2
Wave soldering	Solder temperature: 260 °C max., time: 10 seconds max. number of reflow processes: 1, exposure limit: none **Note**	WS60-00-1
Partial heating	Pin temperature: 300 °C max., time: 10 seconds max., exposure limit: none **Note**	○

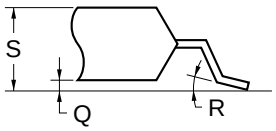
Note Exposure limit before soldering after dry-package is opened.
Storage conditions: 25 °C, relative humidity of 65 % or less.

Caution Do not apply two or more soldering methods (except partial heating) in combination.

80 PIN PLASTIC QFP (14×20)



detail of lead end



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.2±0.2	$0.913^{+0.009}_{-0.008}$
B	20.0±0.2	$0.787^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.2	0.677±0.008
F	1.0	0.039
G	1.8	0.031
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S80GF-80-3B9-3

[MEMO]

[MEMO]