NEC

MOS INTEGRATED CIRCUIT

μPD16449

SOURCE DRIVER FOR 240-OUTPUT TFT-LCD (NAVIGATION, AUTOMOBILE LCD-TV)

DESCRIPTION

μPD16449 is a source driver for TFT liquid crystal panels. This IC consists of a multiplexer circuit supporting a variety of pixel arrays, a shift register that generates sampling timing, and two sample and hold circuits that sample analog voltages. Because the two sample and hold circuits alternately execute sampling and holding, a high definition can be obtained.

In addition, simultaneous sampling and successive sampling are automatically selected according to the pixel array of the LCD panel. It is ideal for a wide range of applications, including navigation systems and automobile LCD-TVs.

FEATURES

- Can be driven on 5 V (Dynamic range: 4.3 V, V_{DD2} = 5.0 V)
- 240-output
- f_{CLK} = 15 MHz MAX. (V_{DD1} = 3.0 V)
- Simultaneous/successive sampling selectable according to pixel array
  - Simultaneous sampling: Vertical stripe
  - Successive sampling: Delta array, mosaic array
- Two sample and hold circuits
- Low output deviation between pins (± 20 mV MAX.)
- Stripe, delta, and mosaic pixel arrays supported by internal multiplexer circuit
- Left and right shift selected by R,/L pin
- TCP/COG mounting possible

★ **Remark** /xxx indicates active low signal.

★ ORDERING INFORMATION

Part Number	Package
μPD16449N-xxx	TCP
μPD16449P	Chip

Remark Purchasing the above chip entails the exchange of documents such as a separate memorandum or product quality, so please contact one of our sales representative.

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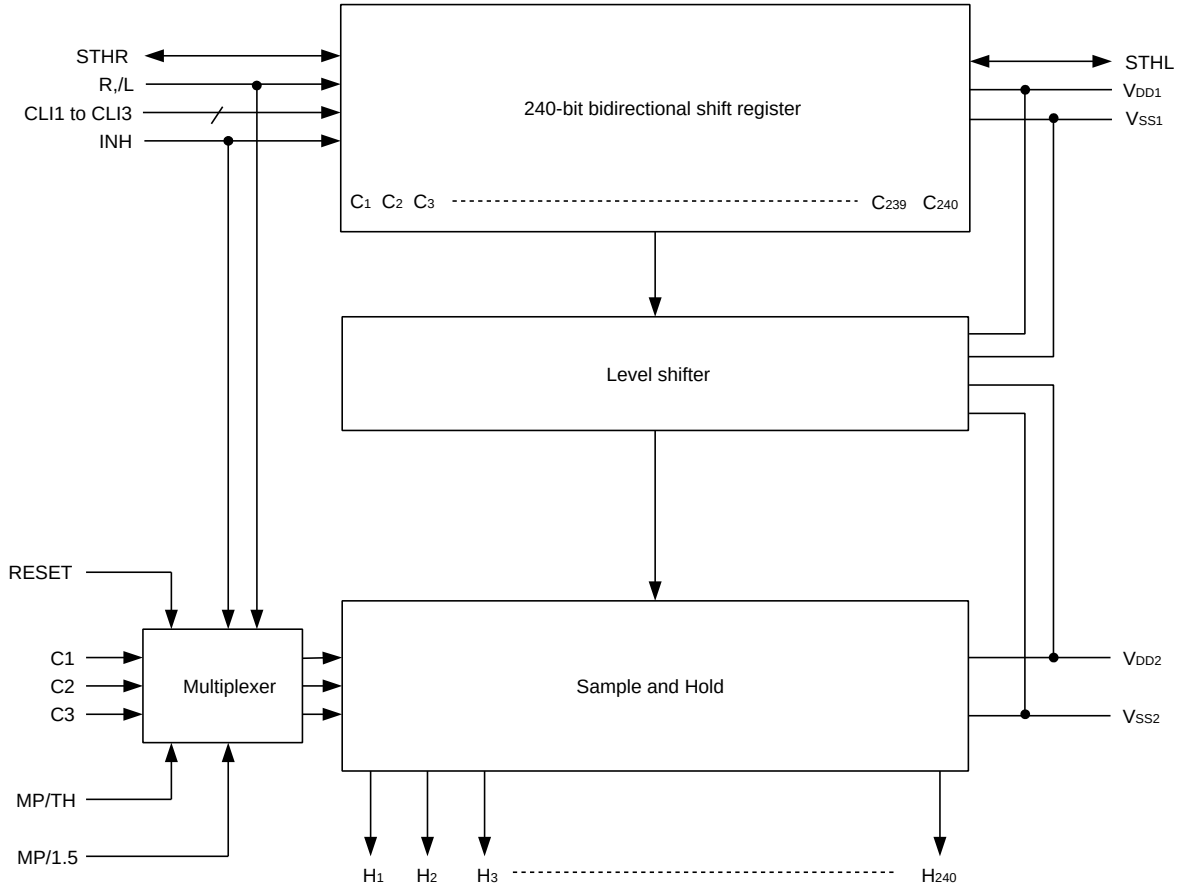
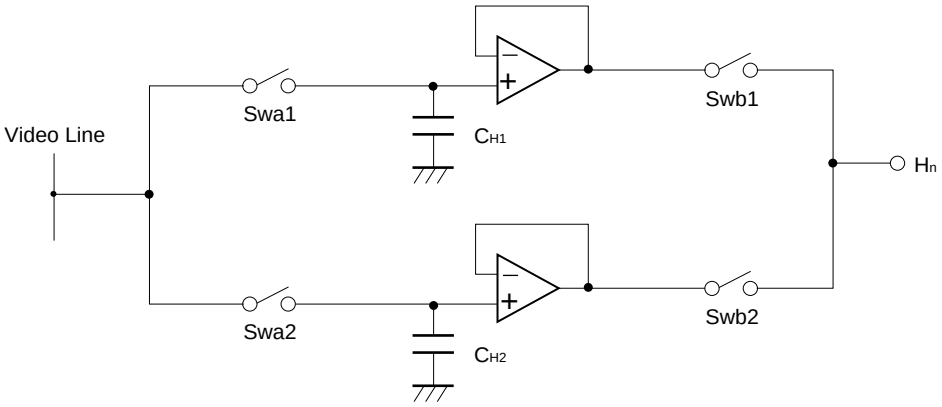
The mark ★ shows major revised points.

★ 1. BLOCK DIAGRAM



2. SAMPLE AND HOLD CIRCUIT AND OUTPUT CIRCUIT



3. PIN CONFIGURATION

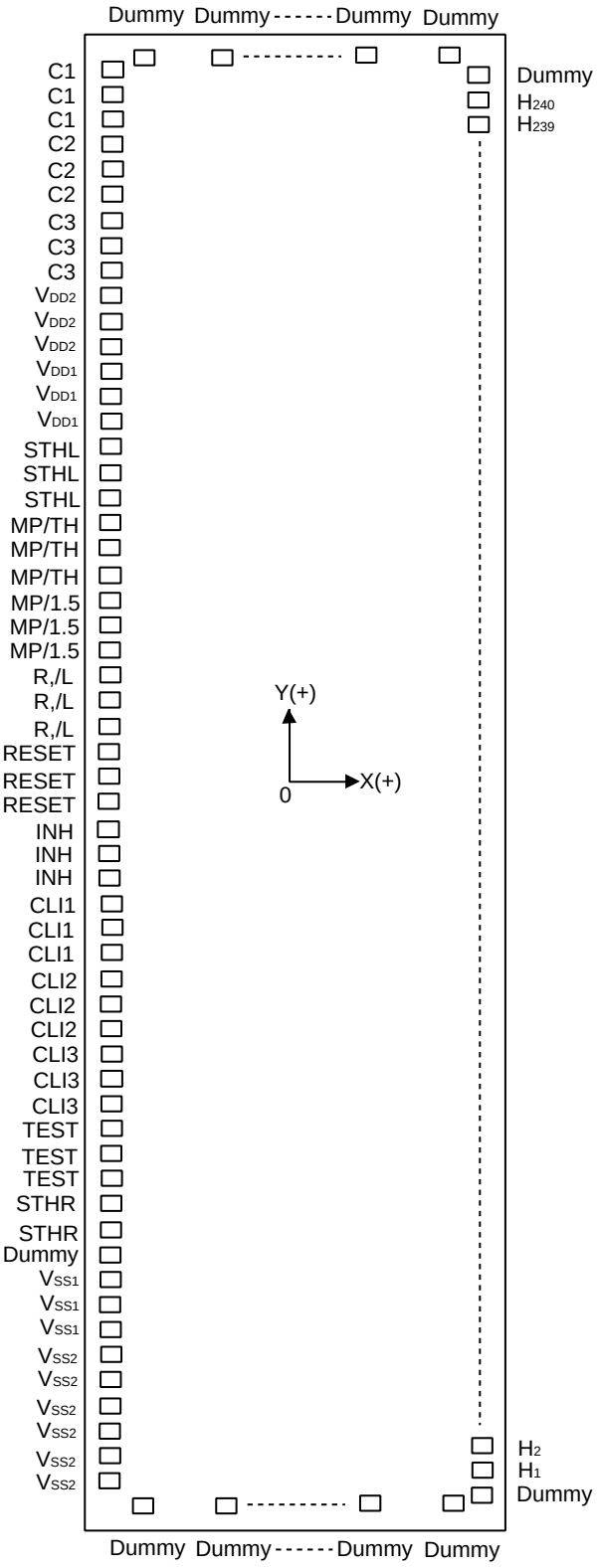


Table 3–1. Pad Layout (1/3)

No.	PAD Name	X [μm]	Y [μm]
1	C1	-400	8033
2	C1	-400	7745
3	C1	-400	7457
4	C2	-400	7169
5	C2	-400	6881
6	C2	-400	6593
7	C3	-400	6305
8	C3	-400	6017
9	C3	-400	5729
10	VDD2	-400	5441
11	VDD2	-400	5153
12	VDD2	-400	4865
13	VDD1	-400	4577
14	VDD1	-400	4289
15	VDD1	-400	4001
16	STHL	-400	3713
17	STHL	-400	3425
18	STHL	-400	3137
19	MP/TH	-400	2849
20	MP/TH	-400	2561
21	MP/TH	-400	2273
22	MP/1.5	-400	1985
23	MP/1.5	-400	1697
24	MP/1.5	-400	1409
25	R,/L	-400	1121
26	R,/L	-400	833
27	R,/L	-400	545
28	RESET	-400	257
29	RESET	-400	-31
30	RESET	-400	-319
31	INH	-400	-607
32	INH	-400	-895
33	INH	-400	-1183
34	CLI1	-400	-1471
35	CLI1	-400	-1759
36	CLI1	-400	-2047
37	CLI2	-400	-2335
38	CLI2	-400	-2623
39	CLI2	-400	-2911
40	CLI3	-400	-3199
41	CLI3	-400	-3487
42	CLI3	-400	-3775
43	TEST	-400	-4063
44	TEST	-400	-4351
45	TEST	-400	-4639
46	STHR	-400	-4927
47	STHR	-400	-5215
48	DUMMY32	-400	-5503
49	VSS1	-400	-5791
50	VSS1	-400	-6079
51	VSS1	-400	-6367
52	VSS2	-400	-6655
53	VSS2	-400	-6943
54	VSS2	-400	-7231
55	VSS2	-400	-7519

No.	PAD Name	X [μm]	Y [μm]
56	VSS2	-400	-7807
57	VSS2	-400	-8095
58	DUMMY39	-277	-8403
59	DUMMY40	-175	-8403
60	DUMMY41	-107	-8403
61	DUMMY42	-39	-8403
62	DUMMY43	29	-8403
63	DUMMY44	131	-8403
64	DUMMY45	327	-8259
65	H1	327	-8157
66	H2	327	-8089
67	H3	327	-8021
68	H4	327	-7953
69	H5	327	-7885
70	H6	327	-7817
71	H7	327	-7749
72	H8	327	-7681
73	H9	327	-7613
74	H10	327	-7545
75	H11	327	-7477
76	H12	327	-7409
77	H13	327	-7341
78	H14	327	-7273
79	H15	327	-7205
80	H16	327	-7137
81	H17	327	-7069
82	H18	327	-7001
83	H19	327	-6933
84	H20	327	-6865
85	H21	327	-6797
86	H22	327	-6729
87	H23	327	-6661
88	H24	327	-6593
89	H25	327	-6525
90	H26	327	-6457
91	H27	327	-6389
92	H28	327	-6321
93	H29	327	-6253
94	H30	327	-6185
95	H31	327	-6117
96	H32	327	-6049
97	H33	327	-5981
98	H34	327	-5913
99	H35	327	-5845
100	H36	327	-5777
101	H37	327	-5709
102	H38	327	-5641
103	H39	327	-5573
104	H40	327	-5505
105	H41	327	-5437
106	H42	327	-5369
107	H43	327	-5301
108	H44	327	-5233
109	H45	327	-5165
110	H46	327	-5097

Table 3–1. Pad Layout (2/3)

No.	PAD Name	X [μm]	Y [μm]
111	H47	327	-5029
112	H48	327	-4961
113	H49	327	-4893
114	H50	327	-4825
115	H51	327	-4757
116	H52	327	-4689
117	H53	327	-4621
118	H54	327	-4553
119	H55	327	-4485
120	H56	327	-4417
121	H57	327	-4349
122	H58	327	-4281
123	H59	327	-4213
124	H60	327	-4145
125	H61	327	-4077
126	H62	327	-4009
127	H63	327	-3941
128	H64	327	-3873
129	H65	327	-3805
130	H66	327	-3737
131	H67	327	-3669
132	H68	327	-3601
133	H69	327	-3533
134	H70	327	-3465
135	H71	327	-3397
136	H72	327	-3329
137	H73	327	-3261
138	H74	327	-3193
139	H75	327	-3125
140	H76	327	-3057
141	H77	327	-2989
142	H78	327	-2921
143	H79	327	-2853
144	H80	327	-2785
145	H81	327	-2717
146	H82	327	-2649
147	H83	327	-2581
148	H84	327	-2513
149	H85	327	-2445
150	H86	327	-2377
151	H87	327	-2309
152	H88	327	-2241
153	H89	327	-2173
154	H90	327	-2105
155	H91	327	-2037
156	H92	327	-1969
157	H93	327	-1901
158	H94	327	-1833
159	H95	327	-1765
160	H96	327	-1697
161	H97	327	-1629
162	H98	327	-1561
163	H99	327	-1493
164	H100	327	-1425
165	H101	327	-1357

No.	PAD Name	X [μm]	Y [μm]
166	H102	327	-1289
167	H103	327	-1221
168	H104	327	-1153
169	H105	327	-1085
170	H106	327	-1017
171	H107	327	-949
172	H108	327	-881
173	H109	327	-813
174	H110	327	-745
175	H111	327	-677
176	H112	327	-609
177	H113	327	-541
178	H114	327	-473
179	H115	327	-405
180	H116	327	-337
181	H117	327	-269
182	H118	327	-201
183	H119	327	-133
184	H120	327	-65
185	H121	327	3
186	H122	327	71
187	H123	327	139
188	H124	327	207
189	H125	327	275
190	H126	327	343
191	H127	327	411
192	H128	327	479
193	H129	327	547
194	H130	327	615
195	H131	327	683
196	H132	327	751
197	H133	327	819
198	H134	327	887
199	H135	327	955
200	H136	327	1023
201	H137	327	1091
202	H138	327	1159
203	H139	327	1227
204	H140	327	1295
205	H141	327	1363
206	H142	327	1431
207	H143	327	1499
208	H144	327	1567
209	H145	327	1635
210	H146	327	1703
211	H147	327	1771
212	H148	327	1839
213	H149	327	1907
214	H150	327	1975
215	H151	327	2043
216	H152	327	2111
217	H153	327	2179
218	H154	327	2247
219	H155	327	2315
220	H156	327	2383

Table 3–1. Pad Layout (3/3)

No.	PAD Name	X [μm]	Y [μm]
221	H157	327	2451
222	H158	327	2519
223	H159	327	2587
224	H160	327	2655
225	H161	327	2723
226	H162	327	2791
227	H163	327	2859
228	H164	327	2927
229	H165	327	2995
230	H166	327	3063
231	H167	327	3131
232	H168	327	3199
233	H169	327	3267
234	H170	327	3335
235	H171	327	3403
236	H172	327	3471
237	H173	327	3539
238	H174	327	3607
239	H175	327	3675
240	H176	327	3743
241	H177	327	3811
242	H178	327	3879
243	H179	327	3947
244	H180	327	4015
245	H181	327	4083
246	H182	327	4151
247	H183	327	4219
248	H184	327	4287
249	H185	327	4355
250	H186	327	4423
251	H187	327	4491
252	H188	327	4559
253	H189	327	4627
254	H190	327	4695
255	H191	327	4763
256	H192	327	4831
257	H193	327	4899
258	H194	327	4967
259	H195	327	5035
260	H196	327	5103
261	H197	327	5171
262	H198	327	5239
263	H199	327	5307
264	H200	327	5375
265	H201	327	5443
266	H202	327	5511
267	H203	327	5579
268	H204	327	5647
269	H205	327	5715
270	H206	327	5783
271	H207	327	5851
272	H208	327	5919
273	H209	327	5987
274	H210	327	6055
275	H211	327	6123

No.	PAD Name	X [μm]	Y [μm]
276	H212	327	6191
277	H213	327	6259
278	H214	327	6327
279	H215	327	6395
280	H216	327	6463
281	H217	327	6531
282	H218	327	6599
283	H219	327	6667
284	H220	327	6735
285	H221	327	6803
286	H222	327	6871
287	H223	327	6939
288	H224	327	7007
289	H225	327	7075
290	H226	327	7143
291	H227	327	7211
292	H228	327	7279
293	H229	327	7347
294	H230	327	7415
295	H231	327	7483
296	H232	327	7551
297	H233	327	7619
298	H234	327	7687
299	H235	327	7755
300	H236	327	7823
301	H237	327	7891
302	H238	327	7959
303	H239	327	8027
304	H240	327	8095
305	DUMMY46	327	8197
306	DUMMY47	131	8405
307	DUMMY48	29	8405
308	DUMMY49	-39	8405
309	DUMMY50	-107	8405
310	DUMMY51	-175	8405
311	DUMMY52	-277	8405

★ 4. PIN FUNCTIONS

<table>
<tr><th>Symbol</th><th>Pin Name</th><th>Pad No.</th><th>I/O</th><th>Description</th></tr>
<tr><td>C1 to C3</td><td>Video signal input</td><td>1 to 3, 4 to 6, 7 to 9</td><td>Input</td><td>Input R, G, and B video signals.</td></tr>
<tr><td>H_1 to H_{300}</td><td>Video signal output</td><td>65 to 304</td><td>Output</td><td>Video signal output pins. Output sampled and held video signals during horizontal period.</td></tr>
<tr><td>STHR,
STHL</td><td>Cascade I/O</td><td>46, 47
16 to 18</td><td>I/O</td><td>Start pulse I/O pins of sample hold timing. STHR serves as an input pin and STHL, as an output pin, in the case of right shift. In the case of left shift, STHL serves as an input pin, and STHR, as an output pin.</td></tr>
<tr><td>CLI1 to
CLI3</td><td>Shift clock input</td><td>34 to 38,
37 to 39,
40 to 42</td><td>Input</td><td>A start pulse is read at the rising edge of CLI1. Sampling pulse SHPn is generated at the rising edge of CLI1 through CLI3 during successive sampling, and at the rising edge of CLI1 during simultaneous sampling (for details, refer to the Timing charts in 5. FUNCTIONAL DESCRIPTION).</td></tr>
<tr><td>INH</td><td>Inhibit input</td><td>31 to 33</td><td>Input</td><td>Selects a multiplexer and one of the two sample and hold circuits at the falling edge.</td></tr>
<tr><td>RESET</td><td>Reset input</td><td>28 to 30</td><td>Input</td><td>Resets the select counter of the multiplexer and the selector circuit of the two sample and hold circuits when it goes high. After reset, the multiplexer is turned OFF, so sure to input one pulse of the INH signal before inputting the video signal. If the video signal is input without the INH signal, sampling is not executed.</td></tr>
<tr><td>MP/TH</td><td>Multiplexer circuit select input (1)</td><td>19 to 21</td><td>Input</td><td rowspan="2">Four types of color filter arrays can be supported by combination of MP/TH and MP/1.5.
<table><tr><th>Mode</th><th>MP/TH</th><th>MP/1.5</th></tr><tr><td>Vertical stripe array</td><td>L</td><td>L</td></tr><tr><td>Single-side delta array</td><td>L</td><td>H</td></tr><tr><td>Mosaic array</td><td>H</td><td>L</td></tr><tr><td>Double-side delta array</td><td>H</td><td>H</td></tr></table></td></tr>
<tr><td>MP/1.5</td><td>Multiplexer circuit select input (2)</td><td>22 to 24</td><td>Input</td></tr>
<tr><td>R,/L</td><td>Shift direction select input</td><td>25 to 27</td><td>Input</td><td>R,/L = H: Right shift: STHR → H_1 → H_{240} → STHL
R,/L = L: Left shift: STHL → H_{240} → H_1 → STHR</td></tr>
<tr><td>V_{DD1}</td><td>Logic power supply</td><td>13 to 15</td><td>–</td><td>3.0 to 5.5 V</td></tr>
<tr><td>V_{DD2}</td><td>Driver power supply</td><td>10 to 12</td><td>–</td><td>5.0 V ± 0.5 V</td></tr>
<tr><td>V_{SS1}</td><td>Logic ground</td><td>49 to 51</td><td>–</td><td>Connect this pin to ground of system.</td></tr>
<tr><td>V_{SS2}</td><td>Driver ground</td><td>52 to 57</td><td>–</td><td>Connect this pin to ground of system.</td></tr>
<tr><td>TEST</td><td>Test</td><td>43 to 45</td><td>–</td><td>Fix this pin to low level.</td></tr>
<tr><td>Dummy</td><td>Dummy</td><td>48, 58 to 64,
305 to 311</td><td>–</td><td>No dummy pins are connected with other pins inside IC.</td></tr>
</table>

5. FUNCTIONAL DISCRIPTION

5.1 Multiplexer Circuit

This circuit selects RGB video signals input to the C1 to C3 pins according to the pixel array of the liquid crystal panel, and outputs the signals to the H_1 through H_{240} pins.

Vertical stripe array, single-/double-side delta array, or mosaic array can be selected by using the MP/TH and MP/1.5 pins.

5.1.1 Vertical stripe array mode (MP/TH = L, MP/1.5 = L)

In this mode, the relation between video signals C1 to C3, and output pins is as shown below. This mode is used to drive a panel of vertical stripe array. In this mode, the multiplexer circuit is in the through status.

Table 5–1. Relation between Video Signals C1 to C3, and Output Pins (during right shift)

Line No. (number of INHn)	RESET	INH	H_1 (H_{240})	H_2 (H_{239})	H_3 (H_{238})	H_4 (H_{237})	...	H_{239} (H_2)	H_{240} (H_1)
0	H	L	Sampling C1 (C3)	Sampling C2 (C2)	Sampling C3 (C1)	Sampling C1 (C3)	...	Sampling C2 (C2)	Sampling C3 (C1)
1	L	↓	Output C1 (C3)	Output C2 (C2)	Output C3 (C1)	Output C1 (C3)	...	Output C2 (C2)	Output C3 (C1)
2	L	↓	Output C1 (C3)	Output C2 (C2)	Output C3 (C1)	Output C1 (C3)	...	Output C2 (C2)	Output C3 (C1)
3	L	↓	Output C1 (C3)	Output C2 (C2)	Output C3 (C1)	Output C1 (C3)	...	Output C2 (C2)	Output C3 (C1)
:	:	:	:	:	:	:	...	:	:

Remark ( ) indicates the case of left shift.

Figure 5–1. Pixel Arrangement of Vertical Stripe Array and Multiplexer Operation

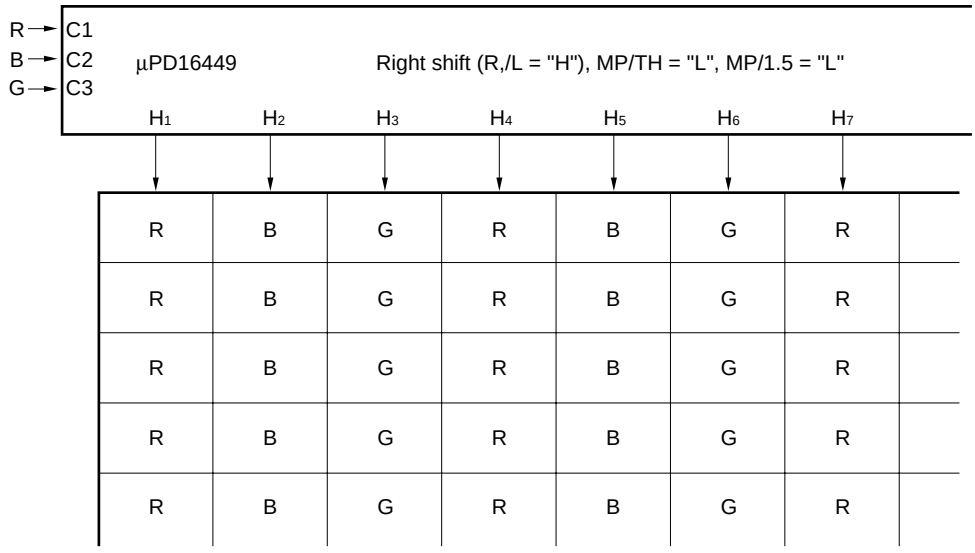
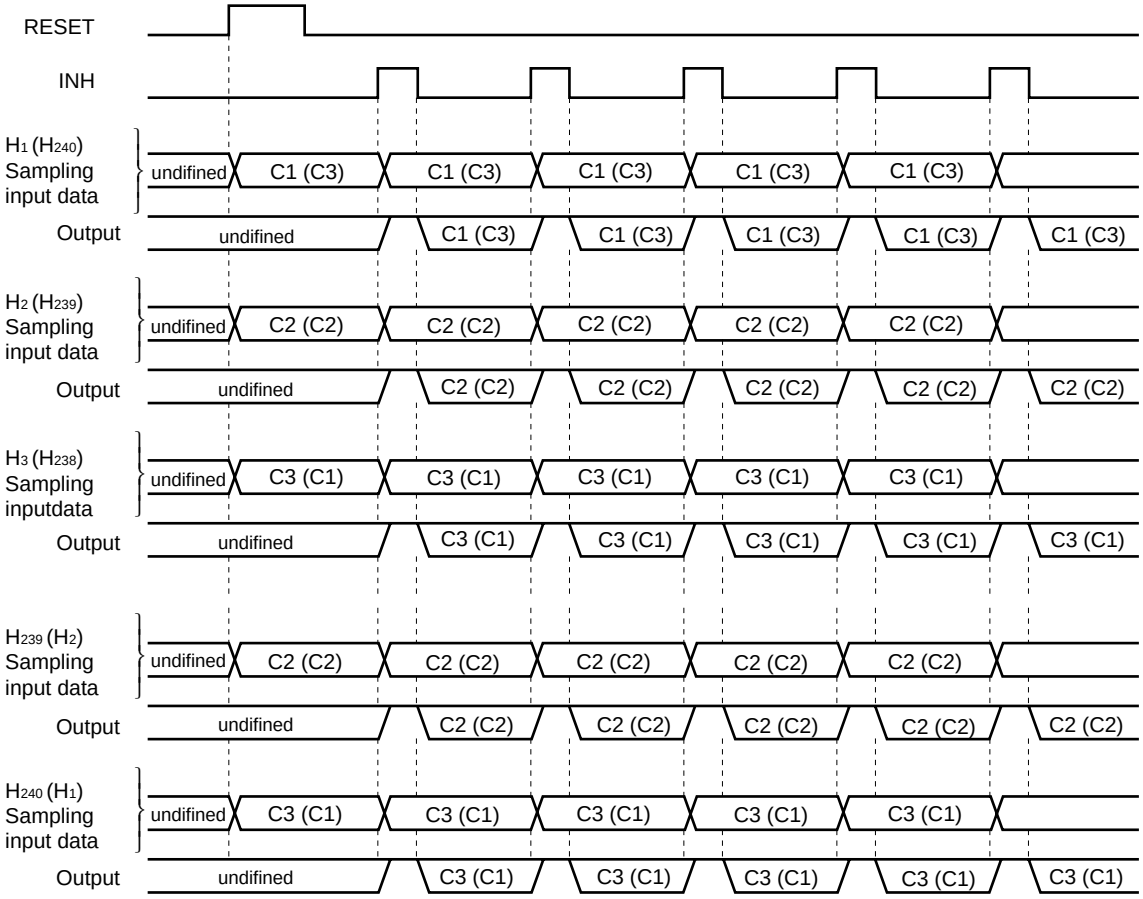


Figure 5–2. Timing Chart of Vertical Stripe Array



5.1.2 Single-side delta array mode (MP/TH = L, MP/1.5 = H)

Table 5–2. Relation between Video Signals C1 to C3, and Output Pins

Line No. (number of INHn)	RESET	INH	H_1 (H_{240})	H_2 (H_{239})	H_3 (H_{238})	H_4 (H_{237})	...	H_{239} (H_2)	H_{240} (H_1)
0	H	L	Undefined	Undefined	Undefined	Undefined	...	Undefined	Undefined
1	L	↓	Sampling C1 (C3)	Sampling C2 (C2)	Sampling C3 (C1)	Sampling C1 (C3)	...	Sampling C2 (C2)	Sampling C3 (C1)
2	L	↓	Output C1 (C3)	Output C2 (C2)	Output C3 (C1)	Output C1 (C3)	...	Output C2 (C2)	Output C3 (C1)
3	L	↓	Output C2 (C1)	Output C3 (C3)	Output C1 (C2)	Output C2 (C1)	...	Output C3 (C3)	Output C1 (C2)
4	L	↓	Output C1 (C3)	Output C2 (C2)	Output C3 (C1)	Output C1 (C3)	...	Output C2 (C2)	Output C3 (C1)
5	L	↓	Output C2 (C1)	Output C3 (C3)	Output C1 (C2)	Output C2 (C1)		Output C3 (C3)	Output C1 (C2)
:	:	:	:	:	:	:	...	:	:

Remark ( ) indicates the case of left shift.

Figure 5–3. Pixel Arrangement of Single-Side Delta Array and Multiplexer Operation

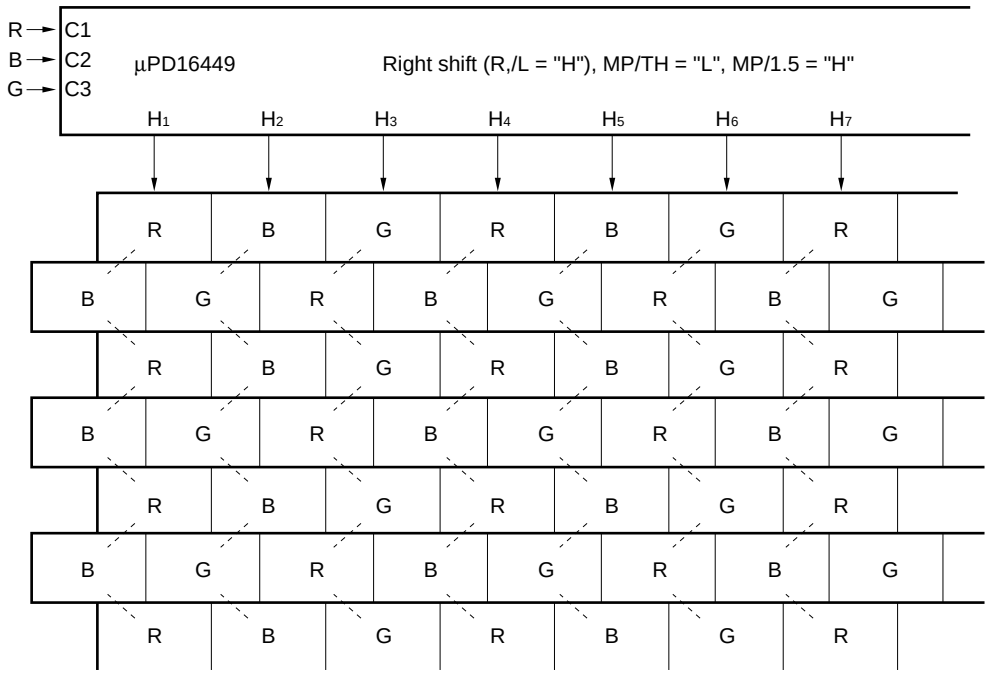
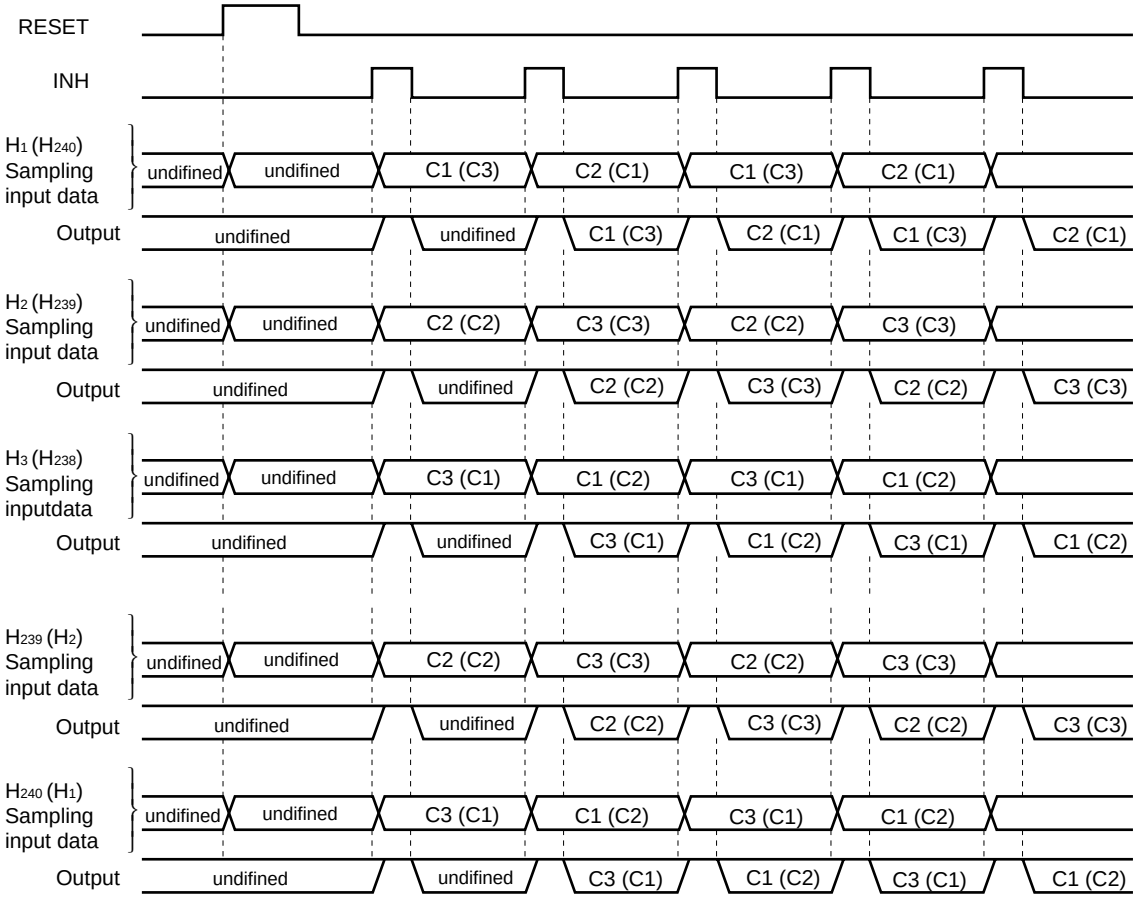


Figure 5–4. Timing Chart of Single-Side Delta Array



5.1.3 Double-side delta array mode (MP/TH = H, MP/1.5 = H)

Because the pad pitch of the μPD16449 is designed so that the IC is mounted on one side, the output pitch must be expanded on the TCP if the IC is mounted on both sides.

Table 5–3. Relation between Video Signals C1 to C3 and Output Pins

Line No. (number of INHn)	RESET	INH	H_1 (H_{240})	H_2 (H_{239})	H_3 (H_{238})	H_4 (H_{237})	...	H_{239} (H_2)	H_{240} (H_1)
0	H	L	Undefined	Undefined	Undefined	Undefined	...	Undefined	Undefined
1	L	↓	Sampling C2 (C3)	Sampling C3 (C2)	Sampling C1 (C1)	Sampling C2 (C3)	...	Sampling C3 (C2)	Sampling C1 (C1)
2	L	↓	Output C2 (C3)	Output C3 (C2)	Output C1 (C1)	Output C2 (C3)	...	Output C3 (C2)	Output C1 (C1)
3	L	↓	Output C1 (C1)	Output C2 (C3)	Output C3 (C2)	Output C1 (C1)	...	Output C2 (C3)	Output C3 (C2)
4	L	↓	Output C2 (C3)	Output C3 (C2)	Output C1 (C1)	Output C2 (C3)	...	Output C3 (C2)	Output C1 (C1)
5	L	↓	Output C1 (C1)	Output C2 (C3)	Output C3 (C2)	Output C1 (C1)	...	Output C2 (C3)	Output C3 (C2)
:	:	:	:	:	:	:	...	:	:

Remark ( ) indicates the case of left shift.

Figure 5–5. Pixel Arrangement of Double-Side Delta Array and Multiplexer Operation

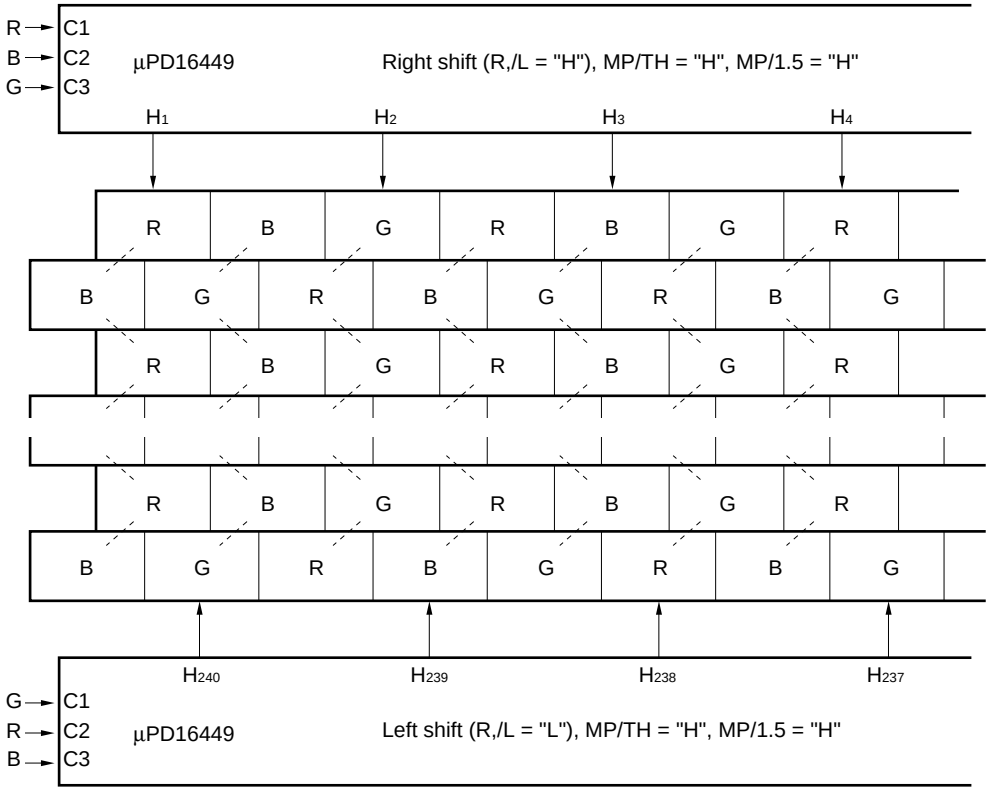
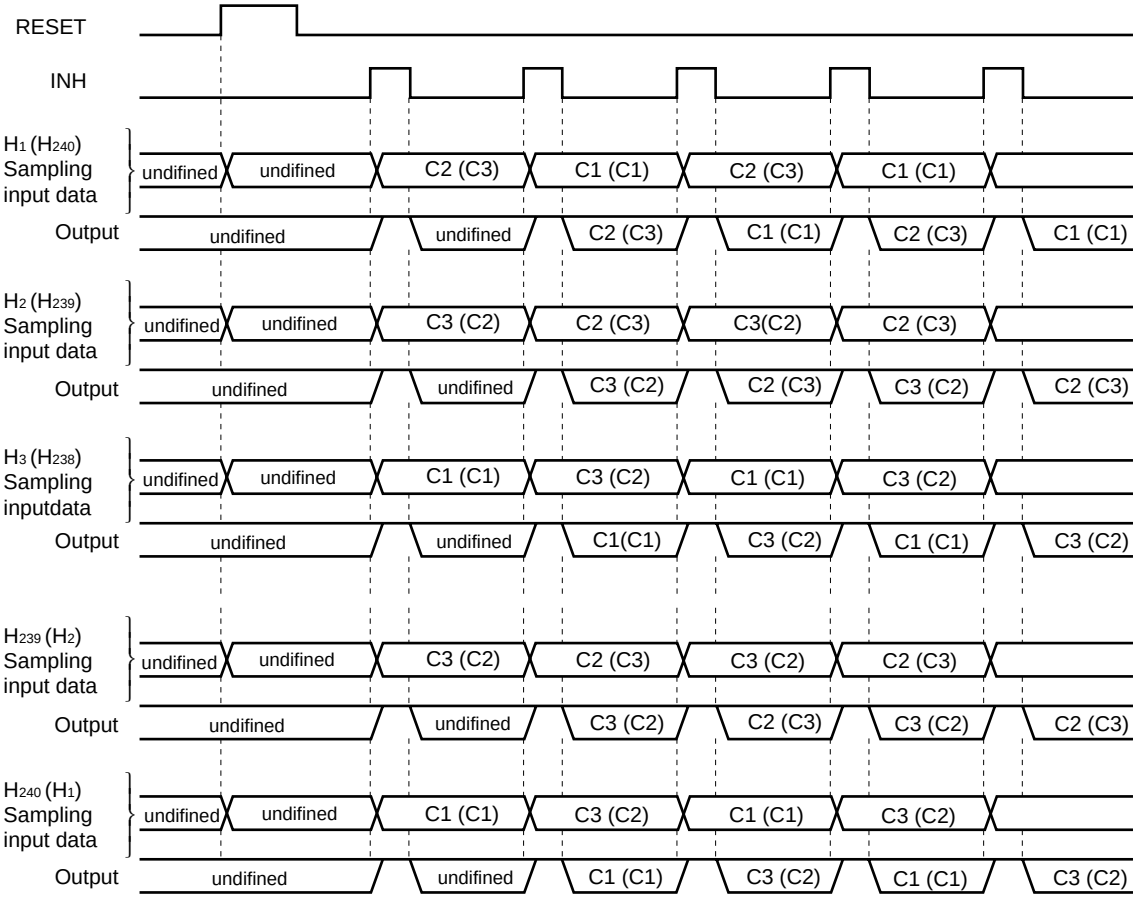


Figure 5–6. Timing Chart of Both-Sides Delta Array



5.1.4 Mosaic array mode (MP/TH = H, MP/1.5 = L)

Table 5–4. Relation between Video Signals C1 to C3, and Output Pins

Line No. (number of INHn)	RESET	INH	H_1 (H_{240})	H_2 (H_{239})	H_3 (H_{238})	H_4 (H_{237})	...	H_{239} (H_2)	H_{240} (H_1)
0	H	L	Undefined	Undefined	Undefined	Undefined	...	Undefined	Undefined
1	L	↓	Sampling C1 (C3)	Sampling C2 (C2)	Sampling C3 (C1)	Sampling C1 (C3)	...	Sampling C2 (C2)	Sampling C3 (C1)
2	L	↓	Output C1 (C3)	Output C2 (C2)	Output C3 (C1)	Output C1 (C3)	...	Output C2 (C2)	Output C3 (C1)
3	L	↓	Output C3 (C2)	Output C1 (C1)	Output C2 (C3)	Output C3 (C2)	...	Output C1 (C1)	Output C2 (C3)
4	L	↓	Output C2 (C1)	Output C3 (C3)	Output C1 (C2)	Output C2 (C1)	...	Output C3 (C3)	Output C1 (C2)
5	L	↓	Output C1 (C3)	Output C2 (C2)	Output C3 (C1)	Output C1 (C3)	...	Output C2 (C2)	Output C3 (C1)
:	:	:	:	:	:	:	...	:	:

Remark ( ) indicates the case of left shift.

Figure 5–7. Pixel Arrangement of Mosaic Array and Multiplexer Operation

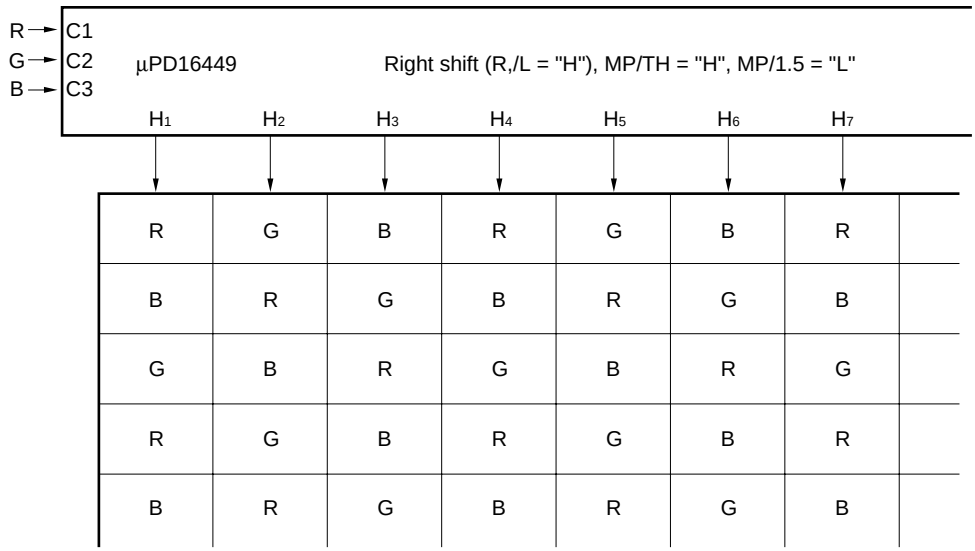
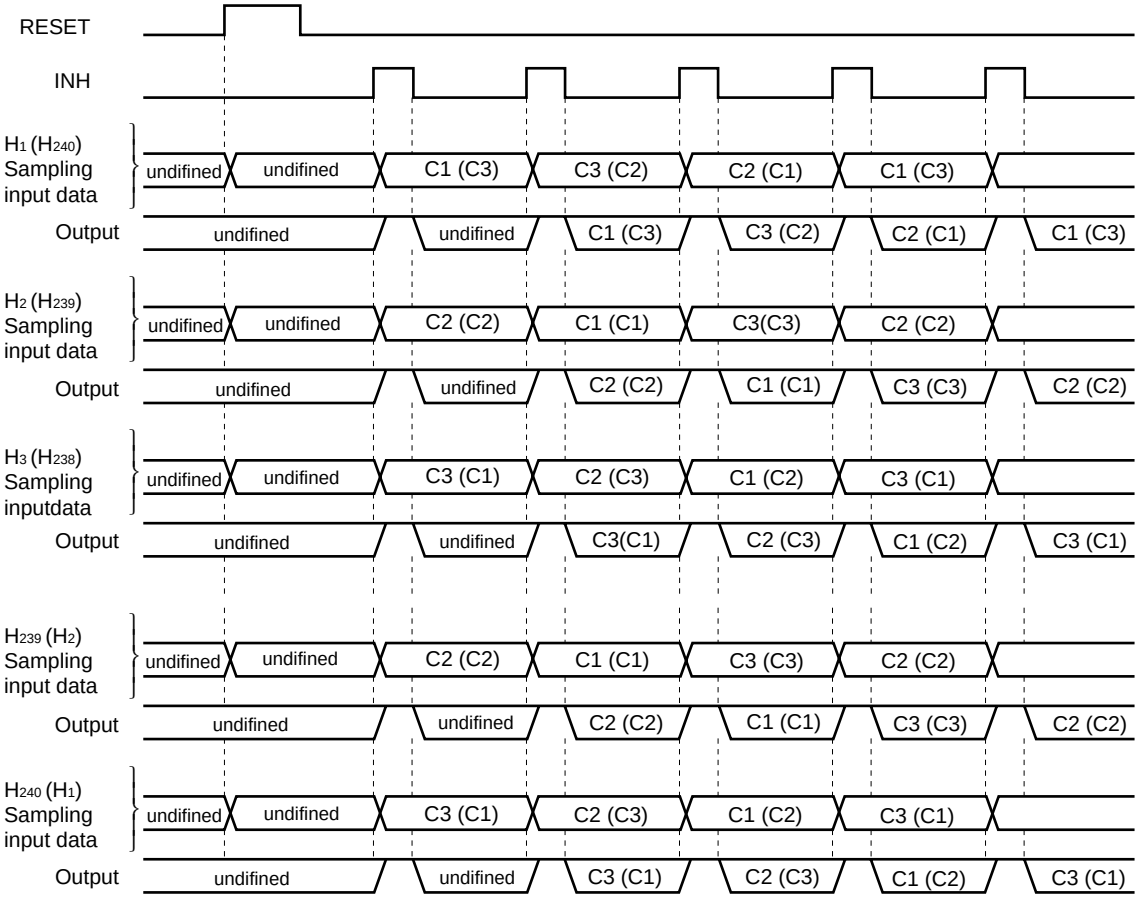
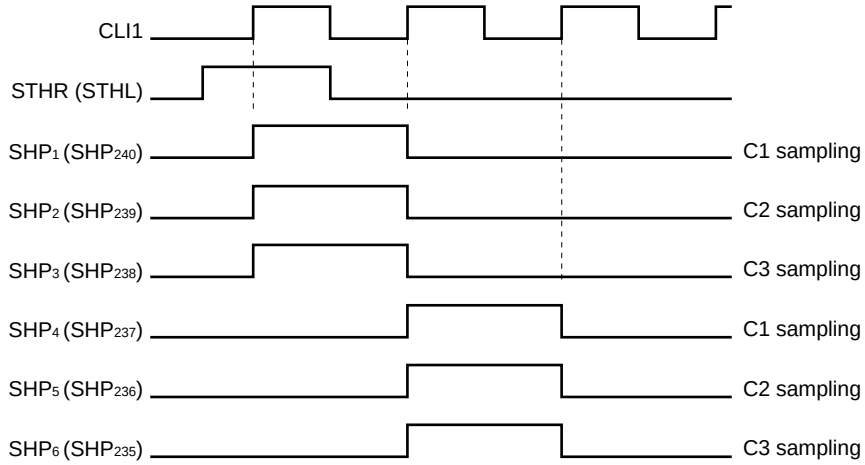


Figure 5–8. Timing Chart of Mosaic Array



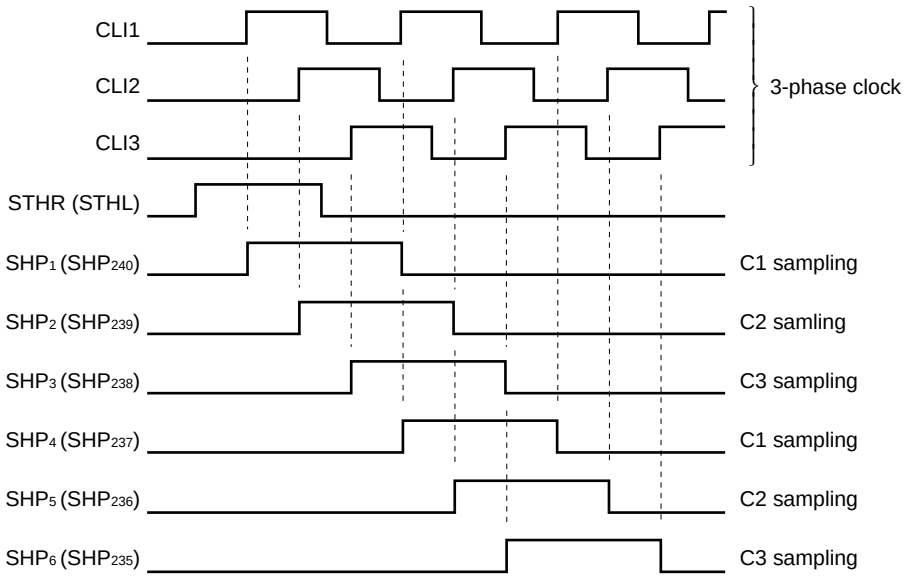
5.1.5 Relation between Shift Clock CLIn and Internal Sampling Pulse SHPn

(1) Simultaneous sampling (( ) indicates the case of left shift.)



Remark C1 through C3 are sampled while SHPn is high level.

(2) Successive sampling (( ) indicates the case of left shift.)

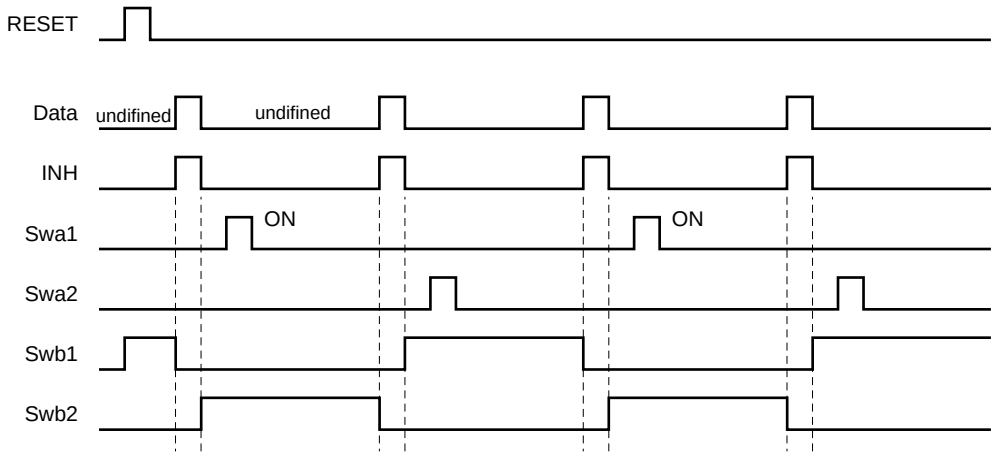


Remarks 1. Input a three-phase clock to shift clock pins CLI1 through CLI3.

2. The video signals (C1 to C3) are sampled while SHPn is high level.

5.2 Sample and Hold Circuit

The sample and hold circuit samples and holds the video input signals C1 through C3 selected by the multiplexer circuit in the timing shown below. Swa1 through Swb2 are reset by the RESET signal and change at the rising and falling edges of the INH signal (refer to **1. BLOCK DIAGRAM**.).



5.3 Write Operation Timing

The sampled video signals are written to the LCD panel by output currents I_{VOL} and I_{VOH} via output buffer. The dynamic range is 4.3 V MIN. (V_{DD2} = 5.0 V).

While INH = H, do not stop shift clocks CLI1 through CLI3.

The output operation of this IC is controlled by INH signals.

INH = Hi-Z

INH = Connected with internal circuit (switch sample and hold circuit at the falling edge.)

Therefore, performing V_{COM} inversion while INH = L causes current flow to these IC output pins, which may result in malfunction. Perform V_{COM} in version during INH = H (Hi-Z) and start output operation of the next line after the V_{COM} signal is stable enough to operate. Make sure to evaluate this output operation sufficiently.

Cautions 1. Turn on power to V_{DD1}, logic input, V_{DD2}, and video signal input in that order to prevent destruction due to latch-up, and turn off power in the reverse sequence. Observe this power sequence even during the transition period.

2. The μPD16449 is designed to input successive signals such as chrome signals. The input band of the video signals is designed to be 9 MHz MAX. If video signals faster than that are input, display is not performed correctly.

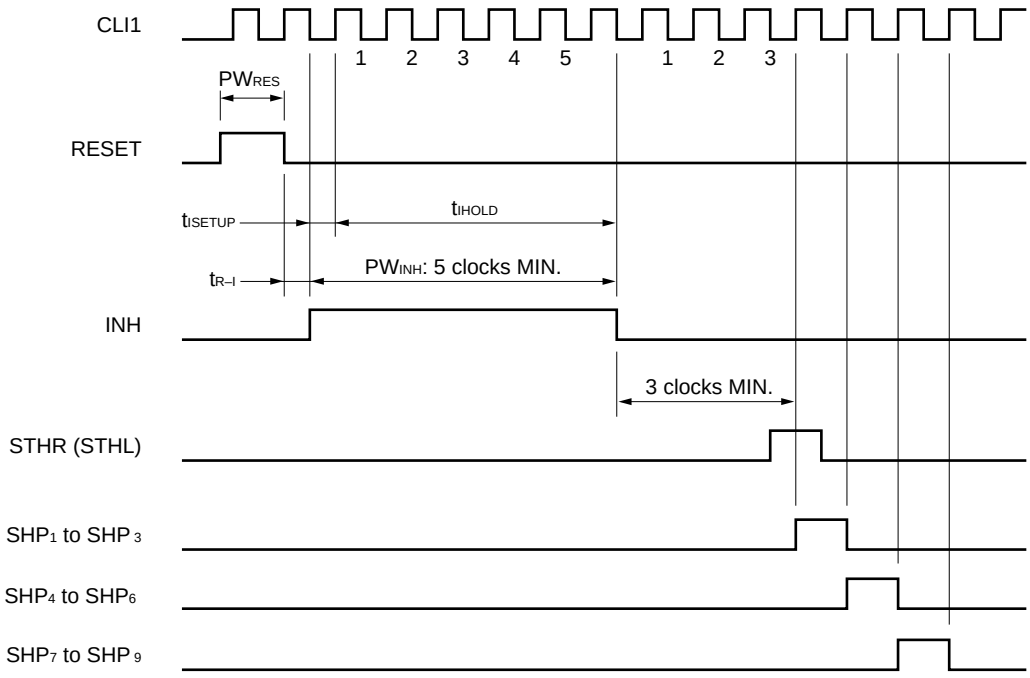
3. Insert a bypass capacitor of 0.1 μF between V_{DD1} and V_{SS1} and between V_{DD2} and V_{SS2}. If the power supply is not reinforced, the sampling voltage may be abnormal if the supply voltage fluctuates.

4. Display may not be correctly performed if noise is superimposed on the start pulse pin. Therefore, be sure to input a reset signal during the vertical blanking period.

5. Even if the start pulse width is extended by half a clock or more, sampling start timing SHP_1 is not affected, and the sampling operation is performed normally.

6. When the multiplexer circuit is used in the vertical stripe mode, C1 to C3 are simultaneously sampled at the rising edge of SHPn. Internally, however, only CLI1 is valid. Therefore, input a shift clock to CLI1 only. At this time, keep the CLI2 and CLI3 pins to "L".
When using the multiplexer circuit in the delta array mode or mosaic array mode, C1 to C3 are sequentially sampled. Input a three-phase clock to CLI1 through CLI3 (for the sampling timing, refer to 5. FUNCTIONAL DESCRIPTION.).

7. The recommended timing of t_{R-1} and PW_{RES} on starting is shown below (The following timing chart shows simultaneous sampling.).
An INH pulse width of at least 5 clocks is required to reset the internal logic. Unless the INH pulse is input after reset, sampling is not performed in the correct sequence.



6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = 0 V)

Parameter	Symbol	Condition	Ratings	Unit
Logic supply voltage	V_{DD1}		–0.5 to +6.0	V
Driver supply voltage	V_{DD2}		–0.5 to +6.0	V
Logic input voltage	V_I		–0.5 to V_{DD1} +0.5	V
Video input voltage	V_{VI}	C1 to C3	–0.5 to V_{DD2} +0.5	V
Logic output voltage	V_{01}		–0.5 to V_{DD1} +0.5	V
Driver output voltage	V_{02}		–0.5 to V_{DD2} +0.5	V
Driver output current	I_{O2}		±10	mA
Operating temperature range	T_A		–30 to +85	°C
Storage temperature range	T_{stg}		–65 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions (T_A = –40 to +85°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Logic supply voltage	V_{DD1}		3.0	3.3	5.5	V
Driver supply voltage	V_{DD2}		4.5	5.0	5.5	V
Video input voltage	V_{VI}		V_{SS2} + 0.35		V_{DD2} – 0.35	V
Driver output voltage	V_{02}		V_{SS2} + 0.35		V_{DD2} – 0.35	V
High level Input voltage	V_{IH}		0.7 V_{DD1}		V_{DD1}	V
Low level Input voltage	V_{IL}		0		0.3 V_{DD1}	V

Electrical Characteristics (T_A = –30 to +85 °C, V_{DD1} = 3.0 to 5.5 V, V_{DD2} = 5.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Maximum video signal output voltage	V_{VOH}			V_{DD2} – 0.35			V
Minimum video signal output voltage	V_{VOL}					0.35	V
Logic high level output voltage	V_{LOH}	STHL, STHR pins, I_{OH} = –1.0 mA		0.9 V_{DD1}			V
Logic low level output voltage	V_{LOL}	STHL, STHR pins I_{OL} = 1.0 mA				0.1 V_{DD1}	V
Video signal high level output current	V_{VOH}	I_{NH} = L, V_{OF} = V_{DD2} – 1.0 V V_O = V_{DD2} – 0.5 V			–0.20	–0.08	mA
Video signal low level output current	V_{VOL}	I_{NH} = L, V_{OF} = 1.0 V, V_O = 0.5 V		0.08	0.20		mA
Reference voltage 1	V_{REF1}	V_{DD2} = 5.0 V, T_A = 25°C, V_{VI} = 0.5 V			0.49		V
Reference voltage 2	V_{REF2}	V_{DD2} = 5.0 V, T_A = 25°C, V_{VI} = 2.0 V			1.99		V
Reference voltage 3	V_{REF3}	V_{DD2} = 5.0 V, T_A = 25°C, V_{VI} = 3.5 V			3.49		V
Output voltage deviation 1	ΔV_{VO1}	V_{DD2} = 5.0 V, T_A = 25°C, V_{VI} = 0.5 V				±20	mV
Output voltage deviation 2	ΔV_{VO2}	V_{DD2} = 5.0 V, T_A = 25°C, V_{VI} = 2.0 V				±20	mV
Output voltage deviation 3	ΔV_{VO3}	V_{DD2} = 5.0 V, T_A = 25°C, V_{VI} = 3.5 V				±20	mV
Logic input leakage current	I_{LL}					±1.0	μA
Video input leakage current	I_{VL}					±10	μA
Logic dynamic current consumption	I_{DD1}	f_{CLI} = 14 MHz V_{VI} = 2.0 V, no load, f_{INH} = 15.4 kHz, PW_{INH} = 5.0 μs	V_{DD1} = 3.3 V ± 0.3 V			2.5	mA
			V_{DD1} = 5.0 V ± 0.5 V			4.0	mA
Driver dynamic current consumption	I_{DD2}	f_{CLI} = 14 MHz V_{VI} = 2.0 V, no load, f_{INH} = 15.4 kHz, PW_{INH} = 5.0 μs				10.0	mA

Remarks 1. V_{OF}: output applied voltage, V_O: output voltage without load

2. The reference values are typical values only. The output deviation is only guaranteed within the chip.

Switching Characteristics (T_A = –30 to +85°C, V_{DD1} = 3.0 to 5.5 V, V_{DD2} = 5.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start pulse propagation delay time	t_{PHL}	C_L = 20 pF	10		54	ns
	t_{PLH}	C_L = 20 pF	10		54	ns
Clock frequency 1	$f_{CLK\,1}$				15	MHz
Clock frequency 2	$f_{CLK\,2}$	With 3-phase clock input			8	MHz
Logic input capacitance	C_{I1}	Other than STHL, STHR			15	pF
STHL, STHR input capacitance	C_{I2}	STHL, STHR			20	pF
Video input capacitance	C_3	C1 to C3, V_{VI} = 2.0 V			50	pF

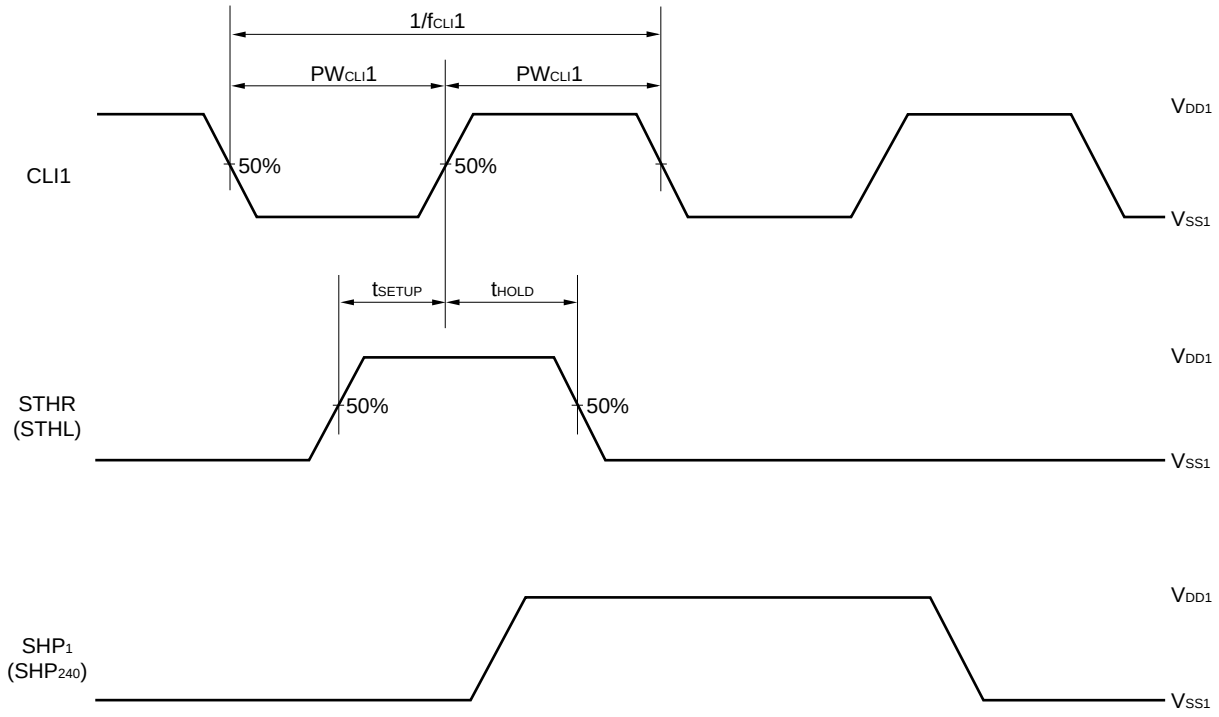
Timing Requirements (T_A = –30 to +85 °C, V_{DD1} = 3.0 to 5.5 V, V_{DD2} = 5.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock pulse width	PW_{CLI}	Duty = 50%	33			ns
Start pulse setup time	t_{SETUP}		8			ns
Start pulse hold time	t_{HOLD}		8			ns
Reset pulse width	PW_{RES}		66			ns
INH setup time	t_{ISETUP}		33			ns
INH hold time	t_{IHOLD}		33			ns
Reset-INH time	t_{R-I}		81			ns
INH pulse width	PW_{INH}		5			CLK

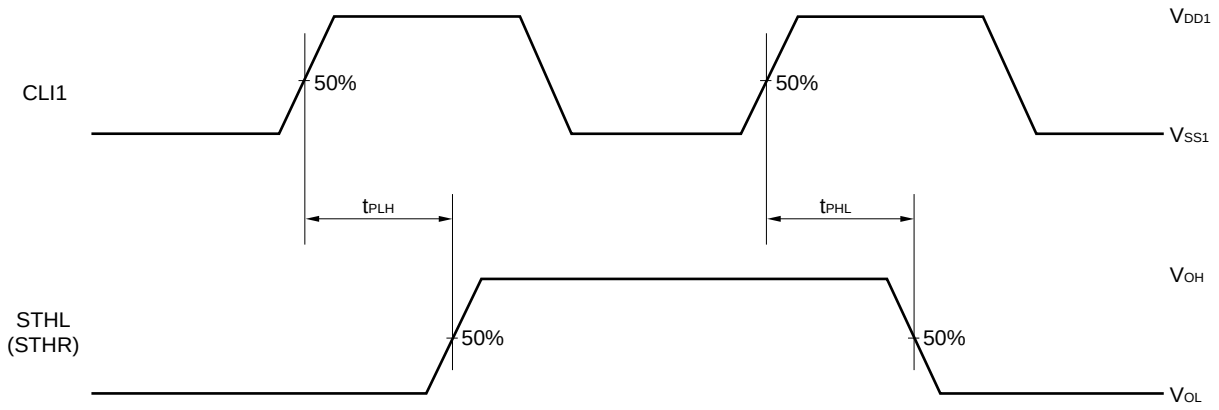
Remark Keep the rise and fall times of the logic input signals to within t_r = t_f = 5 ns (10 to 90%).
As an example, the switching characteristic wave of CLI1 is defined on the next page.

Switching Characteristic Waveform (Simultaneous/successive sampling)

Start Pulse Input Timing

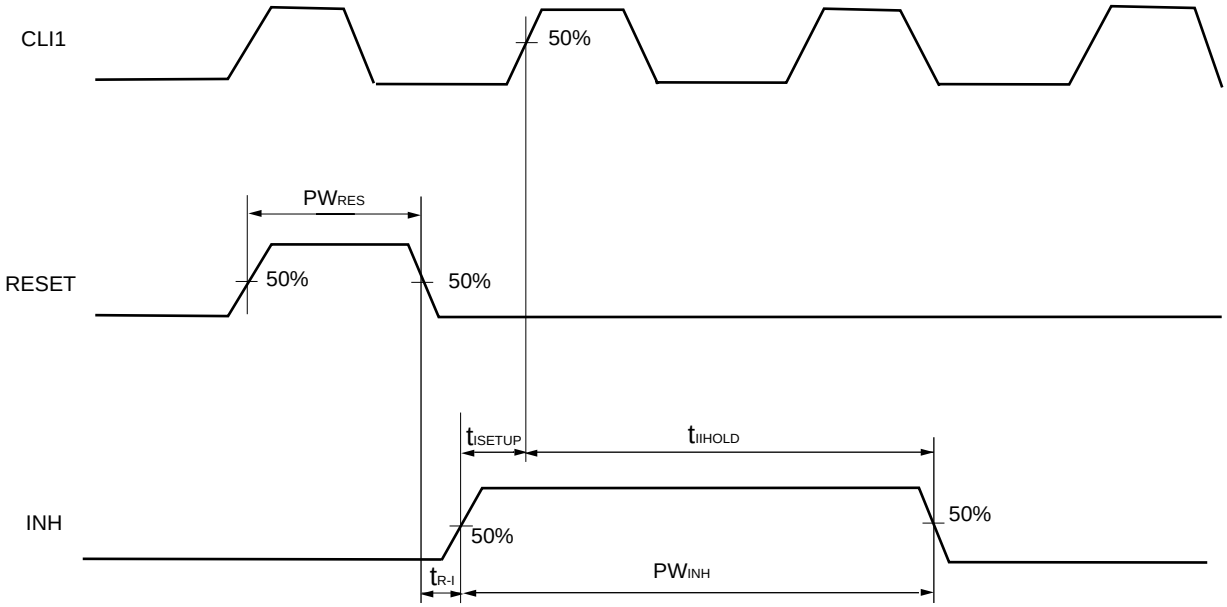


Start Pulse Output Timing



Remark The input/output timing of the start pulse is the same for simultaneous/successive sampling.

RESET INH Pulse Timing



[MEMO]

[MEMO]

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

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