NEC

4-BIT SINGLE-CHIP MICROCONTROLLER WITH
BUILT-IN HARDWARE DEDICATED TO DIGITAL TUNING SYSTEMS

★ The μPD17P709 is produced by replacing the built-in masked ROM of the μPD17704**Note**, μPD17705**Note**, μPD17707, μPD17708, and μPD17709 with a one-time PROM.

The μPD17P709 allows programs to be written once, so that the μPD17P709 is suitable for preproduction in μPD17704, μPD17705, μPD17707, μPD17708, or μPD17709 system development or low-volume production.

When reading this document, also refer to the publications on the μPD17704, μPD17705, μPD17707, μPD17708, or μPD17709.

Note Under development

> **The electrical characteristics (including power supply currents) and PLL analog characteristics of the μPD17P709 differ from those of the μPD17704, μPD17705, μPD17707, μPD17708, and μPD17709. In high-volume application set production, carefully check those differences.**

FEATURES

- Compatible with the μPD17704, μPD17705, μPD17707, μPD17708, and μPD17709
- Built-in one-time PROM   :   32K bytes (16384 $\times$ 16 bits)
- Supply voltage   : V_{DD} = 5 V ±10%

ORDERING INFORMATION

Part number	Package
μPD17P709GC-3B9	80-pin plastic QFP (14 $\times$ 14 mm, 0.65-mm pitch)

The information in this document is subject to change without notice.

The mark ★ shows major revised points.

★ **FUNCTION OVERVIEW**

(1/2)

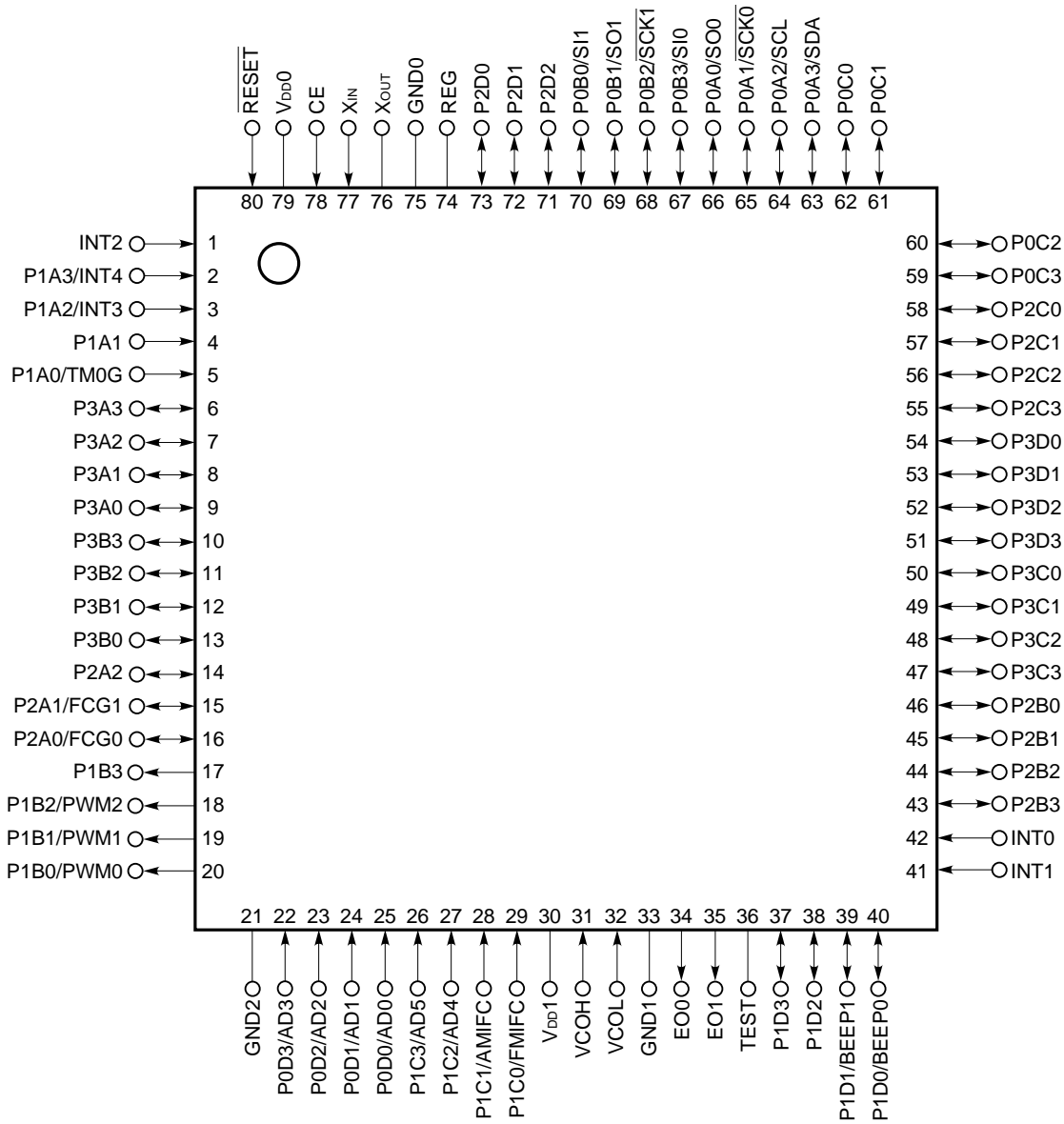| Item \ Product	μPD17704**Note**	μPD17705**Note**	μPD17707	μPD17708	μPD17709	μPD17P709
Program memory (ROM)	8192 × 16 bits (masked ROM)	12288 × 16 bits (masked ROM)		16384 × 16 bits (masked ROM)		16384 × 16 bits (one-time PROM)
General-purpose data memory (RAM)	672 × 4 bits		1120 × 4 bits		1776 × 4 bits	
Instruction execution time	1.78 μs (with 4.5-MHz crystal)					
General-purpose ports	• I/O ports : 46 • Input ports : 12 • Output ports : 4					
Stack level	• Address stack : 15 levels • Interrupt stack : 4 levels • DBF stack : 4 levels (operated by software)					
Interrupt	• External : 6 (CE rising edge and INT0 to INT4) • Internal : 6 (timers 0 to 3, serial interfaces 0 and 1)					
Timers	5 channels • Basic timer (clock: 10, 20, 50, 100 Hz)　　　　　　　　　　: 1 channel • 8-bit timer with gate counter (clock: 1 k, 2 k, 10 k, 100 kHz) : 1 channel • 8-bit timer (clock: 1 k, 2 k, 10 k, 100 kHz)　　　　　　　　: 2 channels • 8-bit timer, also used for PWM (clock: 440 Hz, 4.4 kHz)　　 : 1 channel					
A/D converter	8 bits × 6 channels (Hardware or software mode can be selected.)					
D/A converter (PWM)	3 channels (8-bit or 9-bit resolution, selected by software.) Output frequency : 4.4 kHz, 440 Hz (8-bit PWM) 　　　　　　　　　　2.2 kHz, 220 Hz (9-bit PWM)					
Serial interface	2 systems (3 channels) • 3-wire serial I/O　　　　　　: 2 channels • 2-wire serial I/O/I2C bus　 : 1 channel					
PLL　Frequency division system	• Direct frequency division system (VCOL pin (MF mode) : 0.5 to 3 MHz) • Pulse swallow system　　　　(VCOL pin (HF mode) : 10 to 40 MHz) 　　　　　　　　　　　　　　　(VCOH pin (VHF mode) : 60 to 130 MHz)					
Reference frequency	Can be set to one of 13 frequencies (1, 1.25, 2.5, 3, 5, 6.25, 9, 10, 12.5, 18, 20, 25, or 50 kHz).					
Charge pump	2 error output pins (EO0 and EO1)					
Phase comparator	Unlock detection is enabled by software.					
Intermediate frequency counter	• Intermediate frequency measurement 　P1C0/FMIFC pin : 10 to 11 MHz in FMIF mode 　　　　　　　　　　　　0.4 to 0.5 MHz in AMIF mode 　P1C1/AMIFC pin : 0.4 to 0.5 MHz in AMIF mode • External gate width measurement 　P2A1/FCG1 and P2A0/FCG0 pins					

Note　Under development

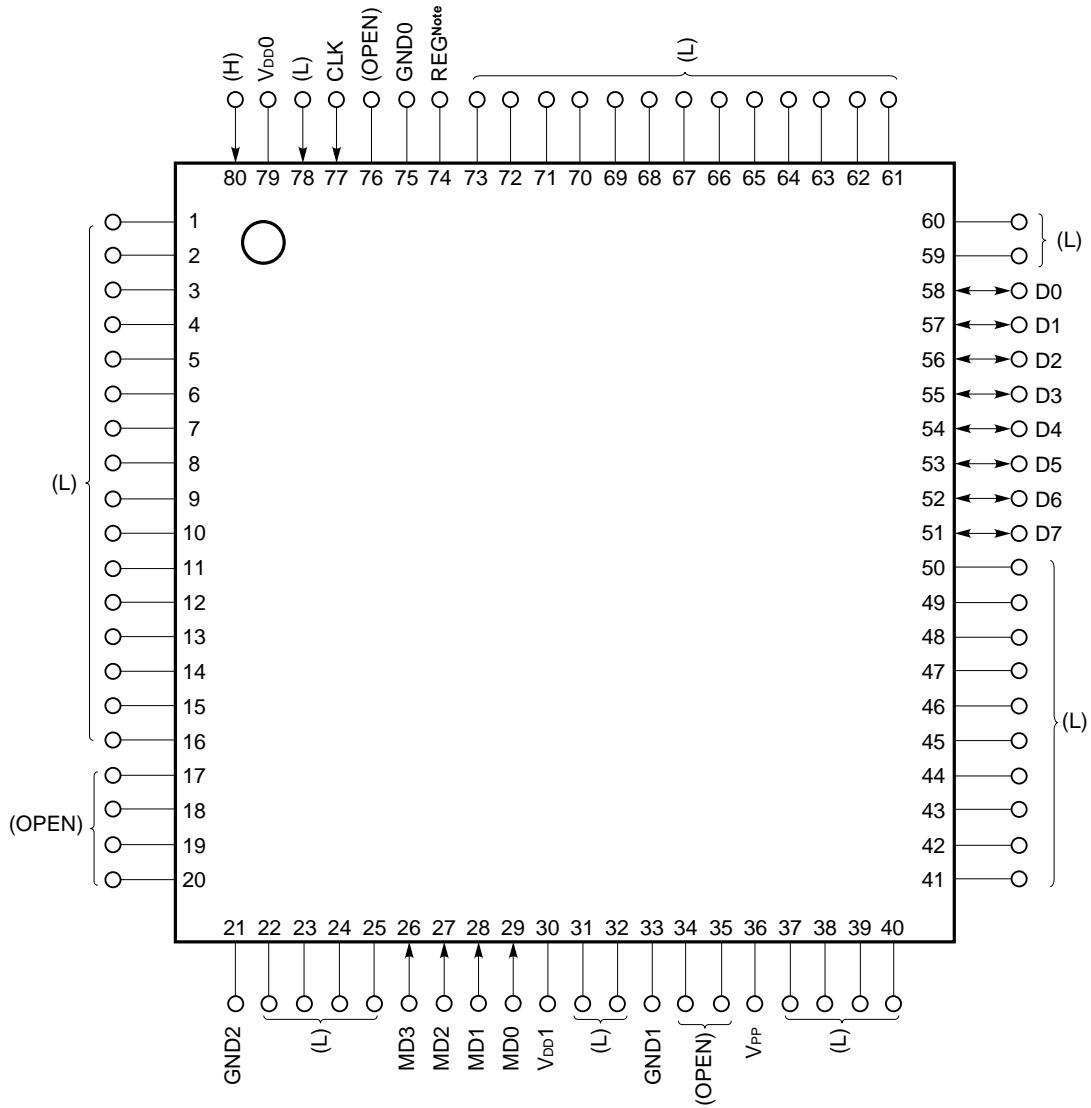| Item \ Product	μPD17704**Note**	μPD17705**Note**	μPD17707	μPD17708	μPD17709	μPD17P709
BEEP output	2 Output frequency : 1 kHz, 3 kHz, 4 kHz, 6.7 kHz (BEEP0 pin) 67 kHz, 200 Hz, 3 kHz, 4 kHz (BEEP1 pin)					

Reset	• Power-on reset (when the power is turned on)
	• Reset using the $\overline{\text{RESET}}$ pin
	• Watchdog timer reset
	  Can be set only once at power-on: 65,536 instructions, 131,072 instructions, or non-use
	  can be selected.
	• Stack pointer overflow/underflow reset
	  Can be set only once at power-on: the interrupt stack or address stack can be selected.
	• CE reset (CE pin: low → high)
	  A CE reset delay timing can be set.
	• Power-failure detection function					

Standby	• Clock stop mode (STOP) • Halt mode (HALT)					
Supply voltage	• PLL operation : V_{DD} = 4.5 to 5.5 V • CPU operation : V_{DD} = 3.5 to 5.5 V					
Package	80-pin plastic QFP (14 × 14 mm, 0.65-mm pitch)					

Note Under development

PIN CONFIGURATION (TOP VIEW)

80-pin plastic QFP (14 × 14 mm, 0.65-mm pitch)
μ**PD17P709GC-3B9**

(1) Normal operation mode

Top row pins (80–61): $\overline{RESET}$ (80), V$_{DD0}$ (79), CE (78), X$_{IN}$ (77), X$_{OUT}$ (76), GND0 (75), REG (74), P2D0 (73), P2D1 (72), P2D2 (71), P0B0/SI1 (70), P0B1/SO1 (69), P0B2/$\overline{SCK1}$ (68), P0B3/SI0 (67), P0A0/SO0 (66), P0A1/$\overline{SCK0}$ (65), P0A2/SCL (64), P0A3/SDA (63), P0C0 (62), P0C1 (61)

Left column pins (1–20):
1 INT2
2 P1A3/INT4
3 P1A2/INT3
4 P1A1
5 P1A0/TM0G
6 P3A3
7 P3A2
8 P3A1
9 P3A0
10 P3B3
11 P3B2
12 P3B1
13 P3B0
14 P2A2
15 P2A1/FCG1
16 P2A0/FCG0
17 P1B3
18 P1B2/PWM2
19 P1B1/PWM1
20 P1B0/PWM0

Right column pins (60–41):
60 P0C2
59 P0C3
58 P2C0
57 P2C1
56 P2C2
55 P2C3
54 P3D0
53 P3D1
52 P3D2
51 P3D3
50 P3C0
49 P3C1
48 P3C2
47 P3C3
46 P2B0
45 P2B1
44 P2B2
43 P2B3
42 INT0
41 INT1

Bottom row pins (21–40): GND2 (21), P0D3/AD3 (22), P0D2/AD2 (23), P0D1/AD1 (24), P0D0/AD0 (25), P1C3/AD5 (26), P1C2/AD4 (27), P1C1/AMIFC (28), P1C0/FMIFC (29), V$_{DD1}$ (30), VCOH (31), VCOL (32), GND1 (33), EO0 (34), EO1 (35), TEST0 (36), P1D3 (37), P1D2 (38), P1D1/BEEP1 (39), P1D0/BEEP0 (40)

(2) PROM programming mode

Note Connect to the same potential as V_DD.

Caution The parentheses above indicate the handling of the pins not used in PROM programming mode.

L   : Connect each pin to GND through a resistor (470 ohms).

H   : Connect each pin to V_DD through a resistor (470 ohms).

OPEN : Leave each pin open.

PIN NAMES

AD0-AD5	: A/D converter inputs	P2B0-P2B3	: Port 2B
AMIFC	: AM frequency counter input	P2C0-P2C3	: Port 2C
BEEP0, BEEP1	: Beep outputs	P2D0-P2D2	: Port 2D
CE	: Chip enable	P3A0-P3A3	: Port 3A
CLK	: Address update clock input	P3B0-P3B3	: Port 3B
D0-D7	: Data I/O	P3C0-P3C3	: Port 3C
EO0, EO1	: Error outputs	P3D0-P3D3	: Port 3D
FCG0, FCG1	: Frequency counter gate inputs	REG	: CPU regulator
FMIFC	: FM frequency counter input	$\overline{\text{RESET}}$	: Reset input
GND0-GND2	: Ground 0 to 2	$\overline{\text{SCK0}}$, $\overline{\text{SCK1}}$	: 3-wire serial clock I/O
INT0-INT4	: External interrupt inputs	SCL	: 2-wire serial clock I/O
MD0-MD3	: Operating mode selection	SDA	: 2-wire serial data I/O
PWM0-PWM2	: D/A converter outputs	SI0, SI1	: 3-wire serial data input
P0A0-P0A3	: Port 0A	SO0, SO1	: 3-wire serial data output
P0B0-P0B3	: Port 0B	TEST	: Test input
P0C0-P0C3	: Port 0C	TM0G	: Timer 0 gate input
P0D0-P0D3	: Port 0D	VCOH	: Local oscillation high input
P1A0-P1A3	: Port 1A	VCOL	: Local oscillation low input
P1B0-P1B3	: Port 1B	$V_{DD}0$, $V_{DD}1$	: Power supply
P1C0-P1C3	: Port 1C	V_{PP}	: Program voltage application
P1D0-P1D3	: Port 1D	X_{IN}, X_{OUT}	: Main clock oscillation
P2A0-P2A2	: Port 2A		

BLOCK DIAGRAM
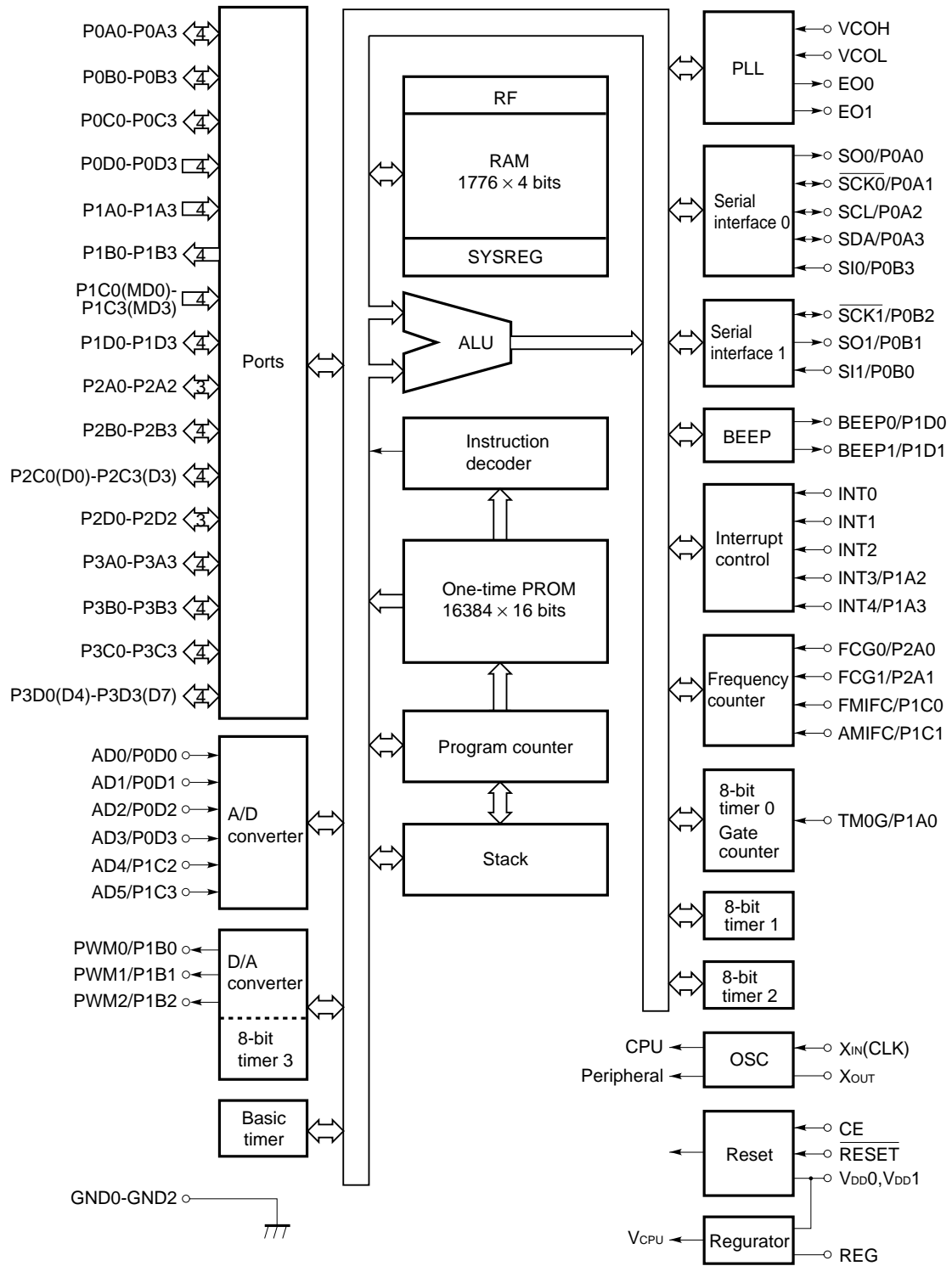
Remark Pins enclosed in parentheses are used in PROM programming mode.

CONTENTS

★ **1. PIN FUNCTIONS**

1.1 NORMAL OPERATION MODE

Pin No.	Symbol	Function	Output format
1 41 42	INT2 INT1 INT0	Edge-detected vectored interrupt. Either a rising edge or falling edge can be selected.	—

2
3
4
5
	P1A3/INT4
	P1A2/INT3
	P1A1
	P1A0/TM0G
		Port 1A. External interrupt request signal input and event signal input
		• P1A3-P1A0
		  • 4-bit input port
		• INT4, INT3
		  • Edge-detected vectored interrupt
		• TM0G
		  • Gate input for 8-bit timer 0
			—

	When reset			When the clock is stopped
	Power-on reset	WDT&SP reset	CE reset	
	Input (P1A3-P1A0)	Input (P1A3-P1A0)	Held	Held

Pin No.	Symbol	Function	Output format
6 to 9	P3A3 to P3A0	4-bit I/O port. Input/output can be specified in 4-bit units.	CMOS push-pull

	When reset			When the clock is stopped
	Power-on reset	WDT&SP reset	CE reset	
	Input	Input	Held	Held

Pin No.	Symbol	Function	Output format
10 to 13	P3B3 to P3B0	4-bit I/O port. Input/output can be specified in 4-bit units.	CMOS push-pull

	When reset			When the clock is stopped
	Power-on reset	WDT&SP reset	CE reset	
	Input	Input	Held	Held

Pin No.	Symbol	Function	Output format

14
15
16
	P2A2
	P2A1/FCG1
	P2A0/FCG0
		Port 2A. External gate counter input
		• P2A2-P2A0
		  • 3-bit I/O port
		  • Input/output can be specified bit by bit.
		• FCG1, FCG0
		  • External gate counter input
			CMOS push-pull

	When reset			When the clock is stopped
	Power-on reset	WDT&SP reset	CE reset	
	Input (P2A2-P2A0)	Input (P2A2-P2A0)	Held (P2A2-P2A0)	Held (P2A2-P2A0)

Pin No.	Symbol	Function				Output format
17 to 20	P1B3 P1B2/PWM2 to P1B0/PWM0	Port 1B. D/A converter output • P1B3-P1B0 　• 4-bit output port • PWM2-PWM0 　• 8-bit or 9-bit D/A converter output				N-ch open-drain (12-V withstand voltage)
		When reset			When the clock is stopped	
		Power-on reset	WDT&SP reset	CE reset		
		Low-level output (P1B3-P1B0)	Low-level output (P1B3-P1B0)	Held	Held (P1B3-P1B0)	
21 33 75	GND2 GND1 GND0	Ground				—
22 to 25	P0D3/AD3 to P0D0/AD0	Port 0D. A/D converter input • P0D3-P0D0 　• 4-bit input port 　• A pull-down resistor can be set bit by bit. • AD3-AD0 　• Analog input for 8-bit-resolution A/D converter				—
		When reset			When the clock is stopped	
		Power-on reset	WDT&SP reset	CE reset		
		Input with pull-down resistors (P0D3-P0D0)	Input with pull-down resistors (P0D3-P0D0)	Held	Held	
26 27 28 29	P1C3/AD5 P1C2/AD4 P1C1/AMIFC P1C0/FMIFC	Port 1C. A/D converter input and IF counter input • P1C3-P1C0 　• 4-bit input port • AD5, AD4 　• Analog input for 8-bit-resolution A/D converter • FMIFC, AMIFC 　• Frequency counter input				—
		When reset			When the clock is stopped	
		Power-on reset	WDT&SP reset	CE reset		
		Input (P1C3-P1C0)	Input (P1C3-P1C0)	• P1C3/AD5, P1C2/AD4 Held • P1C1/AMIFC, P1C0/FMIFC Input (P1C1, P1C0)	• P1C3/AD5, P1C2/AD4 Held • P1C1/AMIFC, P1C0/FMIFC Input (P1C1, P1C0)	

Pin No.	Symbol	Function	Output format
30 79	VDD1 VDD0	Power supply. Apply the same voltage to the VDD1 and VDD0 pins. • When the CPU and peripheral functions are operating: 4.5 to 5.5 V • When only the CPU is operating: 3.5 to 5.5 V • When the clock is stopped: 2.2 to 5.5 V	—

31
32
	VCOH
	VCOL
		PLL local oscillation (VCO) frequency input
		 • VCOH
		  • Active when VHF mode is selected by software. Otherwise, pulled down.
		 • VCOL
		  • Active when HF or MW mode is selected by software. Otherwise, pulled down.
		
		Inputs to these pins are to be AC-amplified. Cut, therefore, the DC components in the input signals by using capacitors.
			—

34 35	EO0 EO1	Output from the charge pump of the PLL frequency synthesizer. The result of phase comparison between the divided local oscillation frequency and reference frequency is output. <table><tr><td colspan="3">When reset</td><td rowspan="2">When the clock is stopped</td></tr><tr><td>Power-on reset</td><td>WDT&SP reset</td><td>CE reset</td></tr><tr><td>High-impedance output</td><td>High-impedance output</td><td>High-impedance output</td><td>High-impedance output</td></tr></table>	CMOS tristate
36	TEST	Test input pin. Be sure to connect it to GND.	—

37
38
39
40
	P1D3
	P1D2
	P1D1/BEEP1
	P1D0/BEEP0
		Port 1D. BEEP output
		 • P1D3-P1D0
		  • 4-bit I/O port
		  • Input/output can be specified bit by bit.
		 • BEEP1, BEEP0
		  • BEEP output
		
		<table><tr><td colspan="3">When reset</td><td rowspan="2">When the clock is stopped</td></tr><tr><td>Power-on reset</td><td>WDT&SP reset</td><td>CE reset</td></tr><tr><td>Input
		(P1D3-P1D0)</td><td>Input
		(P1D3-P1D0)</td><td>Held
		(P1D3-P1D0)</td><td>Held
		(P1D3-P1D0)</td></tr></table>
			CMOS push-pull

43 to 46	P2B3 to P2B0	4-bit I/O port. Input/output can be specified bit by bit. <table><tr><td colspan="3">When reset</td><td rowspan="2">When the clock is stopped</td></tr><tr><td>Power-on reset</td><td>WDT&SP reset</td><td>CE reset</td></tr><tr><td>Input</td><td>Input</td><td>Held</td><td>Held</td></tr></table>	CMOS push-pull
47 to 50	P3C3 to P3C0	4-bit I/O port. Input/output can be specified in 4-bit units. <table><tr><td colspan="3">When reset</td><td rowspan="2">When the clock is stopped</td></tr><tr><td>Power-on reset</td><td>WDT&SP reset</td><td>CE reset</td></tr><tr><td>Input</td><td>Input</td><td>Held</td><td>Held</td></tr></table>	CMOS push-pull

Pin No.	Symbol	Function				Output format
51 to 54	P3D3 to P3D0	4-bit I/O port. Input/output can be specified in 4-bit units.				CMOS push-pull
			When reset		When the clock is stopped	
		Power-on reset	WDT&SP reset	CE reset		
		Input	Input	Held	Held	
55 to 58	P2C3 to P2C0	4-bit I/O port. Input/output can be specified bit by bit.				CMOS push-pull
			When reset		When the clock is stopped	
		Power-on reset	WDT&SP reset	CE reset		
		Input	Input	Held	Held	
59 to 62	P0C3 to P0C0	4-bit I/O port. Input/output can be specified bit by bit.				CMOS push-pull
			When reset		When the clock is stopped	
		Power-on reset	WDT&SP reset	CE reset		
		Input	Input	Held	Held	
63 64	P0A3/SDA P0A2/SCL	P0A or P0B. Serial interface I/O • P0A3-P0A0 • 4-bit I/O port • Input/output can be specified bit by bit. • P0B3-P0B0 • 4-bit I/O port • Input/output can be specified bit by bit. • SDA, SCL • Serial data and serial clock I/O when the 2-wire serial I/O or I^{2}C bus of serial interface 0 is selected. • $\overline{SCK0}$, SO0, SI0 • Serial clock I/O, serial data output, and serial data input when the 3-wire serial I/O of serial interface 0 is selected. • $\overline{SCK1}$, SO1, SI1 • Serial clock I/O, serial data output, and serial data input when the 3-wire serial I/O of serial interface 1 is selected.				N-ch open-drain
65 66 67 68 69 70	P0A1/$\overline{SCK0}$ P0A0/SO0 P0B3/SI0 P0B2/$\overline{SCK1}$ P0B1/SO1 P0B0/SI1					CMOS push-pull
			When reset		When the clock is stopped	
		Power-on reset	WDT&SP reset	CE reset		
		Input (P0A3-P0A0 P0B3-P0B0)	Input (P0A3-P0A0 P0B3-P0B0)	Held (P0A3-P0A0 P0B3-P0B0)	Held (P0A3-P0A0 P0B3-P0B0)	
71 to 73	P2D2 to P2D0	3-bit I/O port. Input/output can be specified bit by bit.				CMOS push-pull
			When reset		When the clock is stopped	
		Power-on reset	WDT&SP reset	CE reset		
		Input	Input	Held	Held	

Pin No.	Symbol	Function	Output format
74	REG	CPU regulator. Use 0.1-μF capacitor to connect it to GND.	—
76 77	X$_{OUT}$ X$_{IN}$	A crystal is connected to these pins.	—

78	CE	Input for device operation selection, CE reset, and interrupt signals
		• Device operation selection
		  When CE is high, the PLL frequency synthesizer can be operated.
		  When CE is low, the PLL frequency synthesizer is automatically
		  disabled by the device.
		• CE reset
		  Setting CE from low to high resets the device upon the detection of a
		  rising edge of the internal basic timer setting pulse.
		  A reset timing delay can also be specified.
		• Interrupt
		  A vectored interrupt occurs upon the detection of a falling edge of the
		  input signal.
			—

80	$\overline{\text{RESET}}$	Reset input	—

1.2 PROM PROGRAMMING MODE

Pin No.	Symbol	Function	Output format
26 to 29	MD3 to MD0	Input for operating mode selection for program memory write, read, or verification	—
21 33 75	GND2 GND1 GND0	Ground	—
36	V$_{PP}$	Pin to which program voltage is applied during program memory write, read, or verification. +12.5 V is applied.	—
30 79	V$_{DD}$1 V$_{DD}$0	Power supply pins. +6 V is applied during program memory write, read, or verification.	—
51 to 58	D7 to D0	8-bit data I/O for program memory write, read, or verification	CMOS push-pull
77	CLK	Clock input for address updating during program memory write, read, or verification	—

Remark The pins other than those listed above are not used in PROM programming mode. For the handling
of the unused pins, see **PIN CONFIGURATION**, **(2) PROM programming mode**.

★ **1.3 EQUIVALENT CIRCUIT OF PINS**

(1) P0A (P0A1/$\overline{\text{SCK0}}$, P0A0/SO0)
    P0B (P0B3/SI0, P0B2/$\overline{\text{SCK1}}$, P0B1/SO1, P0B0/SI1)
    P0C (P0C3, P0C2, P0C1, P0C0)
    P1D (P1D3, P1D2, P1D1/BEEP1, P1D0/BEEP0)
    P2A (P2A2, P2A1/FCG1, P2A0/FCG0)
    P2B (P2B3, P2B2, P2B1, P2B0)
    P2C (P2C3, P2C2, P2C1, P2C0)
    P2D (P2D2, P2D1, P2D0)   **(I/O)**
    P3A (P3A3, P3A2, P3A1, P3A0)
    P3B (P3B3, P3B2, P3B1, P3B0)
    P3C (P3C3, P3B2, P3C1, P3C0)
    P3D (P3D3, P3D2, P3D1, P3D0)
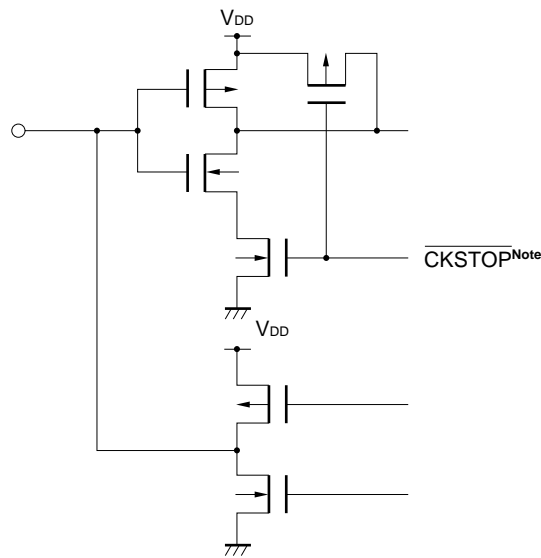
Note In this circuit, a current drained by noise does not increase even if the circuit is in the floating state, because of the internal signal being output when the clock stop instruction is executed.

(2) P0A (P0A3/SDA, P0A2/SCL) (I/O)
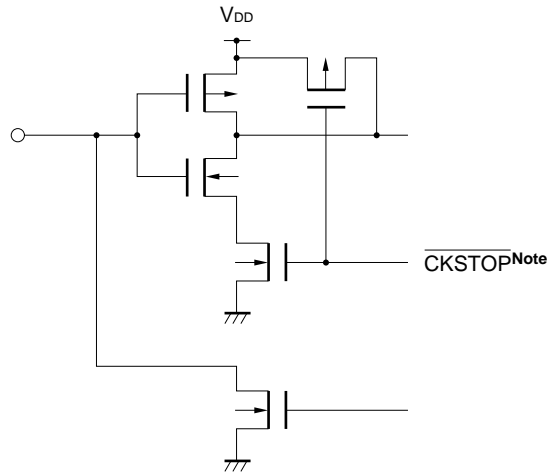
Note   In this circuit, a current drained by noise does not increase even if the circuit is in the floating state, because of the internal signal being output when the clock stop instruction is executed.

(3) P1B (P1B3, P1B2/PWM2, P1B1/PWM1, P1B0/PWM0) (Output)
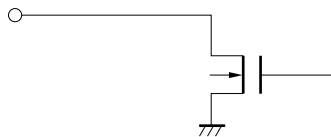
(4) P0D (P0D3/AD3, P0D2/AD2, P0D1/AD1, P0D0/AD0) (Input)
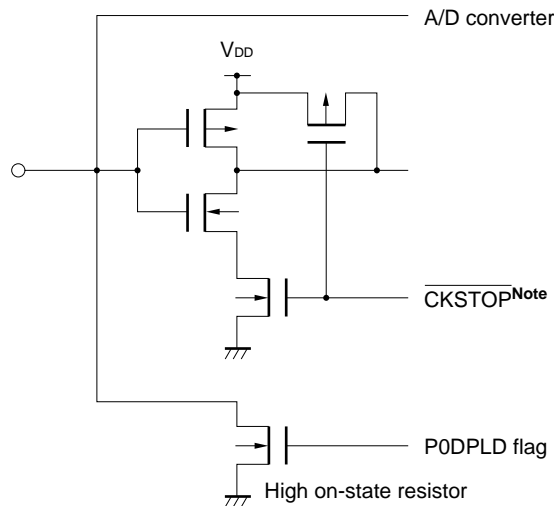
Note   In this circuit, a current drained by noise does not increase even if the circuit is in the floating state, because of the internal signal being output when the clock stop instruction is executed.

(5) P1A (P1A1) (Input)
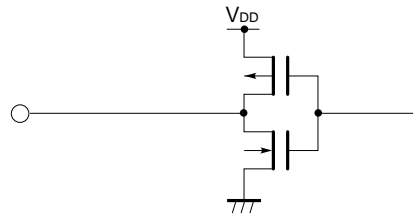
(6) P1C (P1C3/AD5, P1C2/AD4) (Input)
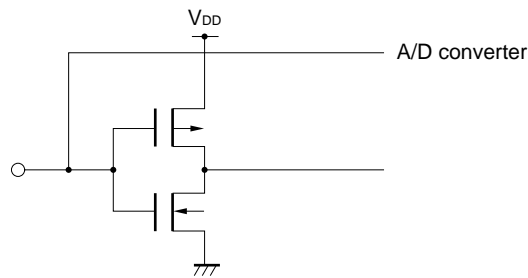
(7) P1C (P1C1/AMIFC, P1C0/FMIFC) (Input)
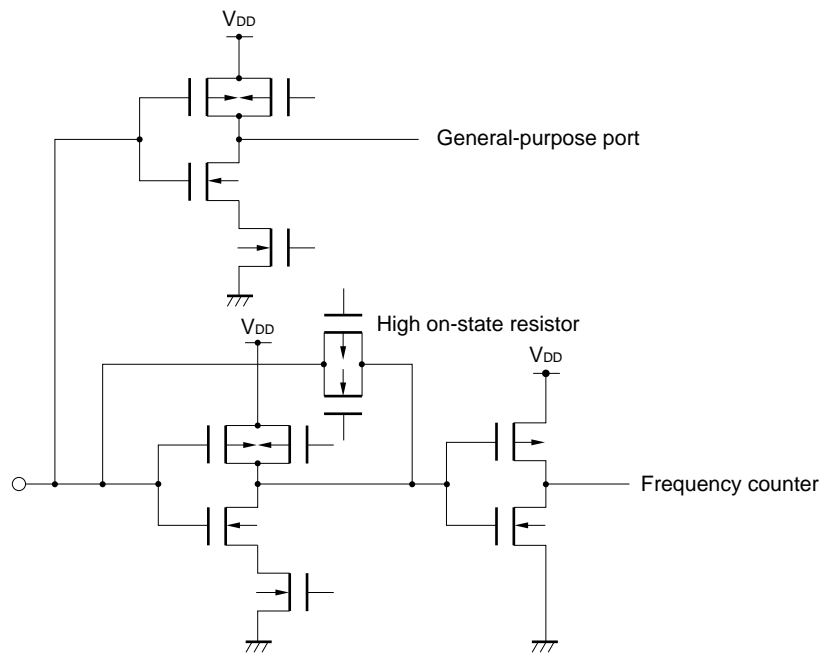
(8) **CE**
  RESET
  INT0, INT1, INT2
  P1A (P1A3/INT4, P1A2/INT3, P1A0/TM0G)
  (Schmitt-triggered input)
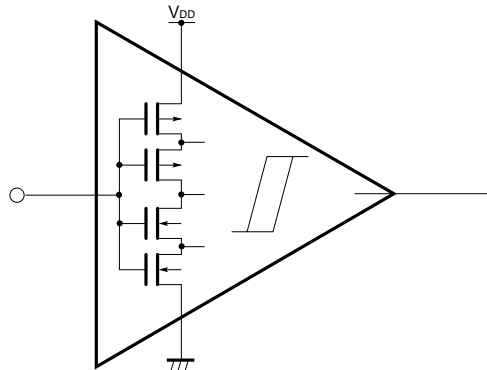
(9) **X_OUT (Output), X_IN (Input)**
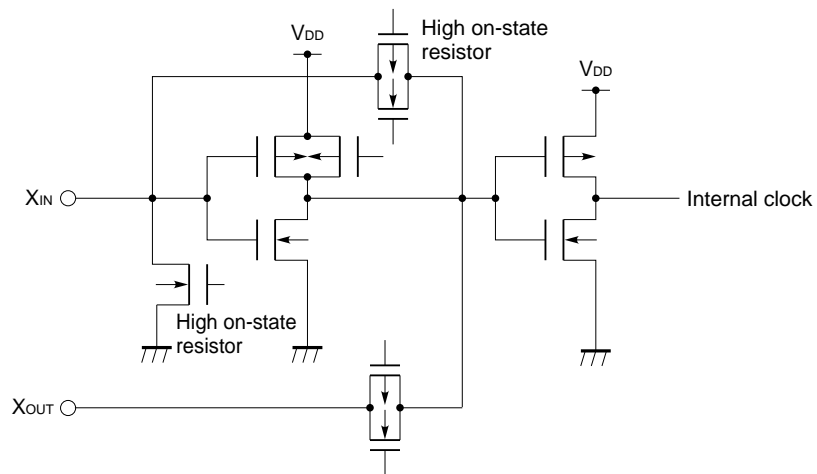
(10) **EO1, EO0 (Output)**
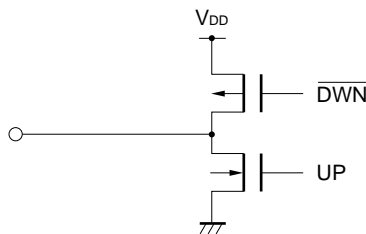
(11) VCOH, VCOL (Input)
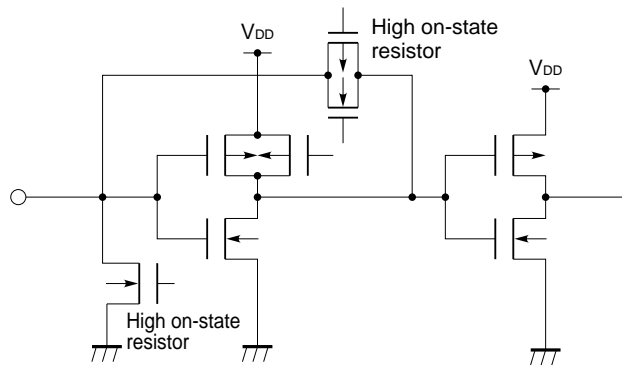
1.4 HANDLING UNUSED PINS

The unused pins should be handled as indicated in Table 1-1.

Table 1-1 Handling Unused Pins   (1/2)

Pin		I/O format	Recommended handling
Port pins	P0D3/AD3-P0D0/AD0	Input	Connect each pin to GND through a resistor.**Note 1**
	P1C3/AD5 P1C2/AD4		
	P1C1/AMIFC**Note 2** P1C0/FMIFC**Note 2**		Specify as a port and connect each pin to V$_{DD}$ or GND through a resistor.**Note 1**
	P1A3/INT4 P1A2/INT3 P1A1 P1A0/TM0G		Connect each pin to GND through a resistor.**Note 1**
	P1B3 P1B2/PWM2-P1B0/PWM0	N-ch open-drain output	Specify low output, in the software, and leave open.
	P0A3/SDA P0A2/SCL P0A1/$\overline{\text{SCK0}}$ P0A0/SO0 P0B3/SI0 P0B2/$\overline{\text{SCK1}}$ P0B1/SO1 P0B0/SI1	I/O**Note 3**	Specify as a general-purpose input port, in the software, and connect each pin to V$_{DD}$ or GND through a resistor.**Note 1**
	P0C3-P0C0		
	P1D3 P1D2 P1D1/BEEP1 P1D0/BEEP0 P2A2 P2A1/FCG1 P2A0/FCG0		
	P2B3-P2B0		
	P2C3-P2C0		
	P2D2-P2D0		

★ (beside P1C1/AMIFC row)

Notes 1. When making an external connection to V$_{DD}$ with a pull-up resistor, or to GND with a pull-down resistor, note the following: If the resistance of the pull-up or pull-down resistor is too high, the pin approaches the high impedance state, thus increasing the through current drawn by the port. In general, pull-up and pull-down resistors should have a resistance of between 20 and 50 kilohms, depending on the application circuit.

2. Do not specify AMIFC or FMIFC. If AMIFC or FMIFC is specified, current drain increases.

3. I/O ports become general-purpose input ports upon power-on reset, reset by the $\overline{\text{RESET}}$ pin, watchdog timer reset, or stack overflow/underflow reset.

(2/2)

	Pin	I/O format	Recommended handling
Port pins	P3A3-P3A0	I/O**Note 2**	Specify as a general-purpose input port, in the software, and connect each pin to V$_{DD}$ or GND through a resistor.**Note 1**
	P3B3-P3B0		
	P3C3-P3C0		
	P3D3-P3D0		
Other than port pins	CE	Input	Connect to V$_{DD}$ through a resistor.**Note 1**
	EO1 EO0	Output	Leave each pin open.
	INT0-INT2	Input	Connect each pin to GND through a resistor.**Note 1**
	$\overline{\text{RESET}}$	Input	Connect to V$_{DD}$ through a resistor.**Note 1**
	TEST	—	Connect directly to GND.**Note 1**
	VCOH VCOL	Input	Disable PLL, in the program, and leave each pin open.

Notes 1. When making an external connection to V$_{DD}$ with a pull-up resistor, or to GND with a pull-down resistor, note the following: If the resistance of the pull-up or pull-down resistor is too high, the pin approaches the high impedance state, thus increasing the through current drawn by the port. In general, pull-up and pull-down resistors should have a resistance of between 20 and 50 kilohms, depending on the application circuit.

★   **2.** I/O ports become general-purpose input ports upon power-on reset, reset by the $\overline{\text{RESET}}$ pin, watchdog timer reset, or stack overflow/underflow reset.

★ **1.5 NOTES ON USE OF THE CE, INT0-INT4, AND $\overline{\text{RESET}}$ PINS (ONLY IN NORMAL OPERATION MODE)**

The CE, INT0-INT4, and $\overline{\text{RESET}}$ pins can be used as the test mode selection pin for testing the internal operation of the μPD17P709 (IC test), besides the usage shown in **Section 1.1**.

Applying a voltage exceeding V_{DD} to the CE, INT0-INT4, or $\overline{\text{RESET}}$ pin causes the μPD17P709 to enter test mode. When noise exceeding V_{DD} comes in during normal operation, the device may not operate normally.

For example, if the wiring from the CE, INT0-INT4, or $\overline{\text{RESET}}$ pin is too long, noise may be induced on the wiring, causing this mode switching.

When installing the wiring, lay the wiring in such a way that noise is suppressed as much as possible. If noise yet arises, use an external part to suppress it as shown below.

- **Connect a diode with low V_F between the pin and V_{DD}.**
- **Connect a capacitor between the pin and V_{DD}.**
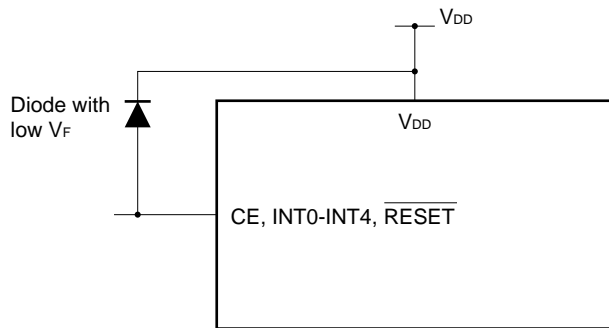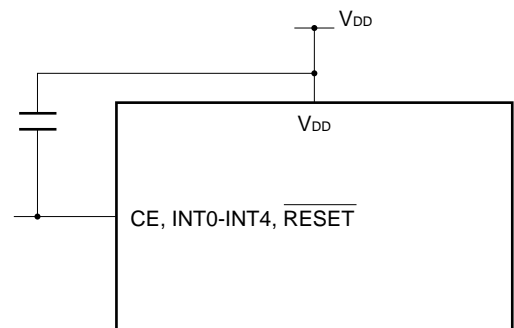
★ **1.6 NOTES ON USE OF THE TEST PIN (ONLY IN NORMAL OPERATION MODE)**

Applying V_{DD} to the TEST pin causes the μPD17P709 to enter test mode or program memory write/verify mode. Keep the wiring as short as possible and connect the TEST pin directly to the GND pin.

When the wiring between the TEST pin and GND pin is too long or external noise enters the TEST pin, a voltage difference may occur between the TEST pin and GND pin. When this happens, your program may malfunction.
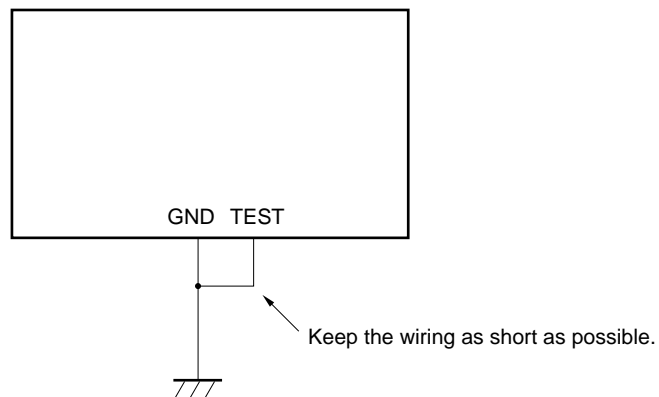
2. ONE-TIME PROM (PROGRAM MEMORY) WRITE, READ, AND VERIFICATION

The program memory built into the μPD17P709 is a one-time PROM (16384 $\times$ 16 bits) that is electrically writable. In normal operation, this PROM is accessed on a 16-bit word basis. During program memory write, read, and verification, the PROM is accessed on an 8-bit word basis. The higher 8 bits of a 16-bit word are located at an even-numbered address, and the lower 8 bits are located at an odd-numbered address.

For PROM write, read, and verification, PROM programming mode must be specified, and the pins listed in Table 2-1 are used.

In this case, address input is not used. Instead, clock input on the CLK pin is used to update addresses.

Table 2-1   Pins Used for Program Memory Write, Read, and Verification

Pin	Function
V_{PP}	Used to apply the program voltage (+12.5 V)
CLK	Used to apply an address update clock
MD0-MD3	Used to select an operating mode
D0-D7	Used to input/output 8-bit data
$V_{DD}0$, $V_{DD}1$	Used to apply the power supply voltage (+6 V)

For writing to the built-in PROM, a specified PROM programmer and dedicated programmer adapter are to be used. The following PROM programmers and programmer adapters are usable:

★

PROM programmer	Programmer adapter
PG-1500 + PA-17KDZ (adapter for PG-1500)	PA-17P709GC

Third-party PROM programmers are also available: For example, AF-9703, AF-9704, AF-9705, and AF-9706 (manufactured by Ando Electric Co., Ltd.)

Fig. 2-1   PA17P709GC and PA-17KDZ

PA-17P709GC

PA-17KDZ

To PG-1500
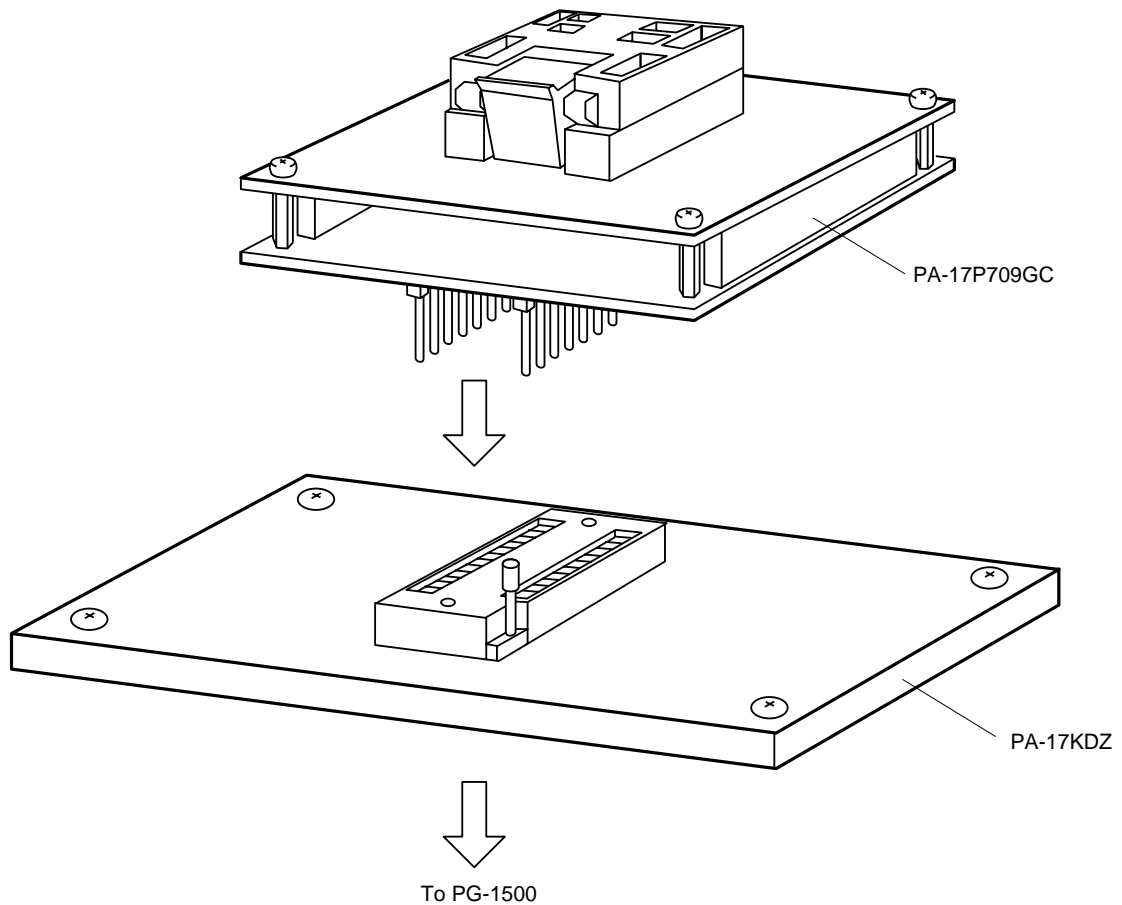
2.1   OPERATING MODES FOR PROGRAM MEMORY WRITE, READ, AND VERIFICATION

The μPD17P709 is placed in program memory write, read, and verify mode when +6 V is applied to the V_DD pin, and +12.5 V to the V_PP pin.

In this mode, one of the operating modes indicated in Table 2-2 is set, depending on the setting of the MD0 to MD3 pins.

The input pins that are not used for program memory write, read, and verification are connected to GND through a pull-down resistor (470 ohms). (See **PIN CONFIGURATION**, **(2) PROM programming mode**.)

Table 2-2   Operating Modes for Program Memory Write, Read, and Verication

Operating mode specification						Operating mode
V_PP	V_DD	MD0	MD1	MD2	MD3	
+12.5V	+6V	H	L	H	L	Program memory address zero-clear mode
		L	H	H	H	Write mode
		L	L	H	H	Read/verify mode
		H	X	H	H	Program inhibit mode

Remark   X: L or H

2.2 PROGRAM MEMORY WRITE PROCEDURE

The program memory write procedure is described below. The procedure allows high-speed write operation.

(1)   Connect the unused pins to GND through pull-down resistors. The CLK pin must be low.

(2)   Apply 5 V to the V_{DD} pin. The V_{PP} pin must be low.

(3)   Apply 5 V to the V_{PP} pin after waiting 10 μs.

(4)   Specify program memory address zero-clear mode, using the mode setting pins.

(5)   Apply 6 V to V_{DD}, and 12.5 V to V_{PP}.

(6)   Program inhibit mode

(7)   Write data in 1-ms write mode.

(8)   Program inhibit mode

(9)   Verify mode. When data has been written normally, proceed to step (10). When data has not been written normally, repeat steps (7) to (9).

(10)   Perform an additional write operation ((X: Number of write operations performed in steps (7) to (9)) $\times$ 1 ms).

(11)   Program inhibit mode

(12)   Apply four pulses to the CLK pin to increment the program memory address by 1.

(13)   Repeat steps (7) to (12) until the last address is reached.

(14)   Program memory address zero-clear mode

(15)   Change the voltage applied to the V_{DD} and V_{PP} pins to 5 V.

(16)   Turn off the power.

Steps (2) to (12) are illustrated below.
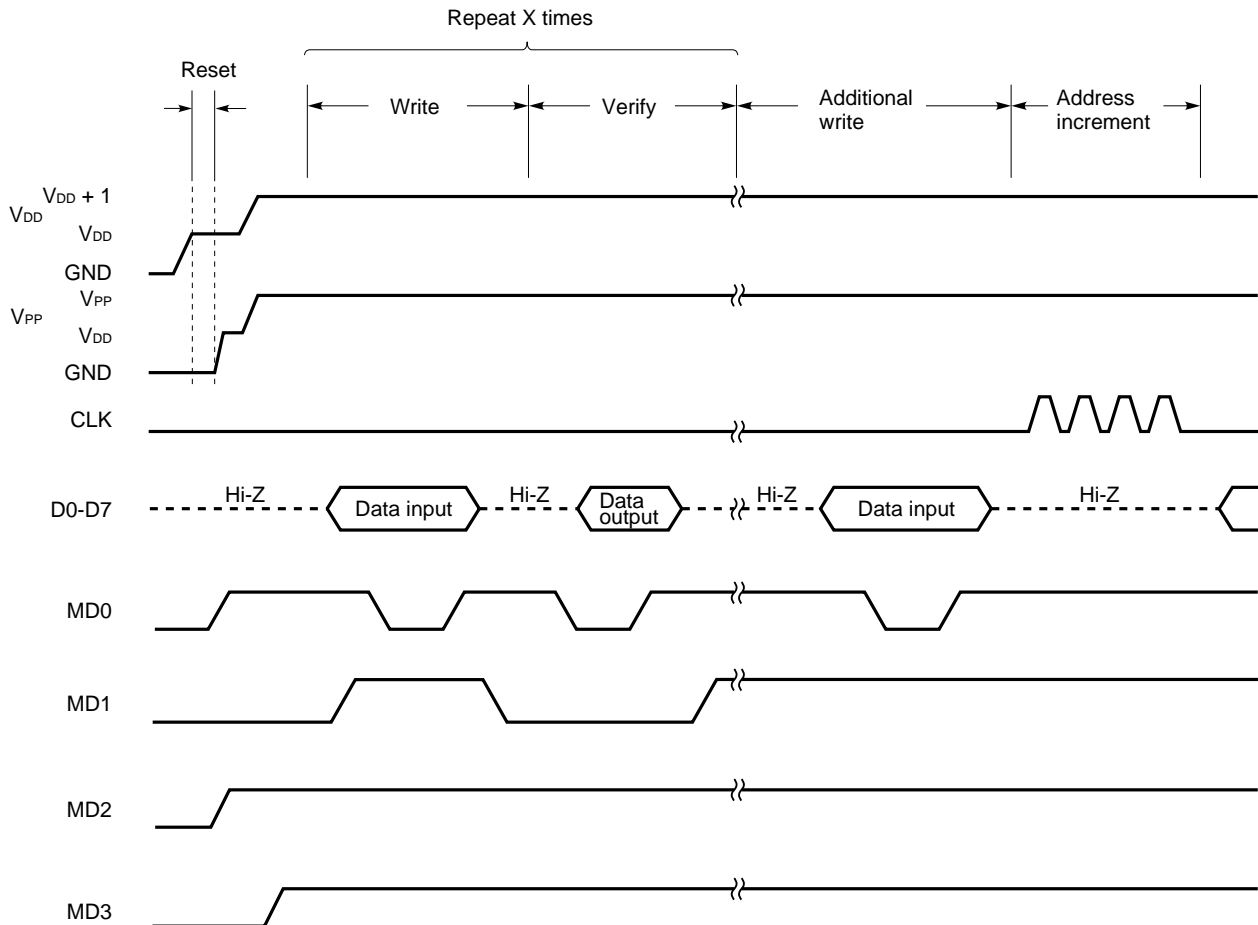
2.3 PROGRAM MEMORY READ PROCEDURE

(1) Connect the unused pins to GND through pull-down resistors. The CLK pin must be low.

(2) Apply 5 V to the V_{DD} pin. The V_{PP} pin must be low.

(3) Apply 5 V to the V_{PP} pin after waiting 10 μs.

(4) Specify program memory address zero-clear mode, using the mode setting pins.

(5) Apply 6 V to V_{DD}, and 12.5 V to V_{PP}.

(6) Program inhibit mode

(7) Verify mode. When a clock pulse signal is applied to the CLK pin, data is output for each address every four clock pulses.

(8) Program inhibit mode

(9) Program memory address zero-clear mode

(10) Change the voltage applied to the V_{DD} and V_{PP} pins to 5 V.

(11) Turn off the power.

Steps (2) to (9) are illustrated below.

3. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

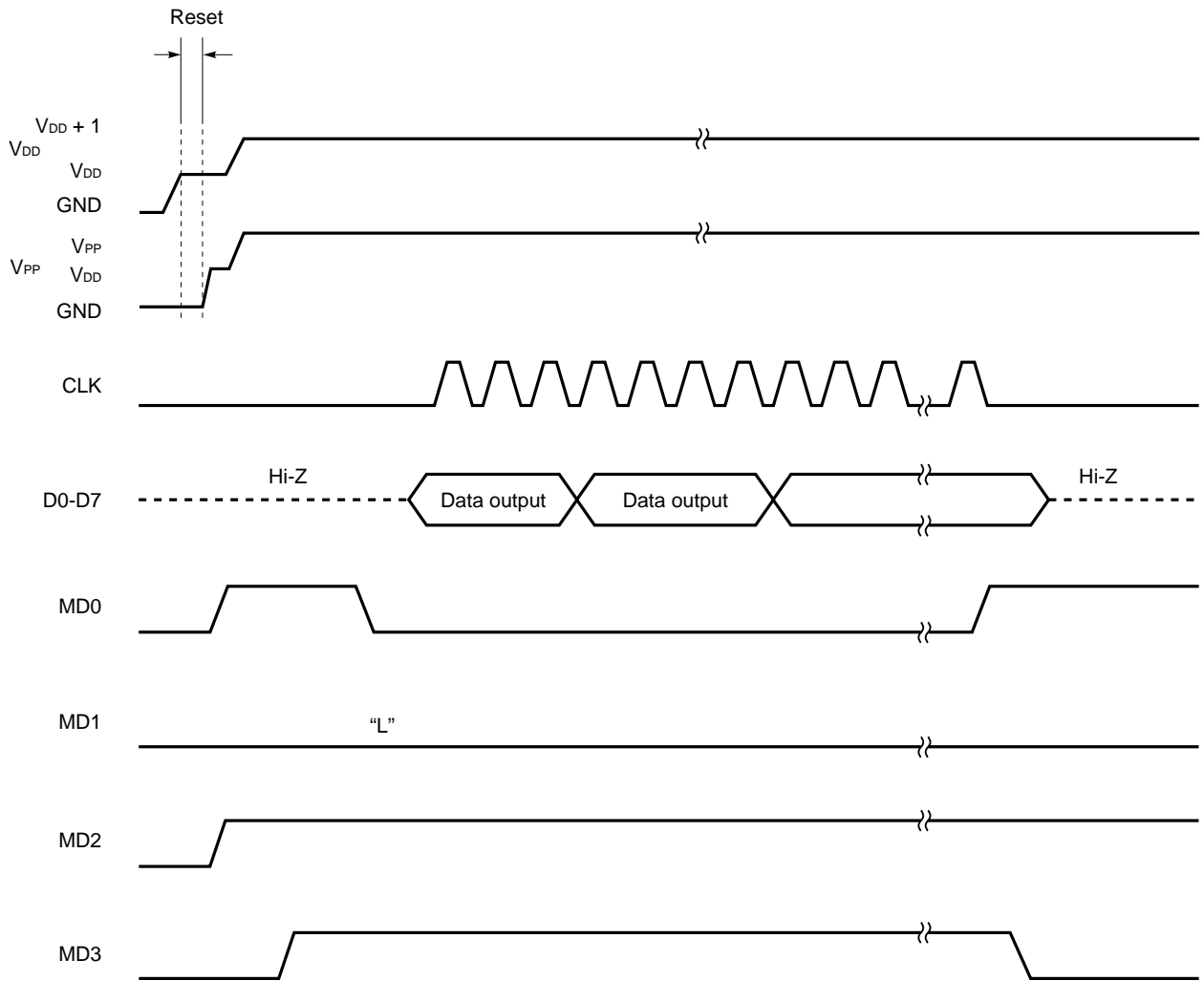| Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}		−0.3 to +6.0	V
PROM program voltage	V_{PP}		−0.3 to +13.5	V
Input voltage	V_I	At other than CE, INT0-INT4, and $\overline{RESET}$ pins	−0.3 to V_{DD} + 0.3	V
		CE, INT0-INT4, and $\overline{RESET}$ pins	−0.3 to V_{DD} + 0.6	V
Output voltage	V_O	At other than P1B0-P1B3	−0.3 to V_{DD} + 0.3	V
High output current	I_{OH}	At one pin	−8.0	mA
		Total for P2A0-P2A2, P3A0-P3A3, and P3B0-P3B3	−15.0	mA
		Total for P0A0-P0A3, P0B0-P0B3, P0C0-P0C3, P1D0-P1D3, P2B0-P2B3, P2C0-P2C3, P2D0-P2D2, P3C0-P3C3, and P3D0-P3D3	−25.0	mA
Low output current	I_{OL}	At one pin of P1B0-P1B3	12.0	mA
		At one pin of other than P1B0-P1B3	8.0	mA
		Total for P2A0-P2A2, P3A0-P3A3, and P3B0-P3B3	15.0	mA
		Total for P0A0-P0A3, P0B0-P0B3, P0C0-P0C3, P1D0-P1D3, P2B0-P2B3, P2C0-P2C3, P2D0-P2D2, P3C0-P3C3, and P3D0-P3D3	25.0	mA
		Total for P1B0-P1B3	25.0	mA
Output withstand voltage	V_{BDS}	P1B0-P1B3	14.0	V
Total loss	P_t		200	mW
Operating ambient temperature	T_A		−40 to +85	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Absolute maximum ratings are rated values beyond which physical damage will be caused to the product; if the rated value of any of the parameters in the above table is exceeded, even momentarily, the quality of the product may deteriorate. Always use the product within its rated values.

RECOMMENDED OPERATING RANGES (T_A = −40 to +85 °C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD1}	While the CPU and PLL are operating	4.5	5.0	5.5	V
	V_{DD2}	While the CPU is operating but the PLL is halted	3.5	5.0	5.5	V

RECOMMENDED OUTPUT WITHSTAND VOLTAGE (T_A = −40 to +85 °C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output withstand voltage	V_{BDS}	P1B0-P1B3			12	V

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Supply current	I_{DD1}	The CPU is operating but the PLL is halted, with a sinusoidal wave applied to the X_{IN} pin. (f_{IN} = 4.5 MHz ±1%, V_{IN} = V_{DD})			1.5	3.0	mA
	I_{DD2}	The CPU and PLL are halted, with a sinusoidal wave applied to the X_{IN} pin. (f_{IN} = 4.5 MHz ±1%, V_{IN} = V_{DD}) The HALT instruction is used.			0.7	1.5	mA
Data hold voltage	V_{DDR1}	The crystal oscillator is operating.		3.5		5.5	V
	V_{DDR2}	The crystal oscillator is halted.	The timer flip-flop is used for detecting power failure.	2.2		5.5	V
	V_{DDR3}		Data memory contents are held.	2.0		5.5	V
Data hold current	I_{DDR1}	The crystal oscillator is halted.	V_{DD} = 5 V, T_A = 25 °C		2.0	4.0	μA
	I_{DDR2}				2.0	30.0	μA
High input voltage	V_{IH1}	P0A0, P0B1, P0C0-P0C3, P1A0, P1A1, P1C0-P1C3, P1D0-P1D3, P2A2, P2B0-P2B3, P2C0-P2C3, P2D0-P2D2, P3A0-P3A3, P3B0-P3B3, P3C0-P3C3, P3D0-P3D3		$0.7V_{DD}$		V_{DD}	V
	V_{IH2}	P0A1-P0A3, P0B0, P0B2, P0B3, P2A0, P2A1, CE, INT0-INT4, $\overline{RESET}$		$0.8V_{DD}$		V_{DD}	V
	V_{IH3}	P0D0-P0D3		$0.55V_{DD}$		V_{DD}	V
Low input voltage	V_{IL1}	P0A0, P0B1, P0C0-P0C3, P1A0, P1A1, P1C0-P1C3, P1D0-P1D3, P2A2, P2B0-P2B3, P2C0-P2C3, P2D0-P2D2, P3A0-P3A3, P3B0-P3B3, P3C0-P3C3, P3D0-P3D3		0		$0.3V_{DD}$	V
	V_{IL2}	P0A1-P0A3, P0B0, P0B2, P0B3, P2A0, P2A1, CE, INT0-INT4, $\overline{RESET}$		0		$0.2V_{DD}$	V
	V_{IL3}	P0D0-P0D3		0		$0.15V_{DD}$	V
High output current	I_{OH1}	P0A0-P0A3, P0B0-P0B3, P0C0-P0C3, P1D0-P1D3, P2A0-P2A2, P2B0-P2B3, P2C0-P2C3, P2D0-P2D2, P3A0-P3A3, P3B0-P3B3, P3C0-P3C3, P3D0-P3D3 V_{OH} = V_{DD} − 1 V		−1.0			mA
	I_{OH2}	EO0, EO1 V_{DD} = 4.5 to 5.5 V, V_{OH} = V_{DD} − 1 V		−3.0			mA
Low output current	I_{OL1}	P0A0-P0A3, P0B0-P0B3, P0C0-P0C3, P1D0-P1D3, P2A0-P2A2, P2B0-P2B3, P2C0-P2C3, P2D0-P2D2, P3A0-P3A3, P3B0-P3B3, P3C0-P3C3, P3D0-P3D3 V_{OL} = 1 V		1.0			mA
	I_{OL2}	EO0, EO1 V_{DD} = 4.5 to 5.5 V, V_{OL} = 1 V		3.0			mA
	I_{OL3}	P1B0-P1B3 V_{OL} = 1 V		7.0			mA
High input current	I_{IH}	P0D0-P0D3 are pulled down. V_{IN} = V_{DD}		5.0		150	μA
Output-off leakage current	I_{LO1}	P1B0-P1B3 V_{IN} = 12 V				1.0	μA
	I_{LO2}	EO0, EO1 V_{IN} = V_{DD}, V_{IN} = 0 V				±1.0	μA
High input leakage current	I_{LIH}	Input pin V_{IN} = V_{DD}				1.0	μA
Low input leakage current	I_{LIL}	Input pin V_{IN} = 0 V				−1.0	μA

AC CHARACTERISTICS (T_A = −40 to +85 °C, V_{DD} = 5 V ±10%)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Operating frequency	f_{IN1}	VCOL pin in MF mode	Sinusoidal wave applied to the V_{IN} pin = 0.15 V_{P-P}	0.8		3	MHz
			Sinusoidal wave applied to the V_{IN} pin = 0.20 V_{P-P}	0.5		3	MHz
	f_{IN2}	VCOL pin in HF mode, with a sinusoidal wave applied to the V_{IN} pin = 0.1 V_{P-P}**Note**		10		40	MHz
	f_{IN3}	VCOH pin in VHF mode, with a sinusoidal wave applied to the V_{IN} pin = 0.1 V_{P-P}**Note**		60		130	MHz
	f_{IN4}	AMIFC pin, with a sinusoidal wave applied to the V_{IN} pin = 0.15 V_{P-P}		0.4		0.5	MHz
	f_{IN5}	FMIFC pin in FMIF count mode, with a sinusoidal wave applied to the V_{IN} pin = 0.20 V_{P-P}		10		11	MHz
	f_{IN6}	FMIFC pin in AMIF count mode, with a sinusoidal wave applied to the V_{IN} pin = 0.15 V_{P-P}		0.4		0.5	MHz
SIO0 input frequency	f_{IN7}	External clock				1	MHz
SIO1 input frequency	f_{IN8}	External clock				0.7	MHz

Note The condition of sinusoidal wave input V_{IN} = 0.1 V_{P-P} is the rated value when the μPD17P709 alone is operating. Where influence of noise must be taken into consideration, operation under input amplitude condition of V_{IN} = 0.15 V_{P-P} is recommended.

A/D CONVERTER CHARACTERISTICS (T_A = −40 to +85 °C, V_{DD} = 5 V ±10%)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Total error in A/D conversion		8 bits			±3.0	LSB
Total error in A/D conversion		8 bits T_A = 0 to 85 °C			±2.5	LSB

REFERENCE CHARACTERISTICS (T_A = +25 °C, V_{DD} = 5.0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current	I_{DD3}	The CPU and PLL are operating, with a sinusoidal wave applied to the VCOH pin. (f_{IN} = 130 MHz, V_{IN} = 0.3 V_{P-P})		6.0	12.0	mA

DC PROGRAMMING CHARACTERISTICS ($T_A = 25$ °C, $V_{DD} = 6.0 \pm 0.25$ V, $V_{PP} = 12.5 \pm 0.5$ V)

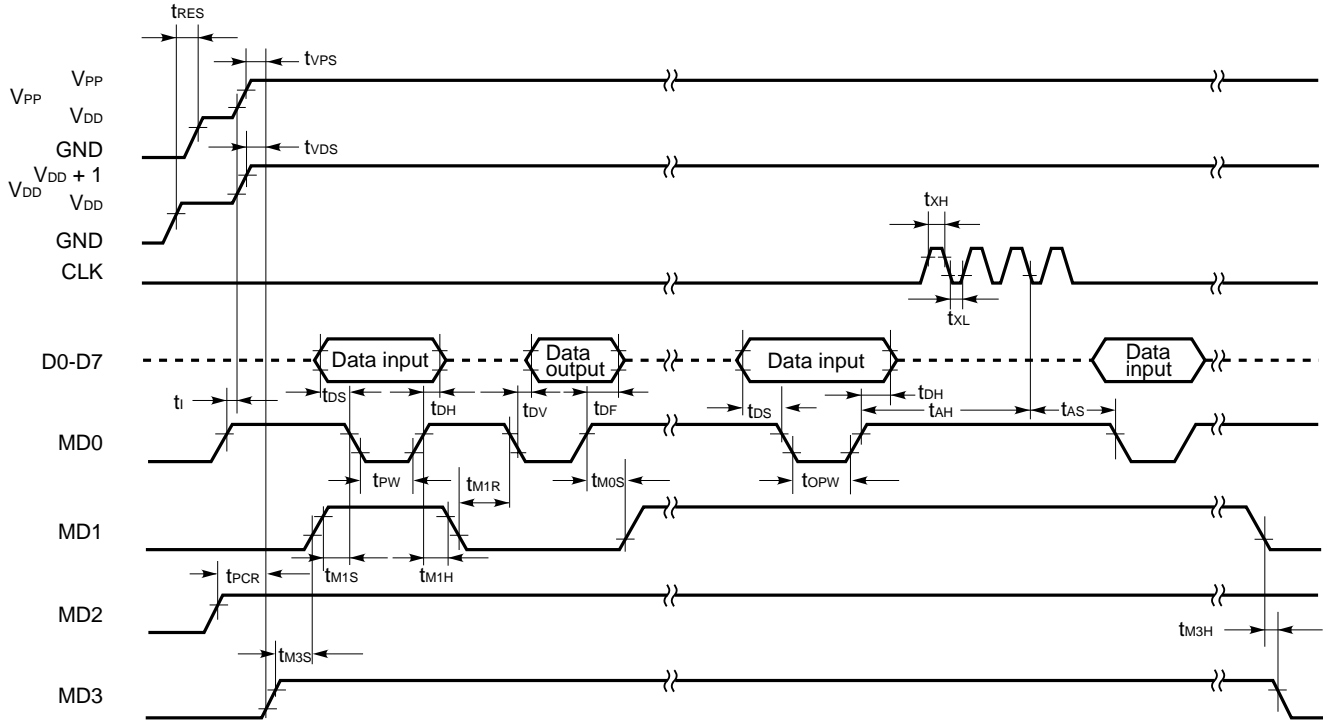| Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input high voltage	V_{IH1}	Other than CLK	$0.7V_{DD}$		V_{DD}	V
	V_{IH2}	CLK	$V_{DD} - 0.5$		V_{DD}	V
Input low voltage	V_{IL1}	Other than CLK	0		$0.2V_{DD}$	V
	V_{IL2}	CLK	0		0.4	V
Input leakage current	I_{LI}	$V_{IN} = V_{IL}$ or V_{IH}			10	μA
Output high voltage	V_{OH}	$I_{OH} = -1$ mA	$V_{DD} - 1.0$			V
Output low voltage	V_{OL}	$I_{OL} = 1$ mA			1.0	V
V_{DD} supply current	I_{DD}				30	mA
V_{PP} supply current	I_{PP}	$MD0 = V_{IL}$, $MD1 = V_{IH}$			30	mA

Cautions 1. V_{PP} must be under +13.5 V including overshoot.

2. V_{DD} must be applied before V_{PP} on and must be off after V_{PP} off.

AC PROGRAMMING CHARACTERISTICS ($T_A = 25$ °C, $V_{DD} = 6.0 \pm 0.25$ V, $V_{PP} = 12.5 \pm 0.5$ V)

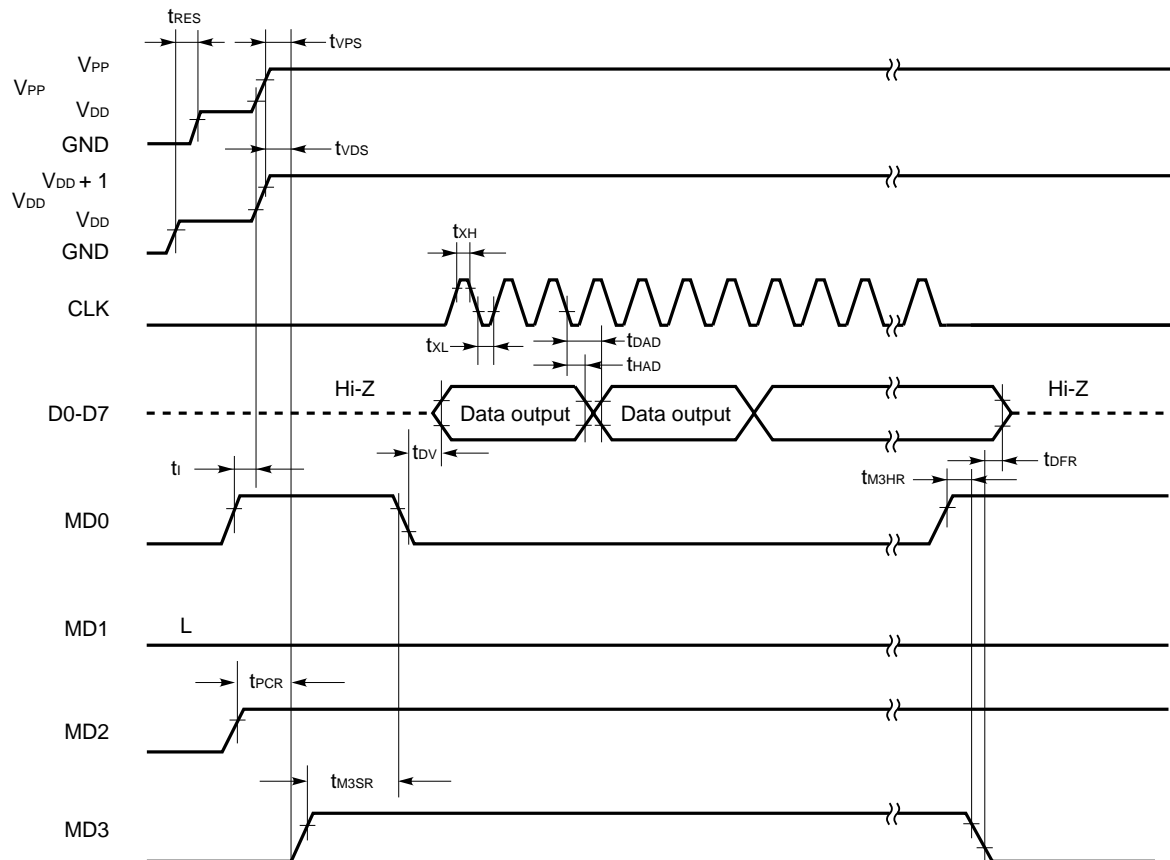| Parameter	Symbol	Note 1	Condition	Min.	Typ.	Max.	Unit
Address setup time[2] (referred to MD0↓)	t_{AS}	t_{AS}		2			μs
MD1 setup time (referred to MD0↓)	t_{M1S}	t_{OES}		2			μs
Data setup time (referred to MD0↓)	t_{DS}	t_{DS}		2			μs
Address hold time[2] (referred to MD0↑)	t_{AH}	t_{AH}		2			μs
Data hold time (referred to MD0↑)	t_{DH}	t_{DH}		2			μs
Data output float delay from MD0↑	t_{DF}	t_{DF}		0		130	ns
V_{PP} setup time (referred to MD3↑)	t_{VPS}	t_{VPS}		2			μs
V_{DD} setup time (referred to MD3↑)	t_{VDS}	t_{VCS}		2			μs
Initial program pulse width	t_{PW}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{OPW}	t_{OPW}		0.95		21.0	ms
MD0 setup time (referred to MD1↑)	t_{M0S}	t_{CES}		2			μs
Data output delay from MD0↓	t_{DV}	t_{DV}	$MD0 = MD1 = V_{IL}$			1	μs
MD1 hold time (referred to MD0↑)	t_{M1H}	t_{OEH}	$t_{M1H} + t_{M1R} \cdot 50$ μs	2			μs
MD1 recovery time (referred to MD0↓)	t_{M1R}	t_{OR}		2			μs
Program counter reset time	t_{PCR}	—		10			μs
CLK input high, low level range	t_{XH}, t_{XL}	—		0.125			μs
CLK input frequency	f_X	—				4.19	MHz
Initial mode set time	t_I	—		2			μs
MD3 setup time (referred to MD1↑)	t_{M3S}	—		2			μs
MD3 hold time (referred to MD1↓)	t_{M3H}	—		2			μs
MD3 setup time (referred to MD0↓)	t_{M3SR}	—	When reading program memory	2			μs
Data output delay from address increment[2]	t_{DAD}	t_{ACC}				2	μs
Data output hold time from address increment[2]	t_{HAD}	t_{OH}		0		130	ns
MD3 hold time (referred to MD0↑)	t_{M3HR}	—		2			μs
Data output float delay from MD3↓	t_{DFR}	—				2	μs
Reset setup time	t_{RES}	—		10			μs

Notes 1. Symbols used for the μPD27C256 (The μPD27C256 is used only for maintenance.)

2. The internal address signal is incremented by 1 on the falling edge of the third clock (CLK) pulse, with four CLK pulses treated as one cycle. Internal addresses are not connected to pins.
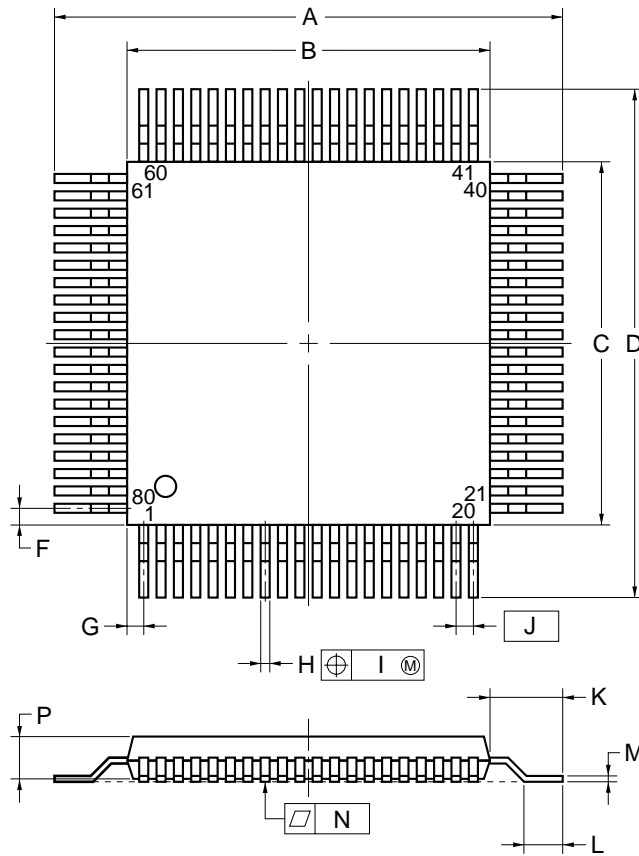
Write program memory timing

V_{PP}	V_{PP} / V_{DD} / GND
V_{DD}	V_{DD} + 1 / V_{DD} / GND

t_{RES}, t_{VPS}, t_{VDS}

CLK — t_{XH}, t_{XL}

D0-D7 — Data input, Data output, Data input, Data input

MD0 — t_I, t_{DS}, t_{DH}, t_{DV}, t_{DF}, t_{DS}, t_{DH}, t_{AH}, t_{AS}

MD1 — t_{PW}, t_{M1R}, t_{M0S}, t_{OPW}

MD2 — t_{PCR}, t_{M1S}, t_{M1H}, t_{M3H}

MD3 — t_{M3S}

Remark The dashed line indicates high-impedance.

Read program memory timing

V_{PP}	V_{PP} / V_{DD} / GND
V_{DD}	V_{DD} + 1 / V_{DD} / GND

t_{RES}, t_{VPS}, t_{VDS}

CLK — t_{XH}, t_{XL}, t_{DAD}, t_{HAD}

D0-D7 — Hi-Z, Data output, Data output, Hi-Z

MD0 — t_I, t_{DV}, t_{M3HR}, t_{DFR}

MD1 — L
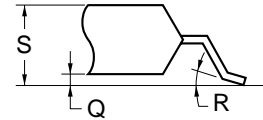
MD2 — t_{PCR}

MD3 — t_{M3SR}

3 0

4. PACKAGE DRAWING

80 PIN PLASTIC QFP (14×14)

detail of lead end

NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.825	0.032
G	0.825	0.032
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S80GC-65-3B9-4

5. RECOMMENDED SOLDERING CONDITIONS

The conditions listed below shall be met when soldering the μPD17P709.

For details of the recommended soldering conditions, refer to our document *SMD Surface Mount Technology Manual* (C10535E).

Please consult with our sales offices in case any other soldering process is used, or in case soldering is done under different conditions.

Table 5-1   Soldering Conditions for Surface-Mount Devices

μ**PD17P709GC-3B9: 80-pin plastic QFP (14 × 14 mm, 0.65-mm pitch)**

Soldering process	Soldering conditions	Recommended conditions
Infrared ray reflow	Peak package's surface temperature: 235 °C Reflow time: 30 seconds or less (at 210 °C or more) Maximum allowable number of reflow processes: 2	IR35-00-2
VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (at 200 °C or more) Maximum allowable number of reflow processes: 2	VP15-00-2
Wave soldering	Solder temperature: 260 °C or less Flow time: 10 seconds or less Number of flow processes: 1 Preheating temperature: 120°C max. (measured on the package surface)	WS60-00-1
Partial heating method	Terminal temperature: 300 °C or less Heat time: 3 seconds or less (for one side of a device)	—

Caution   Do not apply more than a single process at once, except for "Partial heating method."

APPENDIX DEVELOPMENT TOOLS

The following support tools are available for developing programs for the μPD17P709.

Hardware

Name	Description
In-circuit emulator [IE-17K IE-17K-ET**Note 1** EMU-17K**Note 2**]	The IE-17K, IE-17K-ET, and EMU-17K are in-circuit emulators applicable to the 17K series. The IE-17K and IE-17K-ET are connected to the host machine (PC-9800 series or IBM PC/AT™) through the RS-232C interface. The EMU-17K is inserted into the extension slot of the host machine (PC-9800 series). Use the system evaluation board (SE board) corresponding to each product together with one of these in-circuit emulators. *SIMPLEHOST*®, a man machine interface, implements an advanced debug environment. The EMU-17K also enables user to check the contents of the data memory in real time.
SE board (SE-17709)	The SE-17709 is an SE board for the μPD17709 sub-series. It is used alone for evaluating the system. It is also used for debugging, in combination with an in-circuit emulator.
Emulation probe (EP-17K80GC)	The EP-17K80GC is an emulation probe for the μPD17P709GC. When used with the EV-9200GC-80**Note 3**, this emulation probe connects the SE board to the target system.
Conversion socket (EV-9200GC-80**Note 3**)	The EV-9200GC-80 is a conversion socket for the 80-pin plastic QFP (14 × 14 mm). It is used to connect the EP-17K80GC to the target system.
PROM Programmer (PG-1500)	The PG-1500 is a PROM programmer for the μPD17P709. Use this PROM programmer with the PA-17KDZ (adapter for the PG-1500) and PA-17P709GC programmer adapter, to program the μPD17P709.
Programmer adapter (PA-17P709GC)	The PA-17P709GC is a socket unit for the μPD17P709. It is used with the PG-1500.

Notes 1. Low-end model, operating on an external power supply

2. The EMU-17K is a product of I.C Corporation. Contact I.C Corporation (Tokyo, 03-3733-1163) for details.

3. The EP-17K80GC is supplied together with one EV-9200GC-80. A set of five EV-9200GC-80s is also available.

Remark Third-party PROM programmers are also available: For example, AF-9703, AF-9704, AF-9705, and AF-9706 (manufactured by Ando Electric Co., Ltd.). These PROM programmers can be used with the PA-17P709GC programmer adapter. For details, contact Ando Electric Co., Ltd. (Tokyo, 03-3733-1151).

Software

Name	Description	Host machine	OS		Distribution media	Part number
17K series assembler (AS17K)	AS17K is an assembler applicable to the 17K series. In developing μPD17P709 programs, AS17K is used in combination with a device file (AS17704).	PC-9800 series	MS-DOS™		5.25-inch, 2HD	μS5A10AS17K
					3.5-inch, 2HD	μS5A13AS17K
		IBM PC/AT	PC DOS™		5.25-inch, 2HC	μS7B10AS17K
					3.5-inch, 2HC	μS7B13AS17K
Device file (AS17704)	AS17704 has a device file for the μPD17P709 . It is used together with the assembler (AS17K), which is applicable to the 17K series.	PC-9800 series	MS-DOS		5.25-inch, 2HD	μS5A10AS17704
					3.5-inch, 2HD	μS5A13AS17704
		IBM PC/AT	PC DOS		5.25-inch, 2HC	μS7B10AS17704
					3.5-inch, 2HC	μS7B13AS17704
Support software (SIMPLEHOST)	SIMPLEHOST, running under Windows™, provides a man machine interface in developing programs by using a personal computer and in-circuit emulator.	PC-9800 series	MS-DOS	Windows	5.25-inch, 2HD	μS5A10IE17K
					3.5-inch, 2HD	μS5A13IE17K
		IBM PC/AT	PC DOS		5.25-inch, 2HC	μS7B10IE17K
					3.5-inch, 2HC	μS7B13IE17K

Remark The following table lists the versions of the operating systems described in the above table.

OS	Versions
MS-DOS	Ver. 3.30 to Ver.5.00A[Note]
PC DOS	Ver. 3.1 to Ver. 5.0[Note]
Windows	Ver. 3.0 to Ver. 3.1

Note MS-DOS versions 5.00 and 5.00A and PC DOS Ver. 5.0 are provided with a task swap function. This function, however, cannot be used in these software packages.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

Caution This product contains an I^{2}C bus interface circuit.
When using the I^{2}C bus interface, notify its use to NEC when ordering custom code. NEC can guarantee the following only when the customer informs NEC of the use of the interface:
Purchase of NEC I^{2}C components conveys a license under the Philips I^{2}C Patent Rights to use these components in an I^{2}C system, provided that the system conforms to the I^{2}C Standard Specification as defined by Philips.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

• Device availability

• Ordering information

• Product release schedule

• Availability of related technical literature

• Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)

• Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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