

8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μ PD78F0833Y is a product of the μ PD780833Y Subseries in the 78K/0 Series, and equivalent to the μ PD780833Y with a flash memory in place of internal ROM.

This device can be programmed (write, delete, rewrite) without being removed from the board.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μ PD780833Y Subseries User's Manual: U13892E

78K/0 Series User's Manual Instructions: U12326E

FEATURES

- Pin-compatible with mask ROM versions (except V_{PP} pin)
- Flash memory: 60 KB (self-programming supported)
- Internal high-speed RAM: 1,024 bytes
- Internal expansion RAM: 2,048 bytes
- Supply voltage: $V_{DD} = 4.5$ to 5.5 V

Remark For the differences between the flash memory version and the mask ROM version, refer to **4 DIFFERENCES BETWEEN μ PD78F0833Y AND MASK ROM VERSION.**

APPLICATIONS

Car audios, etc.

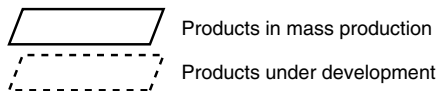
ORDERING INFORMATION

Part Number	Package
μ PD78F0833YGC-8BT	80-pin plastic QFP (14 × 14)

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.



Y subseries products are compatible with I²C bus.

78K/0 Series	Control		
	100-pin	μPD78075B	μ PD78078 with reduced EMI noise
	100-pin	μPD78078 μPD78078Y	μ PD78054 with timer added and enhanced external interface
	100-pin	μPD78070A μPD78070AY	ROMless version of μPD78078
	100-pin	μPD780018AY	μ PD78078Y with enhanced serial I/O and limited functions
	80-pin	μPD780058 μPD780058Y	μ PD78054 with enhanced serial I/O
	80-pin	μPD78058F μPD78058FY	μ PD78054 with reduced EMI noise
	80-pin	μPD78054 μPD78054Y	μ PD78018F with UART and D/A added, and enhanced I/O
	80-pin	μPD780065	μPD780024A with expanded RAM
	64-pin	μPD780078 μPD780078Y	μPD780034A with timer added and enhanced serial I/O
	64-pin	μPD780034A μPD780034AY	μPD780024A with enhanced A/D
	64-pin	μPD780024A μPD780024AY	μPD78018F with enhanced serial I/O
	64-pin	μPD78014H	μPD78018F with reduced EMI noise
	64-pin	μPD78018F μPD78018FY	Basic subseries for control
	42/44-pin	μPD78083	On-chip UART and capable of low voltage operation (1.8 V)
	Inverter control		
	64-pin	μPD780988	On-chip inverter controller and UART. Reduced EMI noise.
	VFD drive		
	100-pin	μPD780208	μPD78044F with enhanced I/O and VFD C/D. Display output total: 53
	80-pin	μPD780232	For panel control. On-chip VFD C/D. Display output total: 53
	80-pin	μPD78044H	μPD78044F with N-ch open drain I/O added. Display output total: 34
	80-pin	μPD78044F	Basic subseries for driving VFD. Display output total: 34
	LCD drive		
	120-pin	μPD780338	μPD780308 with enhanced display function and timer. Segment signal output: 40 pins max.
	120-pin	μPD780328	μPD780308 with enhanced display function and timer. Segment signal output: 32 pins max.
	120-pin	μPD780318	μPD780308 with enhanced display function and timer. Segment signal output: 24 pins max.
	100-pin	μPD780308 μPD780308Y	μPD78064 with enhanced SIO and expanded ROM, RAM
	100-pin	μPD78064B	μPD78064 with reduced EMI noise
	100-pin	μPD78064 μPD78064Y	Basic subseries for driving LCD. On-chip UART.
	Bus interface supported		
	100-pin	μPD780948	On-chip DCAN controller
	80-pin	μPD78098B	μPD78054 with IEBus™ controller added. Reduced EMI noise.
	80-pin	μPD780701Y	On-chip DCAN/IEBus controller
	80-pin	μPD780833Y	On-chip J1850 (CLASS2) controller
	Meter control		
100-pin	μPD780958	For industrial meter control	
80-pin	μPD780852	On-chip controller/driver for automobile meter drive	
80-pin	μPD780824	For automobile meter drive. On-chip DCAN controller	

Remark VFD (Vacuum Fluorescent Display) is referred to as FIPT™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major functional differences among the subseries are listed below.

Function Subseries Name		ROM Capacity	Timer				8-bit	10-bit	8-bit	Serial Interface	I/O	V _{DD} MIN. Value	External Expansion						
			8-bit	16-bit	Watch	WDT	A/D	A/D	D/A										
Control	μPD78078Y	48 K to 60 K	4 ch	1 ch	1 ch	1 ch	8 ch	-	2 ch	3 ch (UART: 1 ch, I ² C: 1 ch)	88	1.8 V	Yes						
	μPD78070AY	-									61	2.7 V							
	μPD780018AY	48 K to 60 K	2 ch	-	-	-	-	-	-	3 ch (I ² C: 1 ch)	88	1.8 V							
	μPD780058Y	24 K to 60 K									68								
	μPD78058FY	48 K to 60 K									69			2.7 V					
	μPD78054Y	16 K to 60 K									2.0 V								
	μPD780078Y	48 K to 60 K									2 ch			-	8 ch	-	4 ch (UART: 2 ch, I ² C: 1 ch)	52	1.8 V
	μPD780034AY	8 K to 32 K									1 ch			8 ch	-	-	3 ch (UART: 1 ch, I ² C: 1 ch)	51	
	μPD780024AY																		
	μPD78018FY	8 K to 60 K									2 ch (I ² C: 1 ch)						53		
LCD drive	μPD780308Y	48 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	-	-	3 ch (time-division UART: 1 ch, I ² C: 1 ch)	57	2.0 V	-						
	μPD78064Y	16 K to 32 K								2 ch (UART: 1 ch, I ² C: 1 ch)									
Bus interface supported	μPD780701Y	60 K	3 ch	2 ch	1 ch	1 ch	16 ch	-	-	4 ch (UART: 1 ch, I ² C: 1 ch)	67	3.5 V	-						
	μPD780833Y										65	4.5 V							

FUNCTION OVERVIEW

Item		μPD78F0833Y
Internal memory	Flash memory	60 KB
	High-speed RAM	1,024 bytes
	Expansion RAM	2,048 bytes
Memory space		64 KB
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Minimum instruction execution time		On-chip minimum instruction execution time variable function 0.48 μs/0.96 μs/1.92 μs/3.84 μs/7.68 μs (@ 4.19 MHz operation)
Instruction set		<ul style="list-style-type: none"> • 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, and Boolean operation) • BCD adjust, etc.
I/O ports		Total: <u>65</u> <ul style="list-style-type: none"> • CMOS input: 54 • TTL input/CMOS output: 8 • N-ch open-drain I/O: 3
A/D converter		<ul style="list-style-type: none"> • 8-bit resolution × 8 channels × 2
Serial interface		<ul style="list-style-type: none"> • 3-wire serial I/O mode: 2 channels • UART mode: 1 channel • I²C bus mode: 1 channel
Timer		<ul style="list-style-type: none"> • 16-bit timer/event counter: 2 channels • 8-bit timer/event counter: 3 channels • Watch timer: 1 channel • Watchdog timer: 1 channel
Timer outputs		5 (8-bit PWM output: 3)
Clock output		32.8 kHz, 65.5 kHz, 130.9 kHz, 261.9 kHz, 523.6 kHz, 1.05 MHz, 2.10 MHz, 4.19 MHz (@ 4.19 MHz operation with system clock)
Bus controller		J1850 (CLASS2) bus interface
Vectored interrupts	Maskable	Internal: 19 External: 9
	Non-maskable	Internal: 1
	Software	1
Power supply voltage		V _{DD} = 4.5 to 5.5 V
Operating ambient temperature		T _A = -40 to +85°C
Package		80-pin plastic QFP (14 × 14)

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)6

2. BLOCK DIAGRAM8

3. PIN FUNCTIONS9

3.1 Port Pins 9

3.2 Non-Port Pins..... 10

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins..... 12

4. DIFFERENCES BETWEEN μPD78F0833Y AND MASK ROM VERSION 16

5. MEMORY SIZE SWITCHING REGISTER (IMS)..... 17

6. INTERNAL EXPANSION RAM SIZE SWITCHING REGISTER (IXS) 18

7. FLASH MEMORY PROGRAMMING 19

7.1 Selection of Communication Mode..... 19

7.2 Flash Memory Programming Functions 20

7.3 Flashpro II and Flashpro III Connection 20

7.4 Flash Memory Programming by Self Write 21

8. ELECTRICAL SPECIFICATIONS28

9. PACKAGE DRAWING44

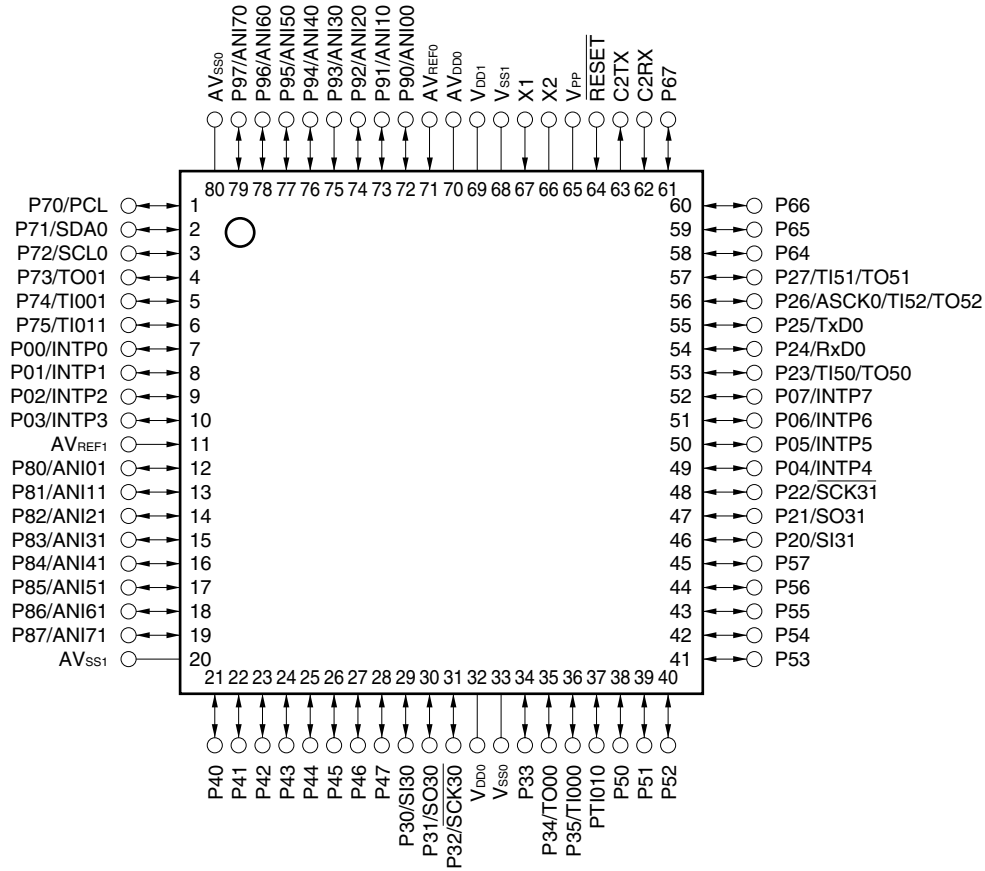
10. RECOMMENDED SOLDERING CONDITIONS45

APPENDIX A. DEVELOPMENT TOOLS46

APPENDIX B. RELATED DOCUMENTS51

1. PIN CONFIGURATION (TOP VIEW)

- 80-pin plastic QFP (14 × 14)
μPD78F0833YGC-8BT

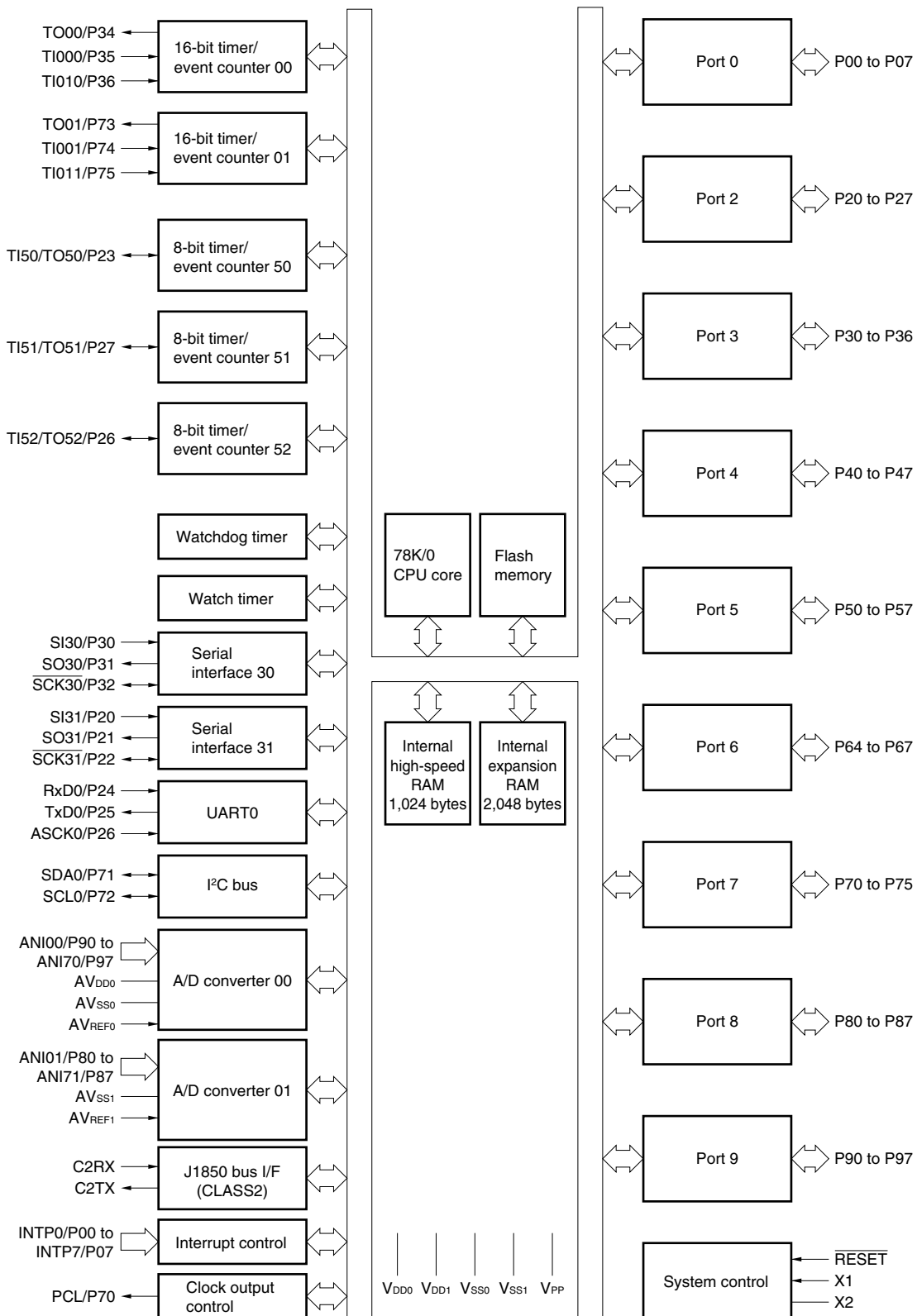


- Cautions**
1. Connect the VPP pin directly to VSS0 or VSS1 in normal operation mode.
 2. Connect the AVDD0 pin to VDD0.
 3. Connect the AVSS0 and AVSS1 pins to VSS0.

PIN IDENTIFICATION

ANI00 to ANI70,		PCL:	Programmable clock
ANI01 to ANI71:	Analog input	RxD0:	Receive data
ASCK0:	Asynchronous serial clock	RESET:	Reset
AV _{DD0} :	Analog power supply	<u>SCK30</u> , <u>SCK31</u> :	Serial clock
AV _{REF0} , AV _{REF1} :	Analog reference voltage	SCL0:	Serial clock
AV _{SS0} , AV _{SS1} :	Analog ground	SDA0:	Serial data
C2RX:	CLASS2 receive data	SI30, SI31:	Serial input
C2TX:	CLASS2 transmit data	SO30, SO31:	Serial output
INTP0 to INTP7:	External interrupt input	TI000, TI010,	
P00 to P07:	Port 0	TI001, TI011,	
P20 to P27:	Port 2	TI50, TI51, TI52:	Timer input
P30 to P36:	Port 3	TO00, TO01,	
P40 to P47:	Port 4	TO50, TO51,	
P50 to P57:	Port 5	TO52:	Timer output
P64 to P67:	Port 6	TxD0:	Transmit data
P70 to P75:	Port 7	V _{DD0} , V _{DD1} :	Power supply
P80 to P87:	Port 8	V _{PP} :	Programming power supply
P90 to P97:	Port 9	V _{SS0} , V _{SS1} :	Ground
		X1, X2:	Crystal

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P00 to P07	I/O	Port 0 8-bit I/O port Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.		Input	INTP0 to INTP7
P20	I/O	Port 2 8-bit I/O port Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.		Input	SI31
P21					SO31
P22					$\overline{\text{SCK31}}$
P23					TI50/TO50
P24					RxD0
P25					TxD0
P26					ASCK0/TI52/TO52
P27					TI51/TO51
P30	I/O	Port 3 7-bit I/O port Input/output can be specified in 1-bit units.		Input	SI30
P31					SO30
P32					$\overline{\text{SCK30}}$
P33		N-ch open-drain I/O port LEDs can be driven directly.			—
P34		An on-chip pull-up resistor can be specified by software.			TO00
P35		TI000			
P36		TI010			
P40 to P47	I/O	Port 4 8-bit I/O port Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software. Interrupt request flag (KRIF) is set to 1 by falling edge detection.		Input	—
P50 to P57	I/O	Port 5 8-bit I/O port TTL level input/CMOS output Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.		Input	—
P64 to P67	I/O	Port 6 4-bit I/O port Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.		Input	—

3.1 Port Pins (2/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P70	I/O	Port 7 6-bit I/O port Input/output can be specified in 1-bit units.	An on-chip pull-up resistor can be specified by software.	Input	PCL
P71			N-ch open-drain I/O port		SDA0
P72					SCL0
P73		An on-chip pull-up resistor can be specified by software.			TO01
P74					TI001
P75					TI011
P80 to P87	I/O	Port 8 1-bit I/O port Input/output can be specified in 1-bit units.		Input	ANI01 to ANI71
P90 to P97	I/O	Port 9 1-bit I/O port Input/output can be specified in 1-bit units.		Input	ANI00 to ANI70

3.2 Non-Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function
INTP0 to INTP7	Input	External interrupt request input for which valid edge can be specified (rising edge, falling edge, both rising and falling edges)		Input	P00 to P07
SI30	Input	Serial interface SIO30 serial data input		Input	P30
SI31		Serial interface SIO31 serial data input			P20
SO30	Output	Serial interface SIO30 serial data output		Input	P31
SO31		Serial interface SIO31 serial data output			P21
SDA0	I/O	Serial interface IIC0 serial data input/output		Input	P71
$\overline{\text{SCK30}}$	I/O	Serial interface SIO30 serial clock input/output		Input	P32
$\overline{\text{SCK31}}$		Serial interface SIO31 serial clock input/output			P22
SCL0		Serial interface IIC0 serial clock input/output			P72
RxD0	Input	Asynchronous serial interface serial data input		Input	P24
TxD0	Output	Asynchronous serial interface serial data output		Input	P25
ASCK0	Input	Asynchronous serial interface serial clock input		Input	P26/TI52/TO52
TI000	Input	External count clock input to 16-bit timer/event counter 00 Capture trigger input to capture register (CR000 and CR010) of 16-bit timer/event counter 00		Input	P35
TI010		Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00			P36
TI001		External count clock input to 16-bit timer/event counter 01 Capture trigger input to capture register (CR001 and CR011) of 16-bit timer/event counter 01			P74
TI011		Capture trigger input to capture register (CR001) of 16-bit timer/event counter 01			P75

3.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
TI50	Input	External count clock input to 8-bit timer/event counter 50	Input	P23/TO50
TI51		External count clock input to 8-bit timer/event counter 51		P27/TO51
TI52		External count clock input to 8-bit timer/event counter 52		P26/ASCK0/TO52
TO00	Output	16-bit timer/event counter 00 output	Input	P34
TO01		16-bit timer/event counter 01 output		P73
TO50		8-bit timer/event counter 50 output		P23/TI50
TO51		8-bit timer/event counter 51 output		P27/TI51
TO52		8-bit timer/event counter 52 output		P26/ASCK0/TI52
PCL	Output	Clock output	Input	P70
ANI00 to ANI70	Input	A/D converter (AD00) analog input	Input	P90 to P97
ANI01 to ANI71		A/D converter (AD01) analog input		P80 to P87
AV _{REF0}	—	A/D converter (AD00) reference voltage input	—	—
AV _{REF1}		A/D converter (AD01) analog power supply and reference voltage input		—
AV _{DD0}		A/D converter (AD00) analog power supply		—
AV _{SS0}		A/D converter (AD00) ground potential. Make the same potential as V _{SS0} or V _{SS1} .		—
AV _{SS1}		A/D converter (AD01) ground potential. Make the same potential as V _{SS0} or V _{SS1} .		—
C2RX		Input		CLASS 2 data input
C2TX	Output	CLASS 2 data output	—	—
RESET	Input	System reset input	—	—
X1	Input	Connecting crystal resonator for oscillation	—	—
X2				—
V _{DD0}		Positive power supply for ports		—
V _{DD1}		Positive power supply (other than for ports)		—
V _{SS0}		Ground potential for ports		—
V _{SS1}		Ground potential (other than for ports)		—
V _{PP}		Applying high voltage for program write/verify Connect directly to V _{SS0} or V _{SS1} in normal operation mode.		—

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.

For the I/O circuit configuration of each type, see Figure 3-1.

Table 3-1. Pin I/O Circuit Types and Recommended Connection of Unused Pins (1/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/INTP0 to P07/INTP7	8-C	I/O	Input: Independently connect to V _{SS0} via a resistor. Output: Leave open.
P20/SI31	5-H		Input: Independently connect to V _{DD0} or V _{SS0} via a resistor. Output: Leave open.
P21/SO31			
P22/SCK31			
P23/TI50/TO50			
P24/RxD0			
P25/TxD0			
P26/ASCK0/TI52/TO52			
P27/TI51/TO51			
P30/SI30			
P31/SO30			
P32/SCK30			
P33	13-P		Input: Independently connect to V _{DD0} via a resistor. Output: Leave open.
P34/TO00	5-H		Input: Independently connect to V _{DD0} or V _{SS0} via a resistor. Output: Leave open.
P35/TI000	8-C		
P36/TI010	5-H		
P40 to P47		Input: Independently connect to V _{DD0} via a resistor. Output: Leave open.	
P50 to P57	5-T	Input: Independently connect to V _{DD0} or V _{SS0} via a resistor. Output: Leave open.	
P64 to P67	5-H		
P70/PCL	13-R		
P71/SDA0		Input: Independently connect to V _{DD0} via a resistor. Output: Leave open.	
P72/SCL0	5-H	Input: Independently connect to V _{DD0} or V _{SS0} via a resistor. Output: Leave open.	
P73/TO01			
P74/TI001			8-C
P75/TI011	11-E	Input: Independently connect to V _{DD0} or V _{SS0} via a resistor. Output: Leave open.	
P80/ANI01 to P87/ANI71			
P90/ANI00 to P97/ANI70	2	Input	Connect to V _{SS0} via a resistor.
C2RX		Output	Leave open.
C2TX		Input	—

Table 3-1. Pin I/O Circuit Types and Recommended Connection of Unused Pins (2/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
AV _{DD0}	—	—	Connect to V _{DD0} .
AV _{REF0}			
AV _{REF1}			
AV _{SS0}			Connect to V _{SS0} .
AV _{SS1}			
V _{PP}			

Figure 3-1. Pin I/O Circuit List (1/2)

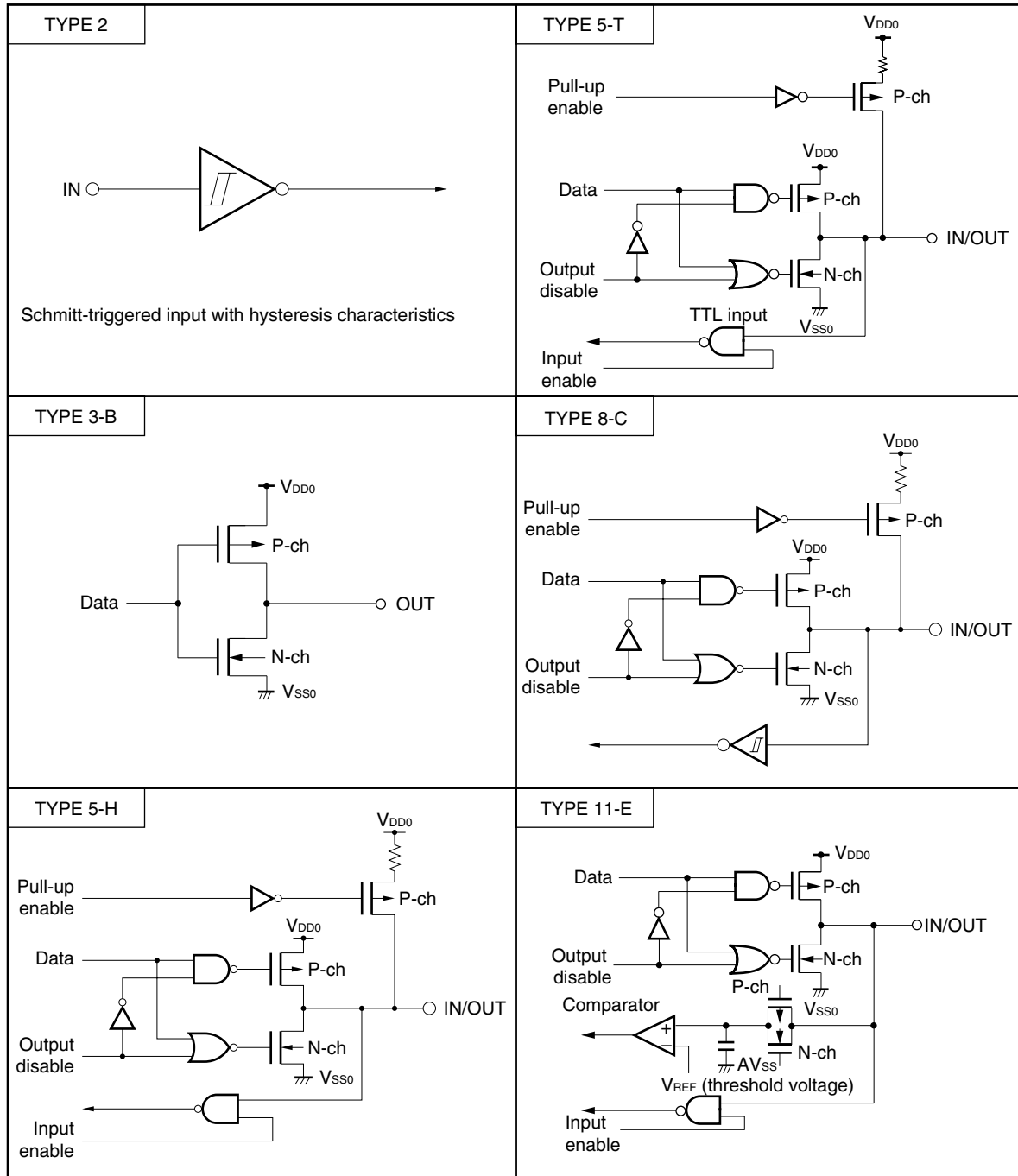
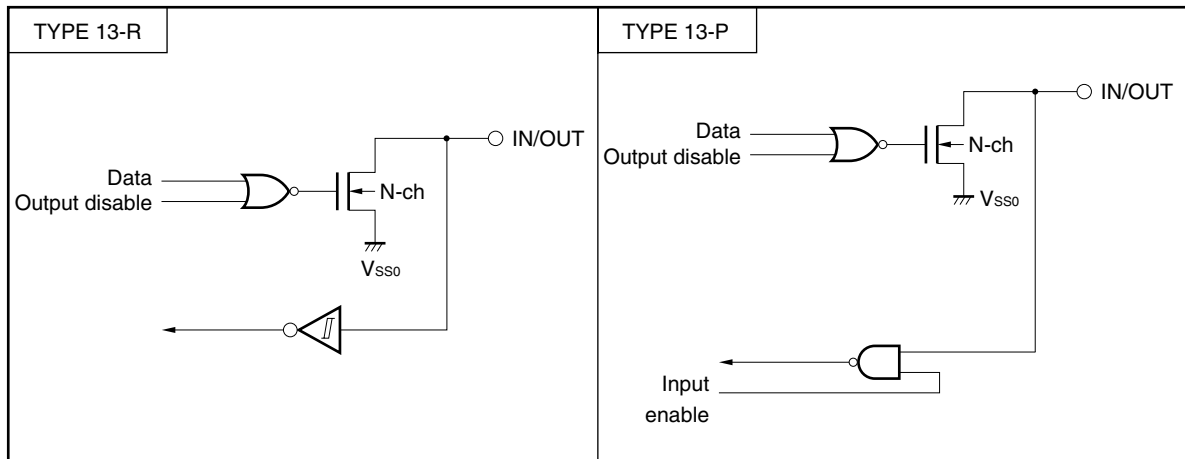


Figure 3-1. Pin I/O Circuit List (2/2)



4. DIFFERENCES BETWEEN μPD78F0833Y AND MASK ROM VERSION

The μPD78F0833Y incorporates flash memory in which a program can be written, deleted, and overwritten while mounted on the board. Table 4-1 lists the differences between the μPD78F0833Y and the mask ROM versions.

Table 4-1. Difference Between μPD78F0833Y and Mask ROM Version

Item	μPD78F0833Y	μPD780833Y
Internal ROM capacity	60 KB	
Internal ROM structure	Flash memory	Mask ROM
IC pin	Not provided	Provided
V _{PP} pin	Provided	Not provided
Electrical specifications, recommended soldering conditions	Refer to the data sheet of individual products.	

Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations on the commercial samples (CS) (not engineering sample, ES) of the mask ROM version.

5. MEMORY SIZE SWITCHING REGISTER (IMS)

This register sets the internal memory capacity by software.

IMS is set with an 8-bit memory manipulation instruction.

RESET input sets IMS to CFH.

Figure 5-1. Format of Memory Size Switching Register (IMS)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

RAM2	RAM1	RAM0	Selection of internal high-speed RAM capacity
1	1	0	1,024 bytes
Other than above			Setting prohibited

ROM3	ROM2	ROM1	ROM0	Selection of internal ROM capacity
1	1	0	0	48 KB
1	1	1	1	60 KB
Other than above				Setting prohibited

6. INTERNAL EXPANSION RAM SIZE SWITCHING REGISTER (IXS)

This register sets the internal expansion RAM capacity by software.

IXS is set with an 8-bit memory manipulation instruction.

RESET input sets IXS to 0CH.

Caution The default value of IXS is 0CH (setting prohibited). Be sure to set 08H as the initial setting.

Figure 6-1. Format of Internal Expansion RAM Size Switching Register (IXS)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
IXS	0	0	0	IXRAM4	IXRAM3	IXRAM2	IXRAM1	IXRAM0	FFF4H	0CH	R/W

IXRAM4	IXRAM3	IXRAM2	IXRAM1	IXRAM0	Selection of internal high-speed RAM capacity
0	1	0	0	0	2,048 bytes
Other than above					Setting prohibited

7. FLASH MEMORY PROGRAMMING

Writing to flash memory can be performed without removing the memory from the target system. Writing is performed with the dedicated flash programmer Flashpro II (part number: FL-PR2) and Flashpro III (part number: FL-PR3 and PG-FP3) connected to the host machine and the target system. Moreover, writing to flash memory can also be performed using a flash memory writing adapter connected to Flashpro II or Flashpro III.

Remark FL-PR2 and FL-PR3 are products of Naito Densai Machida Mfg. Co., Ltd.

7.1 Selection of Communication Mode

Writing to flash memory is performed using Flashpro II or Flashpro III via a serial communication mode. The communication mode is selected from those in Table 7-1. The selection of the communication mode is made by using the format shown in Figure 7-1. Each communication mode is selected by the number of V_{PP} pulses shown in Table 7-1.

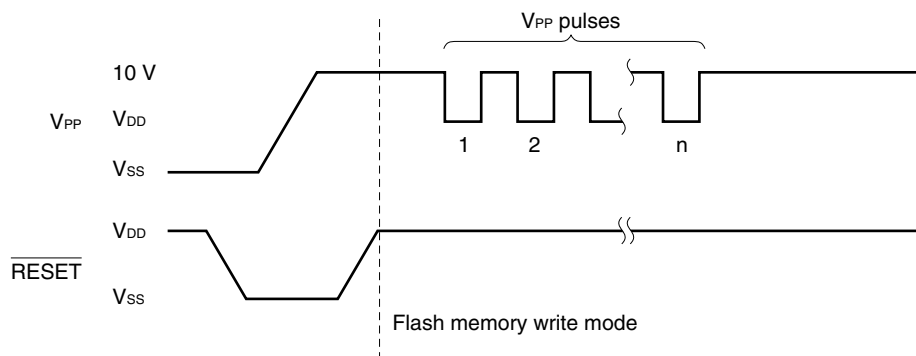
Table 7-1. List of Communication Modes

Communication Mode	Channels	Pin Used ^{Note}	V_{PP} Pulses
3-wire serial I/O (SIO3)	2	SI30/P30 SO30/P31 SCK30/P32	2
		SI31/P20 SO31/P21 SCK31/P22	1

Note Shifting to the flash memory programming mode sets all pins not used for flash memory programming to the same state as immediately after reset. Therefore, all ports enter an output high-impedance state. If the external devices do not acknowledge an output high-impedance state, handling such as connecting to V_{DD} via a resistor or connecting to V_{SS} via a resistor is required.

- Cautions**
1. Be sure to select the number of V_{PP} pulses shown in Table 7-1 for the communication mode.
 2. If performing write operations to flash memory via the UART communication mode, set the system clock oscillation frequency to 3 MHz or higher.

Figure 7-1. Format of Communication Mode Selection



7.2 Flash Memory Programming Functions

Operations such as writing to flash memory are performed by various command/data transmission and reception operations according to the selected communication mode. Table 7-2 shows major functions of flash memory programming.

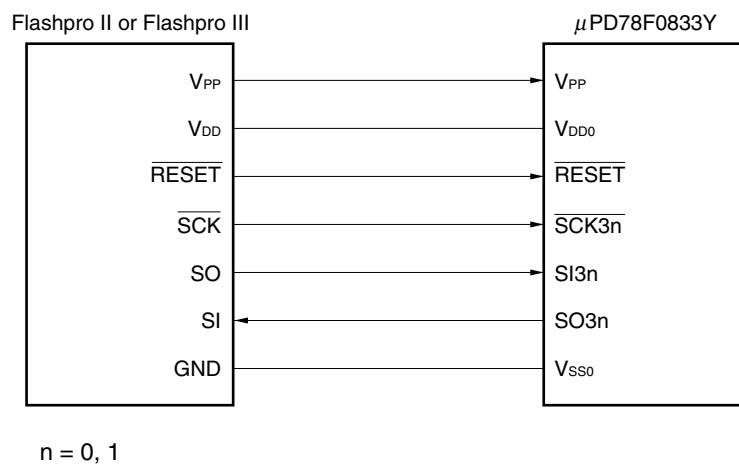
Table 7-2. Major Functions of Flash Memory Programming

Function	Description
Reset	Used to detect write stop and communication synchronization.
Batch verify	Compares entire memory contents and input data.
Batch contents verify	Compares entire memory contents in the different modes.
Batch delete	Deletes the entire memory contents.
Batch blank check	Checks the deletion status of the entire memory.
High-speed write	Writes to flash memory according to write start address and number of write data (bytes).
Continuous write	Successively writes using the data input in a high-speed write operation.
Batch prewrite	Writes 00H to entire memory.
Status	Checks the current operation mode and whether operation has ended.
Oscillation frequency setting	Inputs the resonator oscillation frequency information.
Delete time setting	Inputs the memory delete time.
Silicon signature read	Outputs the device name, memory capacity, and device block information.

7.3 Flashpro II and Flashpro III Connection

The connection of the Flashpro II and Flashpro III and the μPD78F0833Y is shown in Figure 7-2.

Figure 7-2. Connection of Flashpro II and Flashpro III in 3-Wire Serial I/O (SI03) Mode



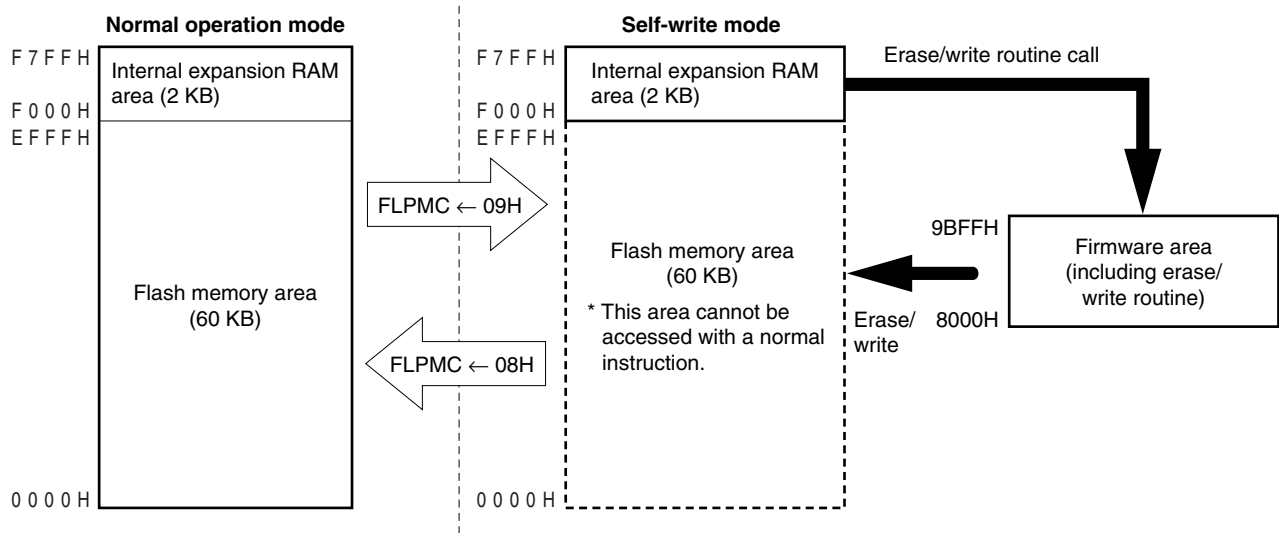
7.4 Flash Memory Programming by Self Write

With the μPD78F0833Y, it is possible to rewrite the flash memory using a program.

(1) Flash memory configuration

The configuration of the flash memory is shown in Figure 7-3.

Figure 7-3. Flash Memory Configuration



(2) Flash programming mode control register (FLPMC)

The flash programming mode control register (FLPMC) is a register for checking the operating mode selection and V_{PP} pin status.

FLPMC is set by a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears this register to 08H.

Figure 7-4. Format of Flash Programming Mode Control Register (FLPMC)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
FLPMC	0	0	0	0	1	VPP	0	FLSPM0	FFCDH	08H ^{Note 1}	R/W ^{Note 2}

VPP	V _{PP} pin voltage application status
0	The voltage required for flash memory erase/write is not applied to V _{PP} pin.
1	Voltage greater than that of V _{DD} pin is applied to V _{PP} pin.

FLSPM0	Operating mode selection
0	Normal operating mode
1	Self-write mode

- Notes**
1. Bit 2 changes depending on the level of the V_{PP} pin.
 2. Bit 2 is read-only.

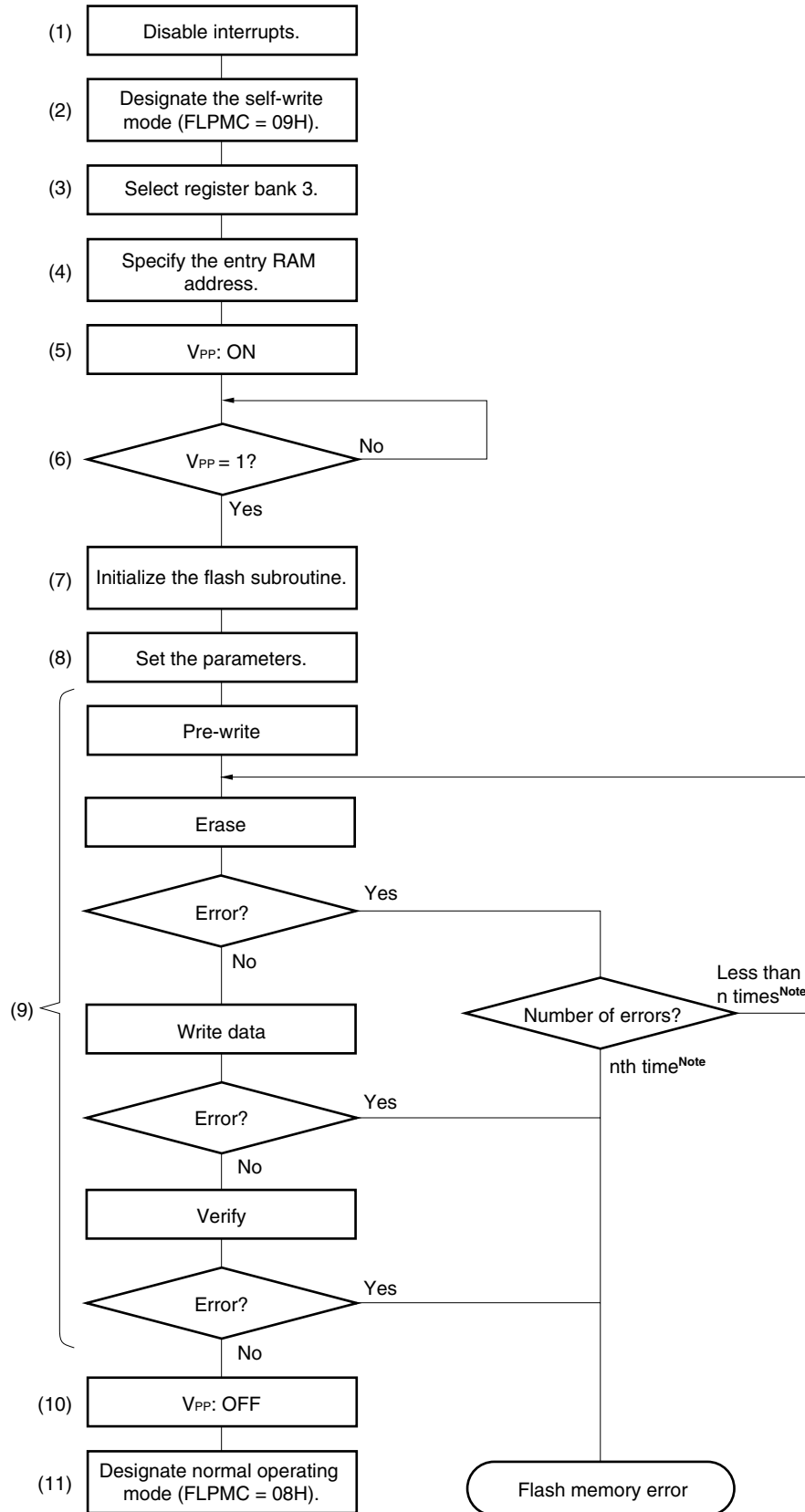
- Cautions**
1. Be sure to set bits 1 and bits 4 to 7 to 0, and set bit 3 to 1.
 2. The VPP bit indicates the status of the voltage applied to the V_{PP} pin. If the VPP bit is 0, the voltage required for erase/write is not applied. However, even if VPP bit is 1, it does not necessarily mean that the voltage required for erase/write is applied. Configure the hardware so that the voltage required for erase/write is applied to the V_{PP} pin.
Also, if software will be used in addition to hardware to check that the voltage required for erase/write is applied, provide an external hardware detection circuit and use its output.

(3) Self-write procedure

The procedure for performing self write is shown below (see Figure 7-5).

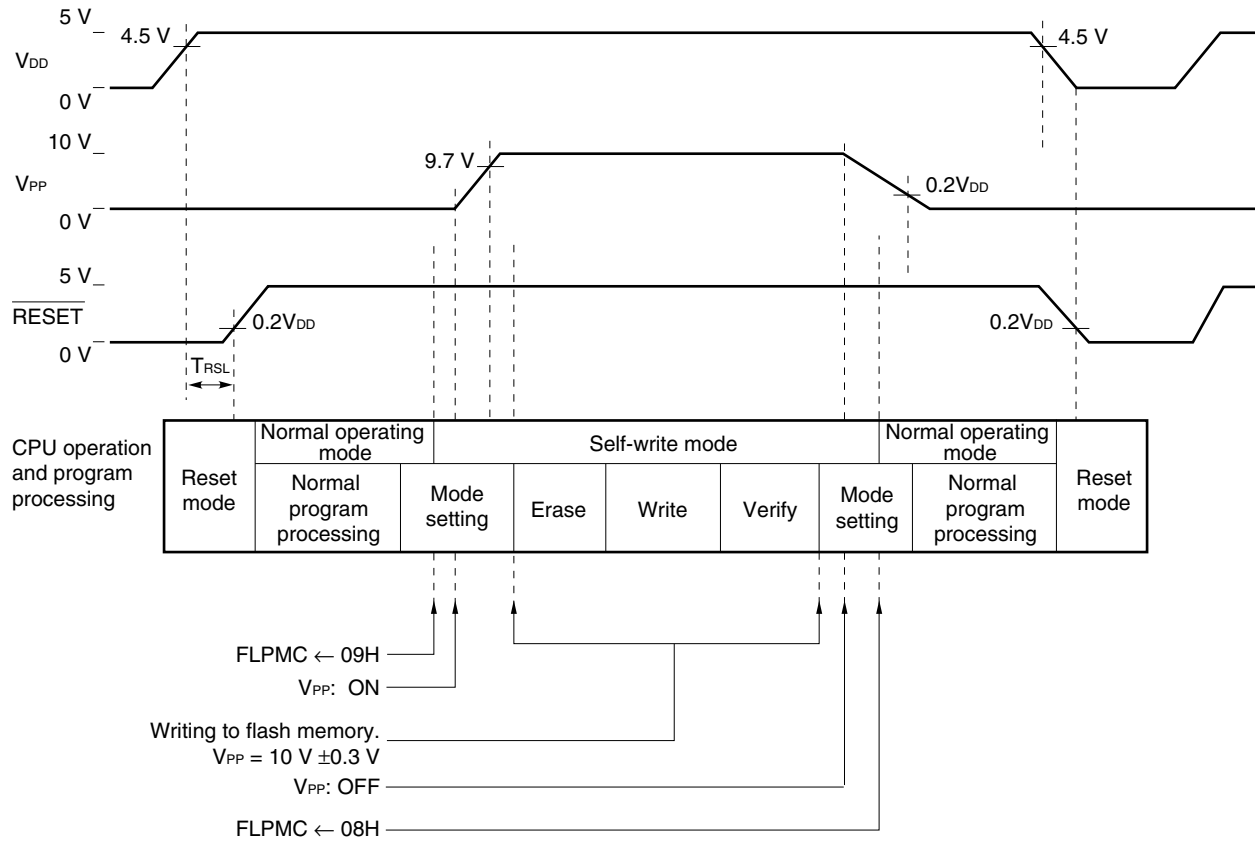
- (1) Disable interrupts.
- (2) Designate the self-write mode (FLPMC = 09H).
- (3) Select register bank 3.
- (4) Specify the start address of the entry RAM for the HL register.
- (5) V_{PP}: ON (ON signal for power supply IC)
- (6) Check the V_{PP} level.
- (7) Initialize the flash subroutine.
- (8) Set the parameters.
- (9) Control the flash memory (erase, write, etc.).
- (10) V_{PP}: OFF (OFF signal for power supply IC)
- (11) Designate the normal operating mode (FLPMC = 08H).

Figure 7-5. Self-Programming Flowchart



Note Differs depending on the user program.

Figure 7-6. Self-Write Timing



(4) CPU resources

The CPU resources used during self write are as follows:

- Register bank: BANK3 (8 bytes)
 B register: Status flag
 C register: Function number
 HL register: Entry RAM area start address
- Stack area: Maximum 16 bytes
- Write data storage area: 1 to 256 bytes
- Entry RAM area: 32 bytes
 RAM area used by the self-write subroutines.
 Can be specified by the user using the HL register.
- Status register

	7	6	5	4	3	2	1	0
Parameter setting error	—	—	Verify error	Write error	—	Blank check error	—	—

(5) Entry RAM area

A description of the entry RAM area is shown in Table 7-3.

Table 7-3. Entry RAM Area

Offset Value	Description
+0	Reserved area (1 byte)
+1	Reserved area (1 byte)
+2	Flash memory start address (2 bytes)
+4	Flash memory end address (2 bytes)
+6	Number of bytes written to flash memory (1 byte)
+7	Write time data (1 byte)
+8	Erase time data (3 bytes)
+11	Reserved area (3 bytes)
+14	Write data storage buffer start address (2 bytes)
+16	Total block number (1 byte)
+17	Total area number (1 byte)
+18	Reserved area (14 bytes)
.	
.	

Example When the value of the HL register of register bank 3 is 0FD00H
 0FD00H: Status
 0FD02H: Flash memory start address
 0FD06H: Number of bytes written to flash memory
 .
 .

Next, the entry RAM area will be explained in detail.

(a) Flash memory start address

This is the flash memory address value used by the _FlashByteWrite subroutine.

(b) Flash memory end address

This is the flash memory address value used by the _FlashGetInfo subroutine.

(c) Number of bytes written in flash memory

Area number and number of bytes written in the flash memory.

(d) Write time data

Set the following values based on the operating frequency.

f _x (MHz)	Setting Value
1.00 to 1.28	20H
1.29 to 2.56	40H
2.57 to 5.12	60H
5.13 to 8.38	80H

(e) Erase time data

Setting value = Erase time (s) × Operating frequency/2⁹ + 1
 (Erase time range: 0.5 to 20 seconds)

Example Erase time: 2 seconds, operating frequency: 4.19 MHz

$$\begin{aligned} \text{Setting value} &= 2 \times 4194304/512 + 1 \\ &= 16385 \text{ (decimal)} \\ &= 4001\text{H (hexadecimal)} \end{aligned}$$

(f) Write data storage buffer start address

This area contains the start address of the write data storage buffer area. The RAM data (write data), for which the data in this area is specified as the address, is written to the flash memory (_FlashByteWrite subroutine). The data in this area is specified as the start address and it is possible to specify up to a maximum of 256 bytes of write data.

(g) Total block number

This is the total flash memory block number used by the _FlashGetInfo subroutine.

(h) Total area number

This is the total flash memory area used by the _FlashGetInfo subroutine.

(6) Self-write subroutines

The self-write subroutines and their functions are shown in Table 7-4 below.

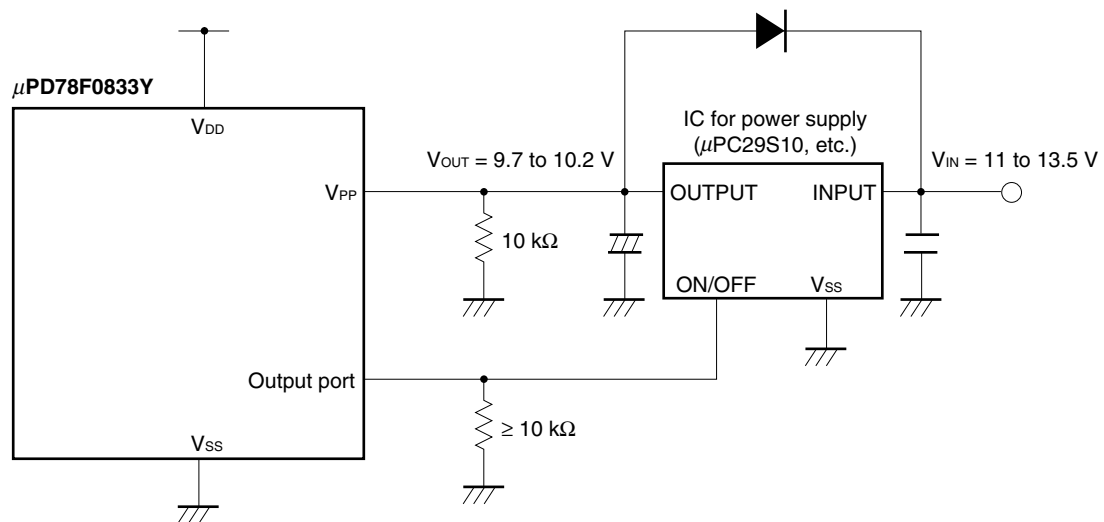
Table 7-4. List of Self-Write Subroutines

Function Number		Subroutine Name	Function
Decimal	Hexadecimal		
0	00H	_FlashEnv	Initializes the flash subroutine.
1	01H	_FlashSetEnv	Sets the parameters.
2	02H	_FlashGetInfo	Reads flash memory data
16	10H	_FlashAreaBlankCheck	Performs a blank check of a specified area.
32	20H	_FlashAreaPreWrite	Performs prewrite for a specified area.
48	30H	_FlashAreaErase	Erases a specified area.
80	50H	_FlashByteWrite	Writes continuously in byte units.
96	60H	_FlashAreaVerify	Performs internal verification of a specified area.

(7) Self-write circuit configuration

The configuration of the self-write circuit is shown in Figure 7-7.

Figure 7-7. Self-Write Circuit Configuration



8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V _{DD}	V _{DD} = AV _{DD} = AV _{REF}		-0.3 to +6.5	V
	AV _{DD}				V
	AV _{REF}				V
	V _{PP}			-0.3 to +10.5	V
	AV _{SS}			-0.3 to +0.3	V
Input voltage	V _{I1}	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, P80 to P87, P90 to P97, C2RX, X1, X2, RESET		-0.3 to V _{DD} + 0.3	V
	V _{I2}	P33	N-ch open-drain	-0.3 to +16	V
Output voltage	V _O	P00 to P07, P20 to P27, P30 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, P80 to P87, P90 to P97, C2TX		-0.3 to V _{DD} + 0.3	V
Analog input voltage	V _{AN}	ANI00 to ANI70 ANI01 to ANI71	Analog input pin	AV _{SS} - 0.3 to AV _{REF} + 0.3 and -0.3 to V _{DD} + 0.3	V
Output current, high	I _{OH}	Per pin for P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70, P73 to P75, P80 to P87, P90 to P97, C2TX		-10	mA
		Total for all pins		-30	mA
Output current, low ^{Note}	I _{OL}	Per pin for P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, P80 to P87, P90 to P97, C2TX	Peak value	20	mA
			rms value	10	mA
		P33	Peak value	30	mA
			rms value	15	mA
		Total for all pins	Peak value	100	mA
			rms value	60	mA
Operating ambient temperature	T _A	During normal operation		-40 to +85	°C
		During flash memory programming		+10 to +40	°C
Storage temperature	T _{stg}			-65 to +150	°C

Note The rms value should be calculated as follows:

$$[\text{rms value}] = [\text{Peak value}] \times \sqrt{\text{Duty}}$$

Caution Product quality may suffer if the absolute maximum rating is exceeded for even single parameter or even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions ensuring that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

System Clock Oscillator Characteristics (T_A = -40 to 85°C, V_{DD} = 4.5 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f _x) ^{Note 1}		4.0		8.4	MHz
		Oscillation stabilization time ^{Note 2}				4	ms
Crystal resonator		Oscillation frequency (f _x) ^{Note 1}		4.0		4.2	MHz
		Oscillation stabilization time ^{Note 2}				10	ms

Notes 1. Indicates only oscillator characteristics.

2. Time required to stabilize oscillation after reset or STOP mode release.

Caution When using the system clock oscillator, wiring in the area enclosed with the broken line in the above figures should be carried out as follows to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a line through which a high fluctuating current flows.
- Always keep the ground point of the oscillator to the same potential as V_{SS1}.
- Do not ground the capacitor to a ground pattern in which a high current flows.
- Do not fetch signals from the oscillator.

Remark For the resonator selection and oscillator constant, users are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{IN}	f = 1 MHz Unmeasured pins returned to 0 V.			15	pF
Output capacitance	C _{OUT}	f = 1 MHz Unmeasured pins returned to 0 V.			15	pF
I/O capacitance	C _{IO}	f = 1 MHz Unmeasured pins returned to 0 V.			15	pF
					20	pF

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = -40 to +85°C, V_{DD} = AV_{DD} = AV_{REF} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V _{IH1}	P21, P25, P31, P34, P40 to P47, P64 to P67, P70 to P73, P80 to P87, P90 to P97		0.7V _{DD}		V _{DD}	V
	V _{IH2}	P00 to P07, P20, P22 to P24, P26, P27, P30, P32, P35, P36, P74, P75, RESET		0.8V _{DD}		V _{DD}	V
	V _{IH3}	P50 to P57		2.3		V _{DD}	V
	V _{IH4}	P33 (N-ch open-drain)		0.7V _{DD}		15	V
	V _{IH5}	X1, X2		V _{DD} - 0.5		V _{DD}	V
	V _{IH6}	C2RX		0.8V _{DD}		V _{DD} + 0.2	V
Input voltage, low	V _{IL1}	P21, P25, P31, P34, P40 to P47, P64 to P67, P70 to P73, P80 to P87, P90 to P97		0		0.3V _{DD}	V
	V _{IL2}	P00 to P07, P20, P22 to P24, P26, P27, P30, P32, P35, P36, P74, P75, C2RX, RESET		0		0.2V _{DD}	V
	V _{IL3}	P50 to P57		0		0.75	V
	V _{IL4}	P33 (N-ch open-drain)		0		0.3V _{DD}	V
	V _{IL5}	X1, X2		0		0.4	V
Output voltage, high	V _{OH1}	I _{OH} = -1 mA	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70, P73 to P75, P80 to P87, P90 to P97, C2TX	V _{DD} - 1.0		V _{DD}	V
	V _{OH2}	I _{OH} = -100 μA		V _{DD} - 0.5		V _{DD}	V
Output voltage, low	V _{OL1}	I _{OL} = 15 mA	P33		0.4	2.0	V
	V _{OL2}	I _{OL} = 1.6 mA	P71, P72			0.4	V
	V _{OL3}	I _{OL} = 1 mA	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70, P73 to P75, P80 to P87, P90 to P97, C2TX			1.0	V
	V _{OL4}	I _{OL} = 500 μA				0.5	V
Input leakage current, high	I _{LIH1}	V _{IN} = V _{DD}	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, P80 to P87, P90 to P97, C2RX, RESET			3	μA
	I _{LIH2}		X1			20	μA
	I _{LIH3}	V _{IN} = 15 V	P33			80	μA
Input leakage current, low	I _{LIL1}	V _{IN} = 0 V	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, P80 to P87, P90 to P97, C2RX, RESET			-3	μA
	I _{LIL2}		X1			-20	μA
	I _{LIL3}		P33			-3 ^{Note}	μA

Note A low-level input leakage current of -200 μA (MAX.) flows only for 1 clock after a read instruction has been executed to P33 or port 33 (P33). At times other than this 1-clock interval a -3 μA (MAX.) current flows.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = -40 to +85°C, V_{DD} = AV_{DD} = AV_{REF} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output leakage current, high	I _{LOH}	V _{OUT} = V _{DD}	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70, P73 to P75, P80 to P87, P90 to P97, C2TX			3	μA
Output leakage current, low	I _{LOL}	V _{OUT} = 0 V	P00 to P07, P20 to P27, P30 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, P80 to P87, P90 to P97, C2TX			-3	μA
Software pull-up resistor	R ₁	V _{IN} = 0 V	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70, P73 to P75	15	30	90	kΩ
Supply current ^{Note 1}	I _{DD1}	4.19 MHz crystal oscillation operation mode ^{Note 2}			6	12	mA
		8.38 MHz crystal oscillation operation mode ^{Note 2}			11	22	mA
	I _{DD2}	4.19 MHz crystal oscillation HALT mode ^{Note 3}			400	700	μA
		8.38 MHz crystal oscillation HALT mode ^{Note 3}			700	1,200	μA
	I _{DD3}	STOP mode			0.1	30	μA

- Notes**
1. Total current flowing in the internal power supply (V_{DD1} and V_{SS1}). AV_{REF}, AV_{DD}, and port current (on-chip pull-up resistor) are not included.
 2. During high-speed mode operation (when the processor clock control register (PCC) is set to 00H).
 3. During low-speed mode operation (when the processor clock control register (PCC) is set to 04H). The WTN0 operating current and the receive wait state operating current of the CLASS2 signal (when bits 5 and 4 (C2SC1 and C2SC0) of the class2 clock selection register (C2CLK) are set to 00B) are included.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation (T_A = -40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (Minimum instruction execution time)	T _{CY}	Using ceramic resonator	0.238		8	μs
		Using crystal resonator	0.476		8	μs
TI000, TI010, TI001, TI011 input high-/low-level width	t _{TIH0} t _{TIL0}		$2/f_{sam}$ + 0.1 ^{Note}			μs
TI50, TI51, TI52 input frequency	f _{TI5}		0		2.5	MHz
TI50, TI51, TI52 input high-/low-level width	t _{TIH5} t _{TIL5}		160			ns
Interrupt request input high-/low-level width	t _{INTH} t _{INTL}	INTP0 to INTP7, P40 to P47	10			μs
$\overline{\text{RESET}}$ low-level width	t _{RSL}		10			μs

Note Selection of $f_{sam} = f_x, f_x/4, f_x/64$ is available with bits 0 and 1 (PRM0n0, PRM0n1) of prescaler mode register 0n (PRM0n). However, if the TI00n valid edge is selected as the count clock, the value becomes $f_{sam} = f_x/8$ (n = 0, 1).

(2) Serial interface (T_A = -40 to +85°C, V_{DD} = 4.5 to 5.5 V)

(a) SIO3 3-wire serial I/O mode (internal clock output): SIO30, SIO31

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK3}}$ cycle time	t _{KCY1}		952			ns
$\overline{\text{SCK3}}$ high-/low-level width	t _{KH1} , t _{KL1}		t _{KCY1} /2 - 50			ns
SI3 setup time (to $\overline{\text{SCK3}}\uparrow$)	t _{SIK1}		100			ns
SI3 hold time (from $\overline{\text{SCK3}}\uparrow$)	t _{KSI1}		400			ns
Delay time from $\overline{\text{SCK3}}\downarrow$ to SO3 output	t _{KSO1}	C = 100 pF ^{Note}			300	ns

Note C is the load capacitance of the $\overline{\text{SCK3}}$ and SO3 output lines.

(b) SIO3 3-wire serial I/O mode (external clock input): SIO30, SIO31

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK3}}$ cycle time	t _{KCY2}		800			ns
$\overline{\text{SCK3}}$ high-/low-level width	t _{KH2} , t _{KL2}		400			ns
SI3 setup time (to $\overline{\text{SCK3}}\uparrow$)	t _{SIK2}		100			ns
SI3 hold time (from $\overline{\text{SCK3}}\uparrow$)	t _{KSI2}		400			ns
Delay time from $\overline{\text{SCK3}}\downarrow$ to SO3 output	t _{KSO2}	C = 100 pF ^{Note}			300	ns

Note C is the load capacitance of the SO3 output line.

(c) UART0 (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					131,250	bps

(d) UART0 (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK0 cycle time	t _{KCY3}		800			ns
ASCK0 high-/low-level width	t _{KH3} , t _{KL3}		400			ns
Transfer rate					39,063	bps

(e) I²C bus mode

Parameter		Symbol	Standard Mode		High-Speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f _{SCL}	0	100	0	400	kHz
Bus free time (between stop and start condition)		t _{BUF}	4.7		1.3		μs
Hold time ^{Note 1}		t _{HD:STA}	4.0		0.6		μs
SCL0 clock low-level width		t _{LOW}	4.7		1.3		μs
SCL0 clock high-level width		t _{HIGH}	4.0		0.6		μs
Start/restart condition setup time		t _{SU:STA}	4.7		0.6		μs
Data hold time	CBUS compatible master	t _{HD:DAT}	5.0		—	—	μs
	I ² C bus		0 ^{Note 2}		0 ^{Note 2}	0.9 ^{Note 3}	μs
Data setup time		t _{SU:DAT}	250		100 ^{Note 4}		ns
SDA0 and SCL0 signal rise time		t _R		1,000		300	ns
SDA0 and SCL0 signal fall time		t _F		300		300	ns
Stop condition setup time		t _{SU:STO}	4.0		0.6		μs
Capacitive load per each bus line		C _b		400		400	pF

- Notes**
1. Upon occurrence of the start condition, the first clock pulse is generated after hold period.
 2. To fill the undefined area of the SCL0 falling edge, it is necessary for the device to internally provide a SDA0 signal (on V_{IHmin.} of SCL0 signal) with at least 300 ns of hold time.
 3. If the device does not extend the SCL0 signal low hold time (t_{LOW}), only the maximum data hold time t_{HD:DAT} needs to be fulfilled.
 4. The high-speed-mode I²C bus is available in the standard-mode I²C bus system. At this time, the conditions described below must be satisfied.
 - If the device does not extend the SCL0 signal low state hold time
t_{SU:DAT} ≥ 250 ns
 - If the device extends the SCL0 signal low state hold time
Be sure to transmit the next data bit to the SDA0 line before the SCL0 line is released (t_{Rmax.} + t_{SU:DAT} = 1,000 + 250 = 1,250 ns by standard mode I²C bus specification).

(3) CLASS2 (T_A = -40 to +85°C, V_{DD} = 4.5 to 5.5 V)

(a) Internal clock count limit

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Internal clock cycle time	t _{CCLK}		467		510	ns

(b) In normal mode

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Rise transfer delay time (from C2TX↑ to C2RX↑)	t _{PDR}				62 t _{CCLK}	μs
Fall transfer delay time (from C2TX↓ to C2RX↓)	t _{PDF}				62 t _{CCLK}	μs

(c) In ×4 speed mode

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Rise transfer delay time (from C2TX↑ to C2RX↑)	t _{PDRX}				8 t _{CCLK}	μs
Fall transfer delay time (from C2TX↓ to C2RX↓)	t _{PDFX}				8 t _{CCLK}	μs

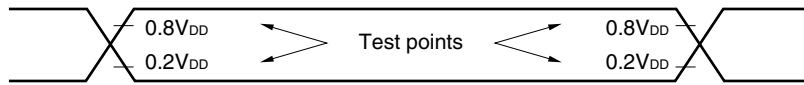
(d) Transmit and receive pulse width (in normal mode)

Symbol	t _{XMIN}	t _{XNOM}	t _{XMAX}	t _{RMIN}	t _{RMAX}	Unit
When Passive "0", Active "1"	60	64	68	37	91 or lower	μs
When Passive "1", Active "0"	122	128	134	100	157 or lower	μs
When Active "SOF"	193	200	207	170	230	μs
When Passive "EOF"	271	280	289	249	320 or lower	μs
Idle point				320 or higher	8 t _{CCLK}	μs
When Active "Break"	768			249 or higher		μs

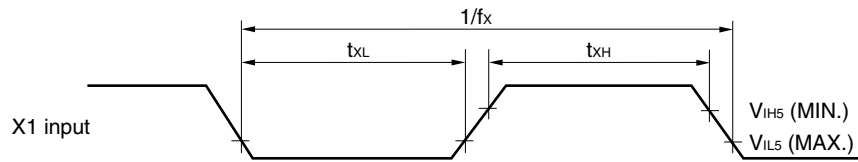
(e) Transmit and receive pulse width (in ×4 speed mode)

Symbol	t _{XMIN}	t _{XNOM}	t _{XMAX}	t _{RMIN}	t _{RMAX}	Unit
When Passive "0", Active "1"	15	16	17	10	22	μs
When Passive "1", Active "0"	30	32	34	25	39	μs
When Active "SOF"	48	50	52	43	57	μs
When Passive "EOF"	68	70	72	63	80	μs
Idle point				80	8 t _{CCLK}	μs
When Active "Break"	768			63		μs

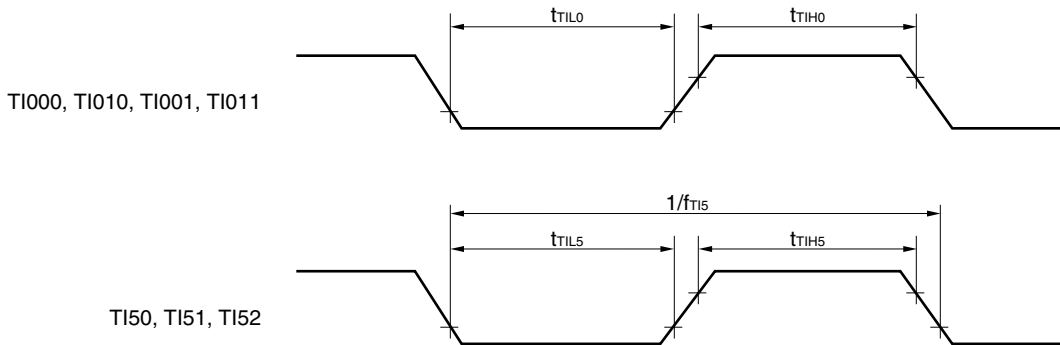
AC Timing Test Points (Excluding X1 Input)



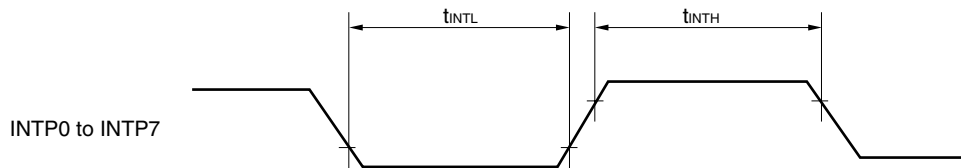
Clock Timing



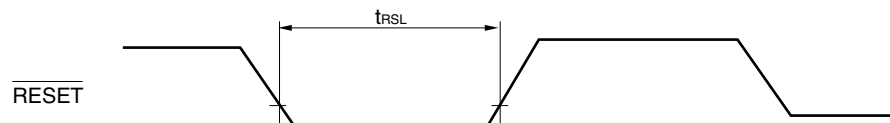
TI Timing



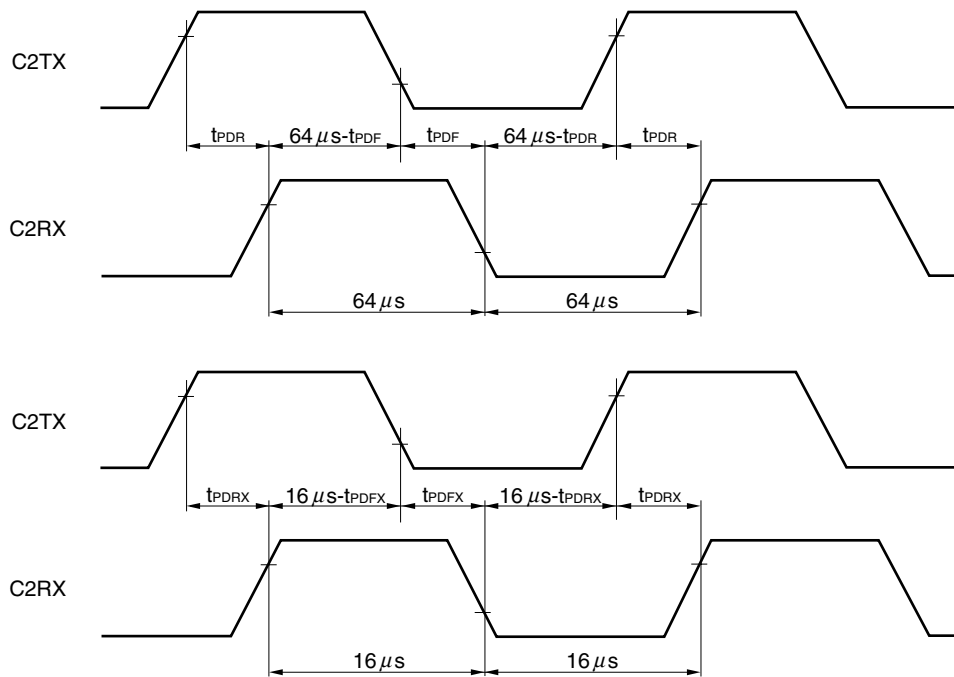
Interrupt Request Input Timing



RESET Input Timing



CLASS2 Transfer Waveform (Example of Short Pulse Width)



Remarks 1. The meanings of the symbols in above figure are as follows.

- t_{PDR} : CLASS2 transceiver rise transfer delay time in normal mode
- t_{PDF} : CLASS2 transceiver fall transfer delay time in normal mode
- t_{PDRX} : CLASS2 transceiver rise transfer delay time in ×4 speed mode
- t_{PDFX} : CLASS2 transceiver fall transfer delay time in ×4 speed mode

2. The values of t_{PDR} , t_{PDF} , t_{PDRX} , and t_{PDFX} can be specified using the class 2 rise transfer delay time correct register (C2PDR) and the class 2 fall transfer delay time correct register (C2PDF).

A/D Converter Characteristics (T_A = -40 to +85°C, V_{DD} = AV_{DD} = AV_{REF} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error ^{Note}					±0.6	%FSR
Conversion time	t _{CONV}		14		100	μs
Analog input voltage	V _{IAN}		AV _{SS}		AV _{REF}	V
AV _{REF} resistance	R _{AIREF}		9.5	15	37	kΩ

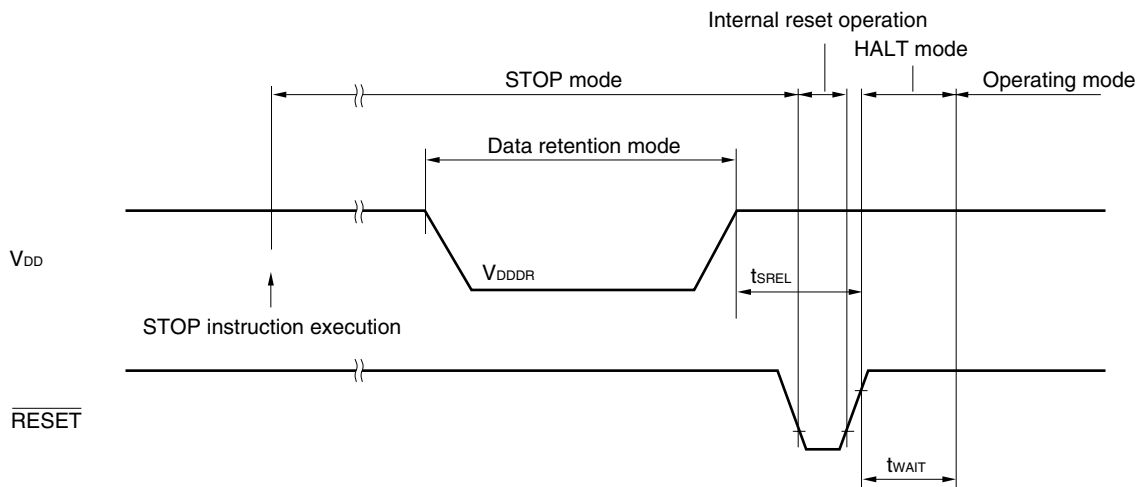
Note Excluding quantization error (±1/2%FSR). This value is indicated as a ratio to the full-scale value.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = -40 to +85°C)

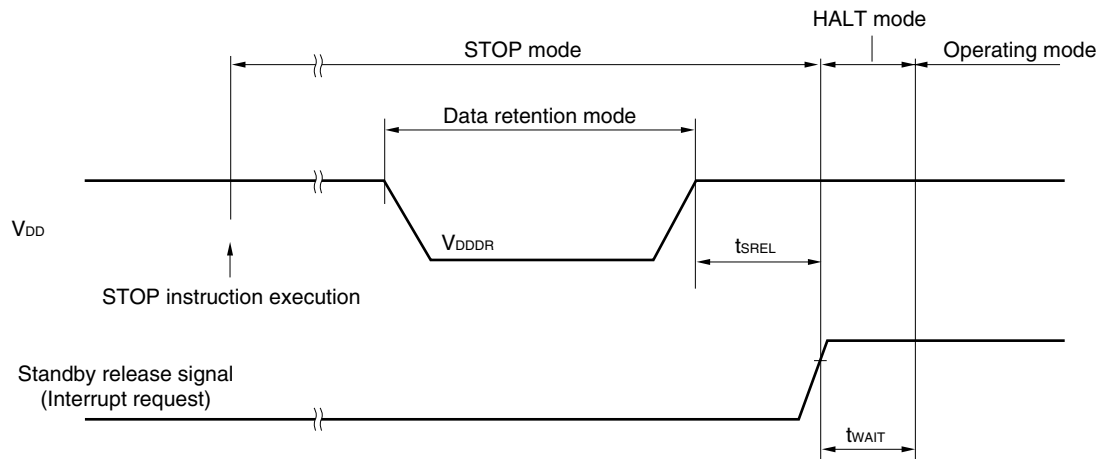
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V _{DDDR}		2.0		5.5	V
Data retention power supply current	I _{DDDR}	V _{DDDR} = 2.0 V		0.1	10	μA
Release signal set time	t _{SREL}		0			μs
Oscillation stabilization wait time	t _{WAIT}	Release by $\overline{\text{RESET}}$		2 ¹⁷ /f _x		ms
		Release by interrupt request		Note		ms

Note Selection of 2¹²/f_x, 2¹⁴/f_x, 2¹⁵/f_x, 2¹⁶/f_x, and 2¹⁷/f_x is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)



Flash Memory Programming Characteristics (V_{DD} = 2.7 to 5.5 V, V_{SS} = 0 V, V_{PP} = 9.7 to 10.3 V)

(1) Basic Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V _{DD} supply voltage	V _{DD}	Operating voltage during write operation	4.5		5.5	V
V _{PP} supply voltage	V _{PPL}	When detecting V _{PP} low level	0		0.2V _{DD}	V
	V _{PP}	When programming flash memory	9.7	10.0	10.3	V
V _{PP} supply current	I _{PP}	V _{PP} = 10.0 V			100	mA
Programming temperature	T _{PRG}		+10		+40	°C
Write time	C _{WRT}	T _{PRG} = +10 to +40°C	20	20	20	Times

Remark The operating clock range in flash memory programming mode is the same as in normal operating mode.

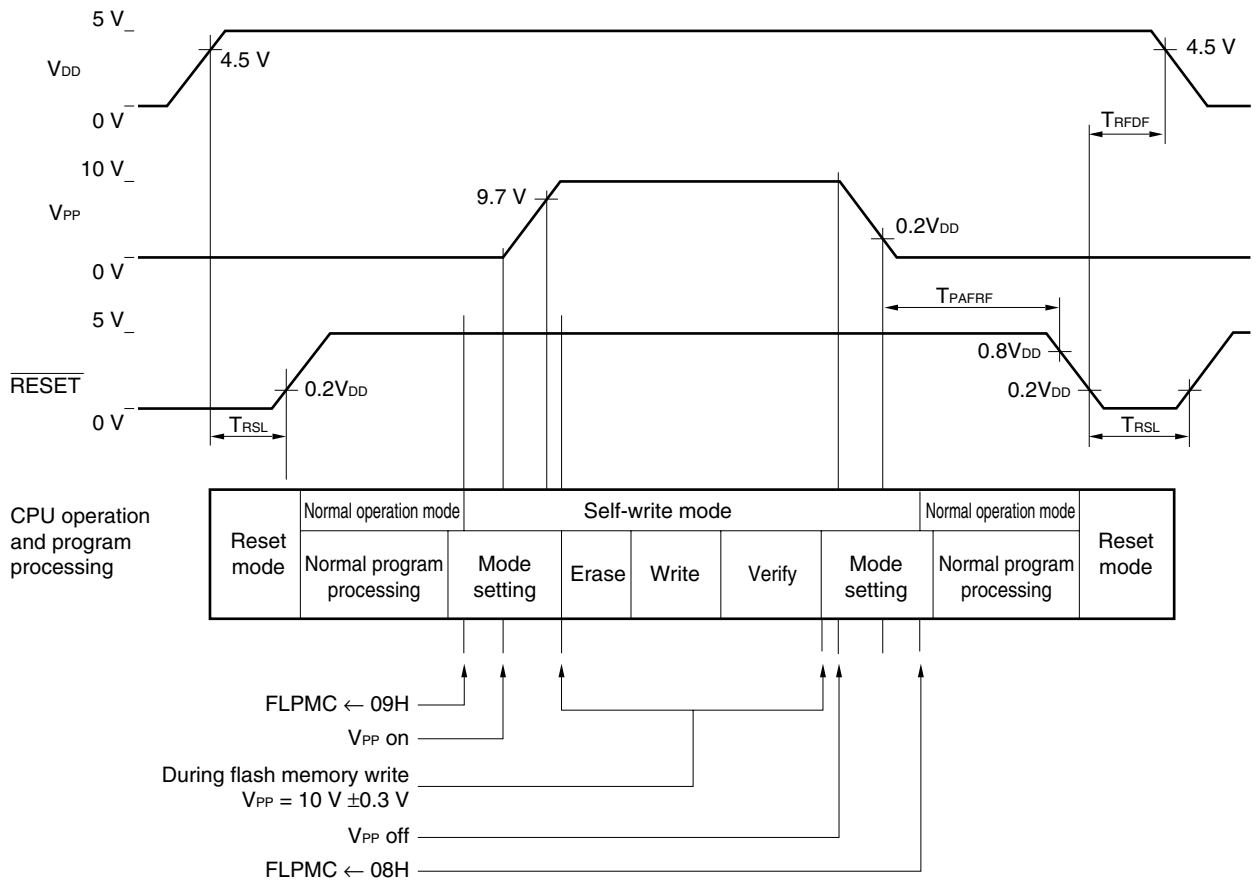
(2) Write Operation Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V _{PP} set time	t _{PSRON}	V _{PP} high voltage	1.0			μs
Set time from V _{DD} ↑ to V _{PP} ↑	t _{DRPSR}	V _{PP} high voltage	1.0			μs
Set time from V _{PP} ↑ to RESET↑	t _{PSRRF}	V _{PP} high voltage	1.0			μs
Time from RESET↑ to V _{PP} count start	t _{RFCF}		1.0			μs
Count execution time	t _{COUNT}				2.0	ms
V _{PP} counter high-/low-level width	t _{CH} , t _{CL}		8.0			μs
V _{PP} counter noise elimination width	t _{NFW}			40		ns

(3) Self-Programming Characteristics

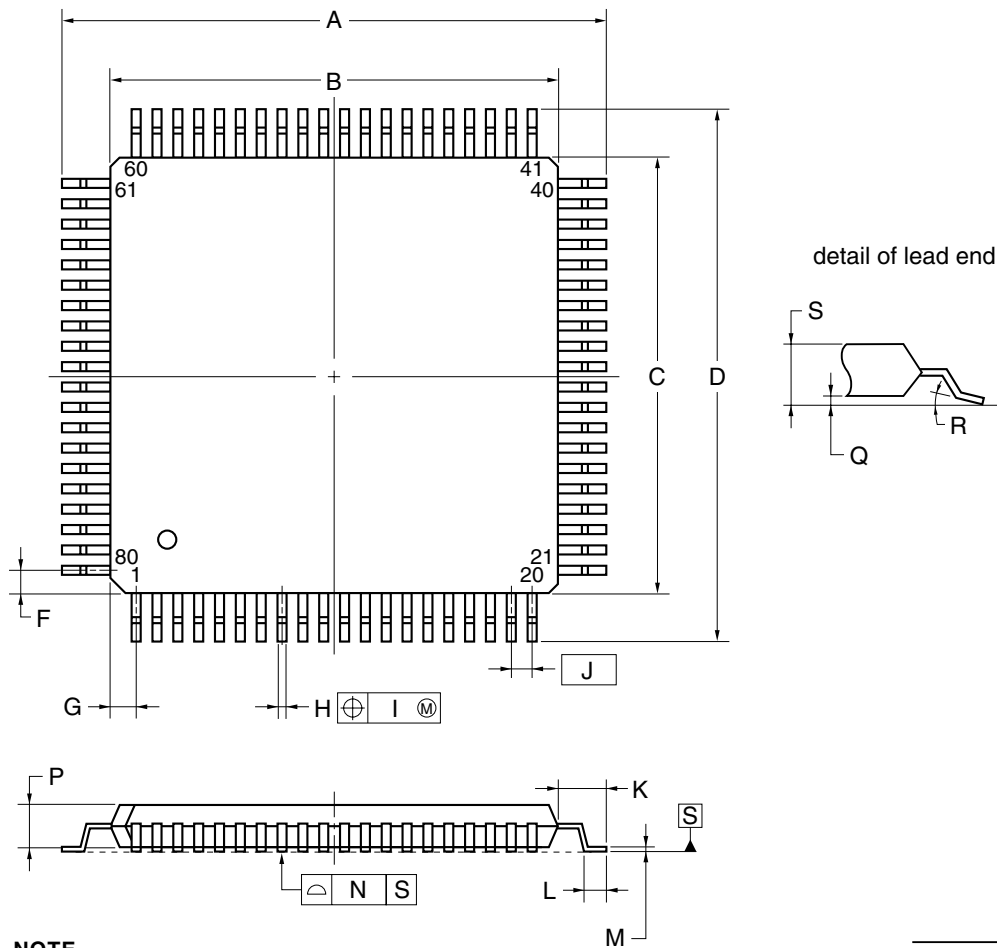
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time from V _{PP} ↓ to RESET↑	t _{PAFRF}		0			μs
Time from RESET↓ to V _{DD}	t _{RDFD}		0			μs

Flash Write Mode Setting Timing



9. PACKAGE DRAWING

80-PIN PLASTIC QFP (14x14)



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.20±0.20
B	14.00±0.20
C	14.00±0.20
D	17.20±0.20
F	0.825
G	0.825
H	0.32±0.06
I	0.13
J	0.65 (T.P.)
K	1.60±0.20
L	0.80±0.20
M	0.17 ^{+0.03} _{-0.07}
N	0.10
P	1.40±0.10
Q	0.125±0.075
R	3° ^{+7°} _{-3°}
S	1.70 MAX.

P80GC-65-8BT-1

10. RECOMMENDED SOLDERING CONDITIONS

The μPD78F0833Y should be soldered and mounted under the following recommended conditions. For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 10-1. Surface Mounting Type Soldering Conditions

μPD78F0833YGC-8BT: 80-pin plastic QFP (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Three times or less, Exposure limit: 7 days ^{Note} (after that, prebake at 125°C for 10 hours)	IR35-107-3
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Three times or less, Exposure limit: 7 days ^{Note} (after that, prebake at 125°C for 10 hours)	VP15-107-3
Wave soldering	Solder bath temperature: 260°C max., Time 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature), Exposure limit 7 days ^{Note} (after that, prebake at 125°C for 10 hours)	WS60-107-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78F0833Y.
 Also refer to (5) **Cautions on using development tools.**

(1) Language Processing Software

RA78K0	Assembler package common to 78K/0 Series
CC78K0	C compiler package common to 78K/0 Series
DF780833	Device file for μPD780833Y Subseries
CC78K0-L	C compiler library source file common to 78K/0 Series

(2) Flash Memory Writing Tools

Flashpro II (FL-PR2), Flashpro III (FL-PR3, PG-FP3)	Flash programmer dedicated to on-chip flash memory microcontroller
FA-80GC	Adapter for flash memory writing used with connected to Flashpro II or Flashpro III. 80-pin plastic QFP (GC-8BT type).

(3) Debugging Tools

• **When using in-circuit emulator IE-78K0-NS**

IE-78K0-NS	In-circuit emulator common to 78K/0 Series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-70000-98-IF-C	Interface adapter when using PC-9800 series as host machine (excluding notebook PCs) (C bus supported)
IE-70000-CD-IF-A	PC card and interface cable when using notebook PC as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT™ compatible as host machine (ISA bus supported)
IE-70000-PCI-IF-A	Adapter necessary when using on-chip PCI bus PC as host machine
IE-780833-NS-EM4	Emulation board to emulate μPD780833Y Subseries
IE-78K0-NS-P02	I/O board necessary when using IE-780833-NS-EM4
NP-80GC	Emulation probe for 80-pin plastic QFP (GC-8BT type)
EV-9200GC-80	Conversion socket for connecting target system board designed to mount an 80-pin plastic QFP (GC-8BT type) and NP-80GC
ID78K0-NS	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series
DF780833	Device file common to μPD780833Y Subseries

• When using in-circuit emulator IE-78001-R-A

IE-78001-R-A	In-circuit emulator common to 78K/0 Series
IE-70000-98-IF-C	Interface adapter when using PC-9800 series as host machine (excluding notebook PCs) (C bus supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT compatible as host machine (ISA bus supported)
IE-70000-PCI-IF	Adapter necessary when using on-chip PCI bus PC as host machine
IE-78000-R-SV3	Interface adapter and cable when using EWS as host machine
IE-780833-NS-EM4	Emulation board to emulate μPD780833Y Subseries
IE-78K0-NS-P02	I/O board necessary to use IE-780833-NS-EM4
IE-78K0-R-EX1	Emulation probe conversion board necessary to use IE-780833-NS-EM4 + IE-78K0-NS-P02 on IE-78001-R-A
EP-78230GC-R	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
EV-9200GC-80	Conversion socket to connect target system board for 64-pin plastic QFP (GC-AB8 type) and EP-78230GC-R
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series
DF780833	Device file common to μPD780833Y Subseries

(4) Real-time OS

RX78K0	Real-time OS for 78K/0 Series
MX78K0	OS for 78K/0 Series

(5) Cautions on using development tools

- The ID78K0-NS, ID78K0, and SM78K0 are used in combination with the DF780833.
- The CC78K0 and RX78K0 are used in combination with the RA78K0 and the DF780833.
- The FL-PR2, FL-PR3, FA-80GC, and NP-80GC are products made by Naito Densai Machida Mfg. Co., Ltd. (TEL: +81-44-822-3813).
- For third-party development tools, see the **Single-Chip Microcontroller Development Tool Selection Guide (U11069E)**.
- The host machines and OSs supporting each software are as follows.

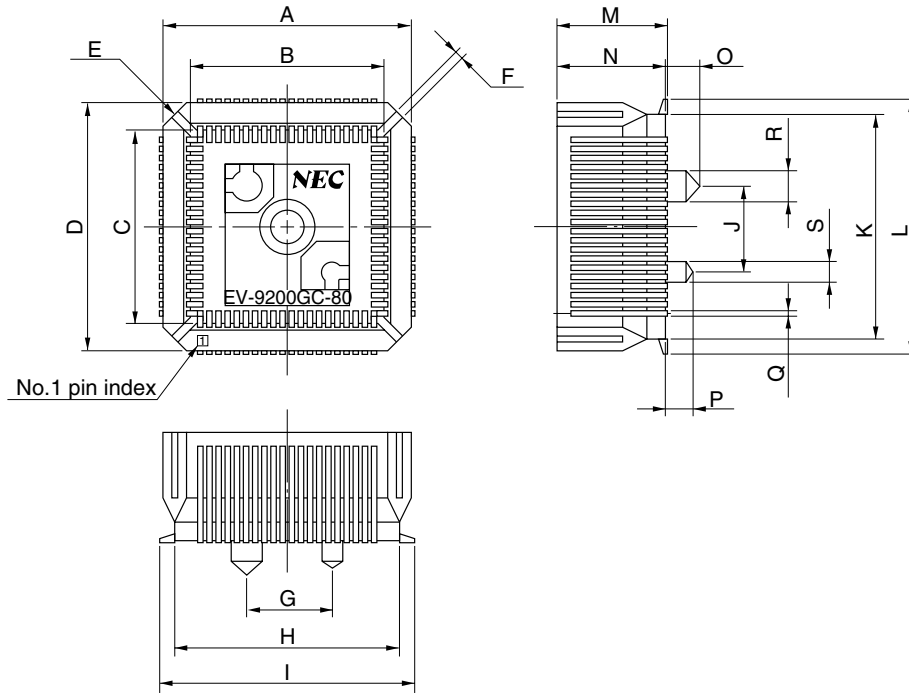
Software	Host Machine [OS]	PC	EWS
		PC-9800 series [Windows™] IBM PC/AT compatible [Japanese/English Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K0		√ Note	√
CC78K0		√ Note	√
ID78K0-NS		√	—
ID78K0		√	√
SM78K0		√	—
RX78K0		√ Note	√
MX78K0		√ Note	√

Note DOS-based software

Conversion Socket (EV-9200GC-80) Package Drawing and Recommended Board Mounting Pattern

Figure A-1. EV-9200GC-80 Package Drawing (for reference) (unit: mm)

Based on EV-9200GC-80
 (1) Package drawing (in mm)

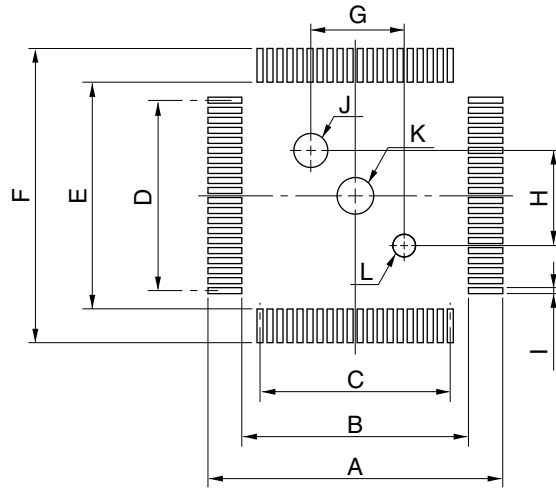


EV-9200GC-80-G0E

ITEM	MILLIMETERS	INCHES
A	18.0	0.709
B	14.4	0.567
C	14.4	0.567
D	18.0	0.709
E	4-C 2.0	4-C 0.079
F	0.8	0.031
G	6.0	0.236
H	16.0	0.63
I	18.7	0.736
J	6.0	0.236
K	16.0	0.63
L	18.7	0.736
M	8.2	0.323
O	8.0	0.315
N	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	φ2.3	φ0.091
S	1.5	0.059

Figure A-2. EV-9200GC-80 Recommended Board Mounting Pattern (for reference) (unit: mm)

Based on EV-9200GC-80
(2) Pad drawing (in mm)



EV-9200GC-80-P1E

ITEM	MILLIMETERS	INCHES
A	19.7	0.776
B	15.0	0.591
C	$0.65 \pm 0.02 \times 19 = 12.35 \pm 0.05$	$0.026^{+0.001}_{-0.002} \times 0.748 = 0.486^{+0.003}_{-0.002}$
D	$0.65 \pm 0.02 \times 19 = 12.35 \pm 0.05$	$0.026^{+0.001}_{-0.002} \quad 0.748 = 0.486^{+0.003}_{-0.002}$
E	15.0	0.591
F	19.7	0.776
G	6.0 ± 0.05	$0.236^{+0.003}_{-0.002}$
H	6.0 ± 0.05	$0.236^{+0.003}_{-0.002}$
I	0.35 ± 0.02	$0.014^{+0.001}_{-0.001}$
J	$\phi 2.36 \pm 0.03$	$\phi 0.093^{+0.001}_{-0.002}$
K	$\phi 2.3$	$\phi 0.091$
L	$\phi 1.57 \pm 0.03$	$\phi 0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD780833Y Subseries User's Manual	U13892E
μPD780833Y Data Sheet	U15012E
μPD78F0833Y Data Sheet	This document
78K/0 Series User's Manual Instructions	U12326E
78K/0, 78K/0S Series Application Note Flash Memory Write	U14458E

Documents Related to Development Tools (User's Manuals)

Document Name	Document No.	
RA78K0 Assembler Package	Operation	U11802E
	Language	U11801E
	Structured Assembly Language	U11789E
CC78K0 C Compiler	Operation	U11517E
	Language	U11518E
PG-FP3 Flash Memory Programmer	U13502E	
IE-78K0-NS	U13731E	
IE-78K0-R-EX1	To be prepared	
IE-780833-NS-EM4	To be prepared	
SM78K0S, SM78K0 System Simulator Windows Based	Operation	U14611E
SM78K Series System Simulator Ver. 2.10 or Later	External Part User Open Interface Specifications	To be prepared
ID78K0-NS Integrated Debugger Ver. 2.00 or Later Windows Based	Operation	U14379E
ID78K0 Integrated Debugger Windows Based	Guide	U11649E
	Reference	U11539E

Caution The above related documents are subject to change without notice. Be sure to read the latest documents before designing.

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No.
78K/0 Series Real-Time OS	Fundamentals	U11537E
	Installation	U11536E
78K/0 Series OS MX78K0	Fundamental	U12257E

Other Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The above related documents are subject to change without notice. Be sure to read the latest documents before designing.

[MEMO]

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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