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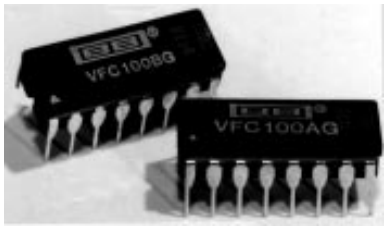


VFC100

Synchronized VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

- FULL-SCALE FREQUENCY SET BY SYSTEM CLOCK; NO CRITICAL EXTERNAL COMPONENTS REQUIRED
- PRECISION 10V FULL-SCALE INPUT, 0.5% max GAIN ERROR
- ACCURATE 5V REFERENCE VOLTAGE
- EXCELLENT LINEARITY:
  0.02% max at 100kHz FS
  0.1% max at 1MHz FS
- VERY LOW GAIN DRIFT: 50ppm/°C

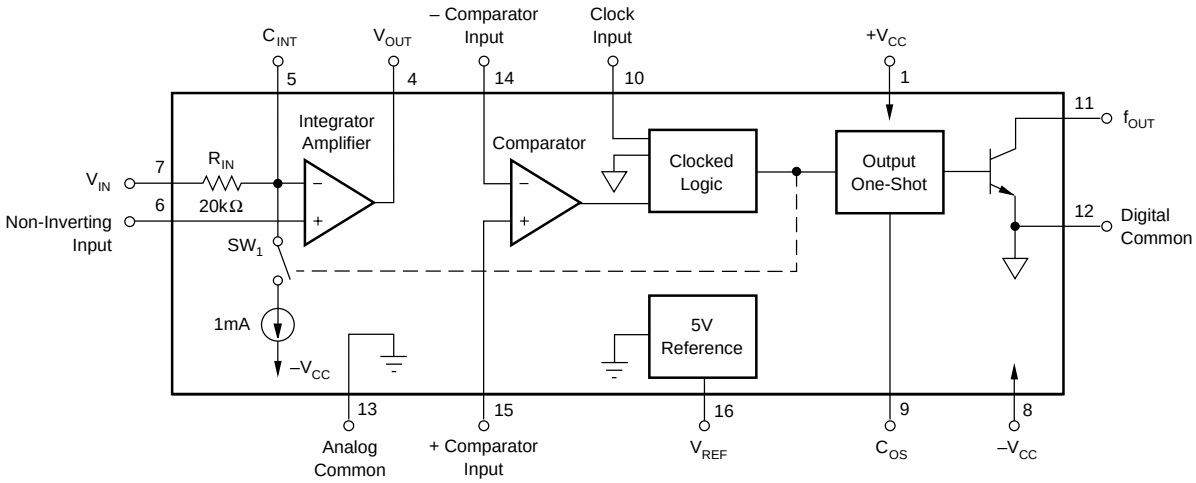
APPLICATIONS

- A/D CONVERSION
- PROCESS CONTROL
- DATA ACQUISITION
- VOLTAGE ISOLATION

DESCRIPTION

The VFC100 voltage-to-frequency converter is an important advance in VFCs. The well-proven charge balance technique is used; however, the critical reset integration period is derived from an external clock frequency. The external clock accurately sets an output full-scale frequency, eliminating error and drift from the external timing components required for other VFCs. A precision input resistor is provided which accurately sets a 10V full-scale input voltage. In many applications the required accuracy can be achieved without external adjustment.

The open collector active-low output provides fast fall time on the important leading edge of output pulses, and interfaces easily with TTL and CMOS circuitry. An output one-shot circuit is particularly useful to provide optimum output pulse widths for optical couplers and transformers to achieve voltage isolation. An accurate 5V reference is also provided which is useful for applications such as offsetting for bipolar input voltages, exciting bridges and sensors, and autocalibration schemes.



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SBVS018

SPECIFICATIONS

At T_A = +25°C and ±15VDC supplies, unless otherwise noted.

PARAMETER	CONDITIONS	VFC100AG			VFC100BG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TRANSFER FUNCTION								
Voltage-to-Frequency Mode	$f_{OUT} = f_{CLOCK} \times (V_{IN}/20V)$							
Gain Error[1]	FSR = 100kHz		±0.5	±1		±0.2	±0.5	% of FSR[4]
Linearity Error	FSR = 100kHz, Over Temperature		±0.01	±0.025		*	±0.02	% of FSR
	FSR = 500kHz, C_{OS} = 60pF		±0.015			*	±0.05	% of FSR
	FSR = 1MHz, C_{OS} = 60pF		±0.025			*	±0.1	% of FSR
Gain Drift[2]	FSR = 100kHz		±70	±100		±30	±50	ppm of FSR/°C
Referred to Internal V_{REF}			±70	±100		±30	±50	ppm of FSR/°C
Offset Referred to Input			±1	±3		±1	±2	mV
Offset Drift			±12	±100		±6.5	±25	µV/°C
Power Supply Rejection	Full Supply Range			0.01			*	%/V
Response Time	To Step Input Change	One Period of New Output Frequency Plus One Clock Period						
Current-to-Frequency Mode	$f_{OUT} = f_{CLOCK} \times (I_{IN}/1mA)$							
Gain Error			±0.5	±1		±0.2	±0.5	% of FSR
Gain Drift[2]			±120	±200		±80	±140	ppm of FSR/°C
Frequency-to-Voltage Mode[3]	$V_{OUT} = 20V \times (f_{IN}/f_{CLOCK})$							
Gain Accuracy[1]	FSR = 100kHz		±0.5	±1		±0.2	±0.5	%
Linearity	FSR = 100kHz		±0.01	±0.025		*	±0.02	%
Input Resistor (R_{IN})								
Resistance		19.8	20	20.2	*	*	*	kΩ
Temperature Coefficient (T_C)[2]			±50	±100		*	*	ppm°C
INTEGRATOR OP AMP								
V_{OS}[1]			±150	±1000		*	*	µV
V_{OS} Drift			±5			*		µV/°C
I_B			±50	±100		±25	±50	nA
I_{OS}			100	200		50	100	nA
A_{OL}	Z_{LOAD} = 5kΩ/10,000pF	100	120		*	*		dB
CMRR		80	105		*	*		dBV
CM Range		–7.5		+0.1	*		*	V
V_{OUT} Range	Z_{LOAD} = 5kΩ/10,000pF	–0.2		+12		*	*	V
Bandwidth			14			*		MHz
COMPARATOR INPUTS								
Input Current (Operating)	$-11V < V_{COMPARATOR} < +V_{CC} - 2V$			5			*	µA
CLOCK INPUT								
(Referred to Digital Common)								
Frequency (Maximum Operating)			4			*		MHz
Threshold Voltage			1.4			*		V
	Over Temperature	0.8		2	*		*	V
Voltage Range (Operating)		$-V_{CC}$ + 2V		$+V_{CC}$	*		*	V
Input Current	$-V_{CC} < V_{CLOCK} < +V_{CC}$		0.5	5		*	*	µA
Rise Time				2			*	µs
OPEN COLLECTOR OUTPUT								
(Referred to Digital Common)								
V_{OL}	I_{OUT} = 10mA			0.4			*	V
I_{OL}				15			*	mA
I_{OH} (Off Leakage)	V_{OH} = 30V		0.01	10		*	*	µA
Delay Time, Positive Clock								
Edge to Output Pulse			300			*		ns
Fall Time			100			*		ns
Output Capacitance			5			*		pF
OUTPUT ONE-SHOT								
Active[6]								
Pulse Width Out	C_{OS} = 300pF	1	1.4	2	*	*	*	µs
Deactivated[5]								
Pulse Width Out	100kHz ≤ FSR < 1MHz		$\frac{1}{4\ f_{CLOCK}}$			*		sec
Pulse Width Out	FSR = 1MHz	250	450	500	*	*	*	ns
REFERENCE VOLTAGE								
Accuracy	No Load	4.9	5	5.1	4.95	*	5.05	V
Drift[2]			±60	±150		±40	±100	ppm/°C
Current Output	Sourcing Capability	10				*		mA
Power Supply Rejection				0.015			0.015	%/V
Output Impedance			0.5	2		*	*	Ω

SPECIFICATIONS (CONT)

At T_A = +25°C and ±15VDC supplies, unless otherwise noted.

PARAMETER	CONDITIONS	VFC100AG			VFC100BG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
Rated Voltage			±15			*		V
Operating Voltage Range								
(See Figure 9)	$+V_{CC}$	+7.5		+28.5	*		*	V
	$-V_{CC}$	–7.5		–28.5	*		*	V
Total Supply	$+V_{CC} - (-V_{CC})$	15		36	*		*	V
Digital Common		$-V_{CC}$ + 2		$+V_{CC}$ – 4	*		*	V
Quiescent Current: $+I_{CC}$	Over Temperature		10.6	15		*	*	mA
$-I_{CC}$			9.6	15		*	*	mA
TEMPERATURE RANGE								
Specification		–25		+85	*		*	°C
Storage		–65		+150	*		*	°C
θ_{JA}			150			*		°C/W
θ_{JC}			100			*		°C/W

* Specification same as AG grade.

NOTES: (1) Offset and gain error can be trimmed to zero. See text. (2) Specified by the box method: (max. – min.) ÷ (FSR x ΔT). (3) Refer to detailed timing diagram in Figure 16 for frequency input signal timing requirements. (4) FSR = Full Scale Range. (5) Pin 9 connected to $+V_{CC}$. (6) Nominal PW_{OUT} = (5ns/pF) x C_{OS} – 90ns.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage ($+V_{CC}$ to $-V_{CC}$) 36V
$+V_{CC}$ to Analog Common 28V
$-V_{CC}$ to Analog Common 28V
Integrator Out Short-Circuit to Ground ..... Indefinite
Integrator Differential Input ..... ±10V
Integrator Common-Mode Input ..... $-V_{CC}$ +5V to +2V
V_{IN} (pin 7) ..... $\pm V_{CC}$
Clock Input ..... $\pm V_{CC}$
V_{REF} Out Short-Circuit to Ground ..... Indefinite
Pin 9 (C_{OS}) ..... 0 to $+V_{CC}$
f_{OUT} (referred to digital common) ..... –0.5V to 36V
Digital Common ..... $\pm V_{CC}$
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (soldering, 10s) ..... 300°C

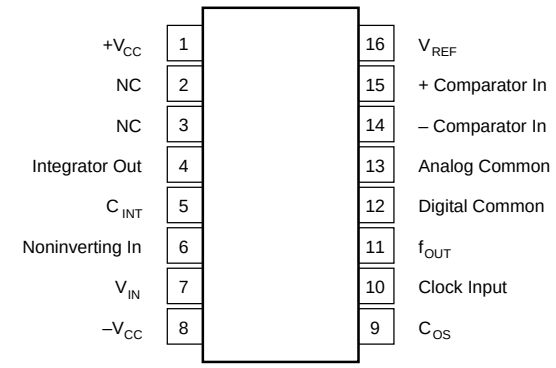
PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
VFC100AG	16-Pin Ceramic DIP	129
VFC100BG	16-Pin Ceramic DIP	129

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

PIN CONFIGURATION

Top View DIP



ELECTROSTATIC DISCHARGE SENSITIVITY

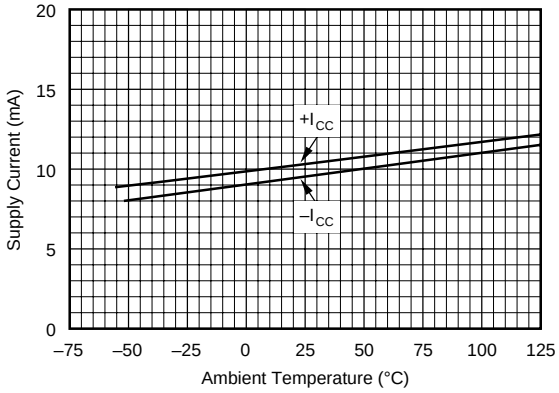
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

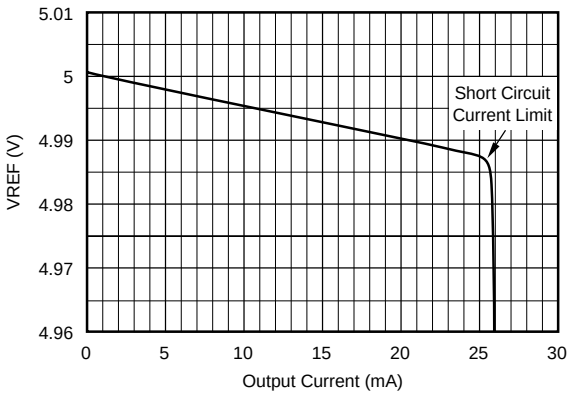
TYPICAL PERFORMANCE CURVES

At +25°C, $\pm V_{CC}$ = 15VDC, and in circuit of Figure 1.

QUIESCENT CURRENT vs TEMPERATURE



REFERENCE VOLTAGE vs REFERENCE LOAD CURRENT



THEORY OF OPERATION

The VFC100 monolithic voltage-to-frequency converter provides a digital pulse train output with an average frequency proportional to the analog input voltage. The output is an active low pulse of constant duration, with a repetition rate determined by the input voltage. Falling edges of the output pulses are synchronized with rising edges of the clock input.

Operation is similar to a conventional charge balance VFC. An input operational amplifier (Figure 1) is configured as an integrator so that a positive input voltage causes an input current to flow in R_{IN}. This forces the integrator output to ramp negatively. When the output of the integrator crosses the reference voltage (5V), the comparator trips, activating the clocked logic circuit. Once activated, the clocked logic awaits a falling edge of the clock input, followed by a rising edge (see Figure 2). On the rising edge, switch S_1 is closed for one complete clock cycle, causing the reset current, I_1, to switch to the integrator input. Since I_1 is larger than the input current, I_{IN}, the output of the integrator ramps positively during the one clock cycle reset period. The clocked logic circuitry also generates a VFC output pulse during the reset period.

Unlike conventional VFC circuits, the VFC100 accurately derives its reset period from an external clock frequency. This eliminates the critical timing capacitor required by other VFC circuits. One period (from rising edge to rising edge) of the clock input determines the integrator reset period.

When the negative-going integration of the input signal crosses the comparator threshold, integration of the input signal will continue until the reset period can start (awaiting

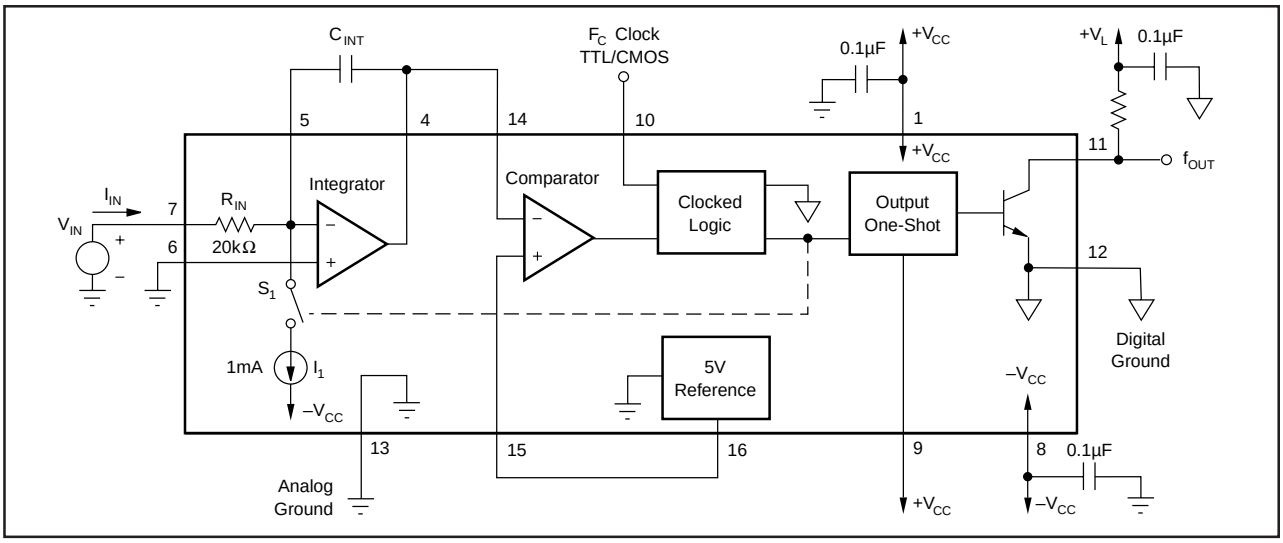


FIGURE 1. Circuit Diagram for Voltage-to-Frequency Mode.

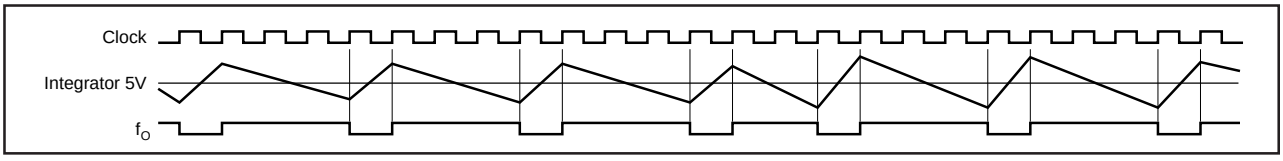


FIGURE 2. Timing Diagram for Voltage-to-Frequency Mode.

the necessary transitions of the clock). Output pulses are thus made to align with rising edges of the external clock. This causes the instantaneous output frequency to be a subharmonic of the clock frequency. The average frequency, however, will be an accurate analog of the input voltage.

A full scale input of 10V (or an input current of 0.5mA) causes a nominal output frequency equal to half the clock frequency. The transfer function is

$$f_{OUT} = (V_{IN}/20V)\ f_{CLOCK}.$$

Figure 3 shows the transfer function graphically. Note that inputs above 10V (or 0.5mA) do not cause an increase in the output frequency. This is an easily detectable indication of an overrange input. In the overrange condition, the integrator amplifier will ramp to its negative output swing limit. When the input signal returns to within the linear range, the integrator amplifier will recover and begin ramping upward during the reset period.

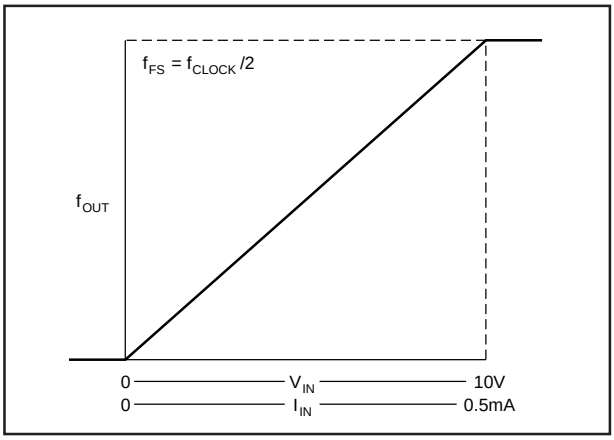


FIGURE 3. Transfer Function for Voltage-to-Frequency Mode.

INSTALLATION AND OPERATING INSTRUCTIONS

The integrator capacitor C_{INT} (see Figure 1) affects the magnitude of the integrator voltage waveform. Its absolute accuracy is not critical since it does not affect the transfer function. This allows a wide range of capacitance to produce excellent results. Figure 4 facilitates choosing an appropriate

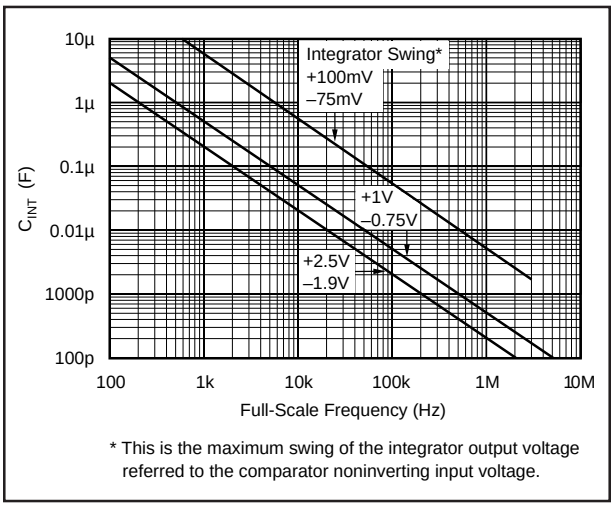


FIGURE 4. Integrator Capacitor Selection Graph.

standard value to assure that the integrator waveform voltage is within acceptable limits. Good dielectric absorption properties are required to achieve best linearity. Mylar®, polycarbonate, mica, polystyrene, Teflon® and glass types are appropriate choices. The choice in a given application will depend on the particular value and size considerations. Ceramic capacitors vary considerably from type to type and some produce significant nonlinearities. Polarized capacitors should not be used.

Deviation from the nominal recommended +1V to –0.75V integrator voltage (as controlled by the integrator capacitor value) is permissible and will have a negligible effect on VFC operation. Certain situations may make deviations from the suggested integrator swing highly desirable. Smaller integrator voltages, for instance, allow more "headroom" for averaging noisy input signals. The VFC is a fully integrating input converter, able to reject large levels of interfering noise. This ability is limited only by the output voltage swing range of the integrator amplifier. By setting a small integrator voltage swing using a large C_{INT} value, larger levels of noise can be integrated without integrator output saturation and loss of accuracy. For instance, with a 50kHz full-scale output and C_{INT} = 0.1µF, the circuit in Figure 1 can accurately average an input through the full 0 to 10V input range with 1Vp-p superimposed 60Hz noise.

The integrator output voltage should not be allowed to exceed +12V or –0.2V, otherwise saturation of the operational amplifier could cause inaccuracies. Operation with positive power supplies less than +15V will limit the output swing of the integrator operational amplifier. Smaller integrator voltage waveforms may be required to avoid output saturation of the integrator amplifier. See "Power Supply Considerations" for information on low voltage operation.

The maximum integrator voltage swing requirement is nearly symmetrical about the comparator threshold voltage (see Figure 12). One-third greater swing is required above the threshold than below it. Maximum demand on positive integrator swing occurs at low scale, while the negative swing is greatest just below full scale.

CLOCK INPUT

The clock input is TTL and CMOS-compatible. Its input threshold is approximately 1.4V (two diode voltage drops) referenced to digital ground (pin 12). The clock "high" input may be standard TLL or may be as high as $+V_{CC}$ – 2V. A CMOS clock should be powered from a voltage source at least 2V below the VFC100's $+V_{CC}$ to prevent overdriving the clock input. Alternatively, a resistive voltage divider may be used to limit the clock voltage swing to $+V_{CC}$ – 2V maximum. The clock input has a high input impedance, so no special drivers are required. Rise time in the transition region from 0.8V to 2V must be less than 2µs for proper operation.

OUTPUT

The frequency output is an open collector current-sink transistor. Output pulses are active low such that the output transistor is on only during the reset integration period (see "Shortened Output Pulses"). This minimizes power dissipation over the full frequency range and provides the fastest logic edge at the beginning of the output pulse, where it is most desirable.

Interface to a logic circuit would normally be made using a pull-up resistor to the logic power supply. Selection of the pull-up resistor should be made such that no more than 15mA flows in the output transistor. The actual choice of the pull-up resistor may depend on the full-scale frequency and the stray capacitance on the output line. The rising edge of an output pulse is determined by the RC time constant of the pull-up resistor and the stray capacitance. Excessive capacitance will produce a rounding of the output pulse rising edge, which may create problems driving some logic circuits. If long lines must be driven, a buffer or digital line transmitter circuit should be used.

The synchronized nature of the VFC100 makes viewing its output on an oscilloscope somewhat tricky. Since all output pulses align with the clock, it is best to trigger and view the clock on one of the input channels; the output can then be viewed on another oscilloscope channel. Depending on the VFC input voltage, the output waveform may appear as if the oscilloscope is not properly triggered. The output might best be visualized by imagining a constant output frequency which is locked to a submultiple of the clock frequency with occasional extra pulses or missing pulses to create the necessary average frequency. It is these extra or missing pulses that make the output waveform appear as if the oscilloscope is not properly triggered. This is normal. Experimentation with the input voltage and oscilloscope triggering generally allows a stable view of the output and provides an understanding of its nature.

SHORTENED OUTPUT PULSES

In normal operation, the negative output pulse duration is equal to one period of the clock input. Shorter output pulses may be useful in driving optical couplers or transformers for voltage isolation or noise rejection. This can be accomplished by connecting capacitor C_{OS} as shown in Figure 5. Pin 9 may be connected to $+V_{CC}$, deactivating the output one-shot circuit. The value of C_{OS} is chosen according to the curve in Figure 6. Output pulses cannot be made to exceed one clock period in duration. Thus, a C_{OS} value which would create an output pulse which is longer than one period of the clock will have the same effect as disabling the one-shot, causing the output pulse to last one clock period. The minimum practical pulse width of the one-shot circuit is approximately 100ns. Using C_{OS} to generate shorter output pulses does not affect the output frequency or the gain equation.

REFERENCE VOLTAGE

Excellent gain drift is achieved by use of a precision internal 5V reference. This reference is brought to an external pin and can be used for a variety of purposes. It is used to offset the noninverting comparator input in voltage-to-frequency mode (although a precise voltage is not required for this function). The reference is very useful for handling bipolar

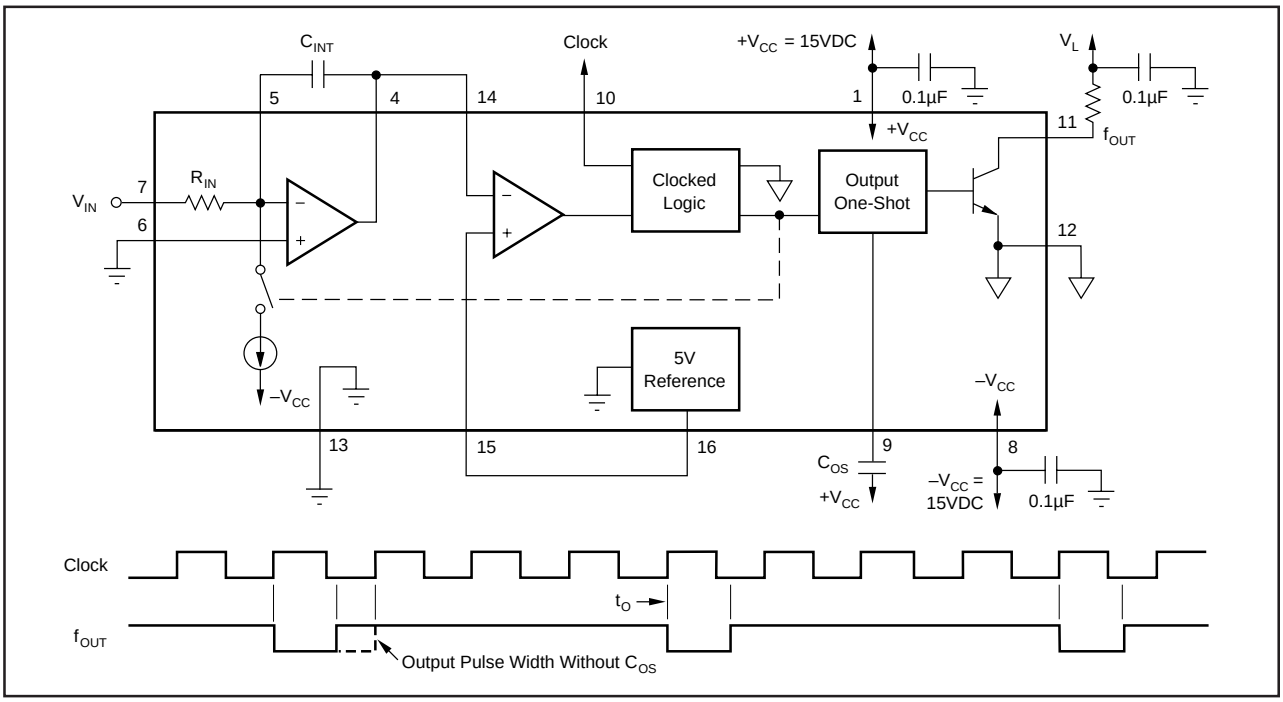


FIGURE 5. Circuit and Timing Diagram for Shortened Output Pulses.

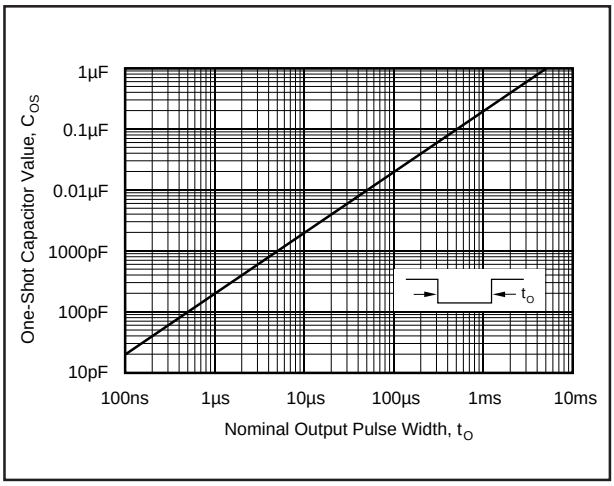


FIGURE 6. Output One-Shot Capacitor Selection.

input signals in many other applications, such as offsetting the input. It can source up to 10mA and sink 100µA. Heavy loading of the reference will change the gain of the VFC and affect the external reference voltage. For instance, a 10mA load interacting with a 0.5Ω typical output impedance will change the VFC gain equation and reference voltage by 0.1%.

Figure 7 shows the reference used to offset the VFC transfer function, to convert a –5V to +5V input to 0–500kHz output. The circuit in Figure 8 uses the reference to excite a 300Ω bridge transducer. R_1 provides the majority of the current to the bridge while the V_{REF} output supplies the balance and accurately controls the bridge voltage. The VFC gain is inversely proportional to the reference voltage, V_{REF}. Since the bridge gain is directly proportional to its excitation voltage, the two equal and opposite effects cancel the effect of reference voltage drift on gain.

The reference output amplifier is specifically designed for excellent transient response, to provide precision in a noisy environment.

OTHER INPUT VOLTAGE RANGES

The internal input resistor, R_{IN} = 20kΩ, sets a full-scale input of 10V. Other input ranges can be created by using an external gain set resistor connected to pin 5. Since the excellent temperature drifts of the VFC100 are achieved by careful matching of internal temperature coefficients, use of an external gain set resistor will generally degrade this drift. Using an external resistor to set the gain, the resulting gain drift would be equal to the sum of the external resistor drift and the specified current gain drift of the VFC100. Different voltage input ranges are best implemented by using the internal input resistor, R_{IN}, in series or parallel with a high quality external resistor, thus maintaining as much of the precision temperature tracking as possible.

For best drift performance, the adjustment range of a fine gain trim should be made as narrow as practical. R_1 and R_2 in Figure 9 allow gain adjustments over a ±1% range (adequate to trim the 100kHz FS gain error to zero) and will not significantly affect the drift performance of the VFC100. R_3, R_4 and R_5 allow trimming of the integrator amplifier input offset voltage. The adjustment range is determined by the ratio of R_4 to R_5. Accurate end-point calibration would be performed by first adjusting the offset trim so that zero volts input just causes all output pulses to cease. The gain trim is then adjusted for the proper full-scale output frequency with an accurate full-scale input voltage.

A different input voltage range could also be made by using only a portion of the normal input range of the VFC. For instance, a 2V full-scale input could be created by using the

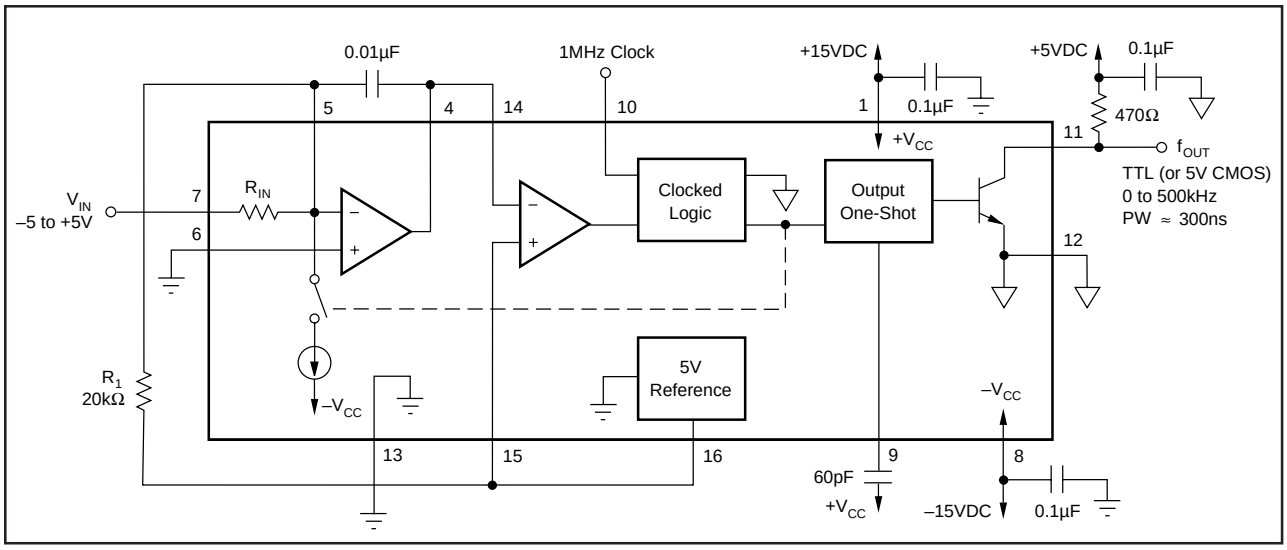


FIGURE 7. Circuit Diagram for Bipolar Input Voltages.

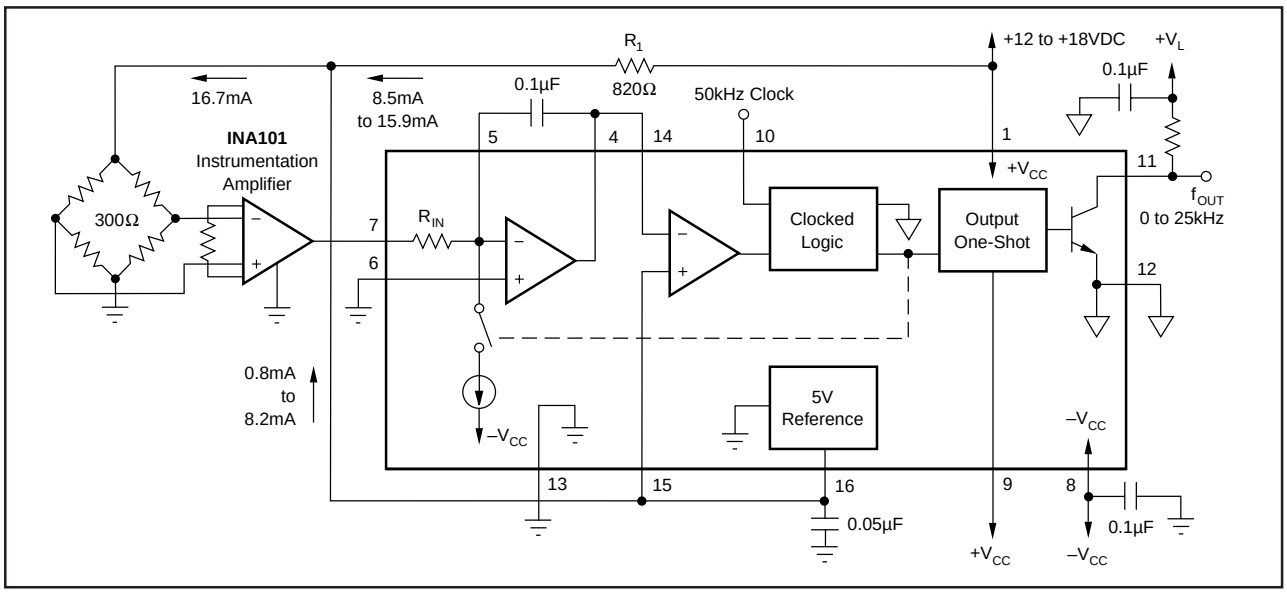


FIGURE 8. Circuit Diagram for Bridge Excitation Using V_{REF}.

internal input resistor and a clock frequency of 10 times the desired full-scale output frequency.

LINEARITY PERFORMANCE

The linearity of the VFC100 is specified as the worst-case deviation from a straight line defined by low scale and high scale end point measurements. This worst-case deviation is expressed as a percentage of the 10V full-scale input. All units are tested and guaranteed for the specified level of performance.

Linearity performance and gain error change with full-scale operating frequency as shown in Figure 10. Figure 11 shows the typical shape of the nonlinearity at 100kHz full scale. Integrator voltage swing (determined by C_{INT}) has a minor effect on linearity. A small integrator voltage swing typically leads to best linearity performance.

The best linearity performance at high full-scale frequencies (above 500kHz) is obtained by using short output pulses with a one-shot capacitor of 60pF. As with any high-frequency circuit, careful attention to good power supply bypassing techniques (see "Power Supplies and Grounding") is also required.

TEMPERATURE DRIFT

Conventional VFC circuits are affected significantly by external component temperature drift. Drift of the external input resistor and timing capacitor required with these devices may easily exceed the specified drift of the VFC itself.

When used with its internal input resistor, the gain drift of the complete VFC100 circuit is totally determined by the performance of the VFC100. Gain drift is specified at a full-scale output frequency of 100kHz. Conventional VFC circuits usually specify drift at 10kHz and degrade significantly

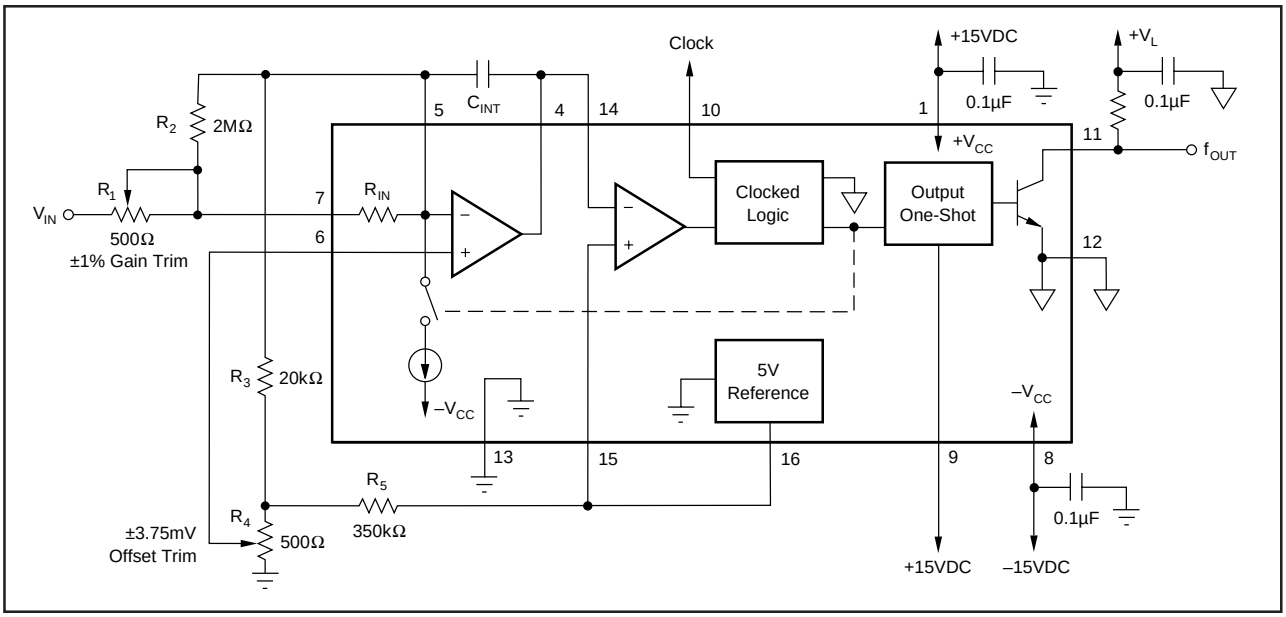


FIGURE 9. Circuit Diagram for Fine Offset and Gain Trim.

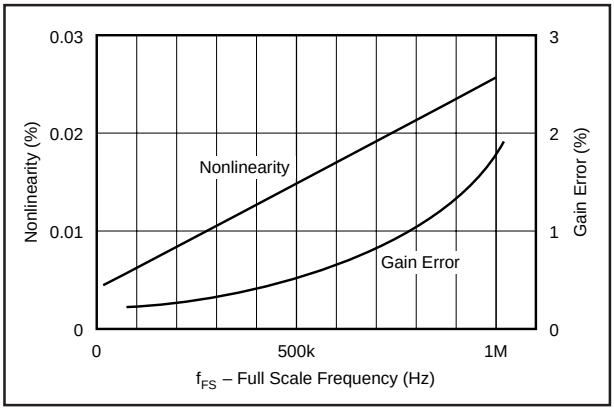


FIGURE 10. Typical Nonlinearity and Gain Error vs Full Scale Frequency.

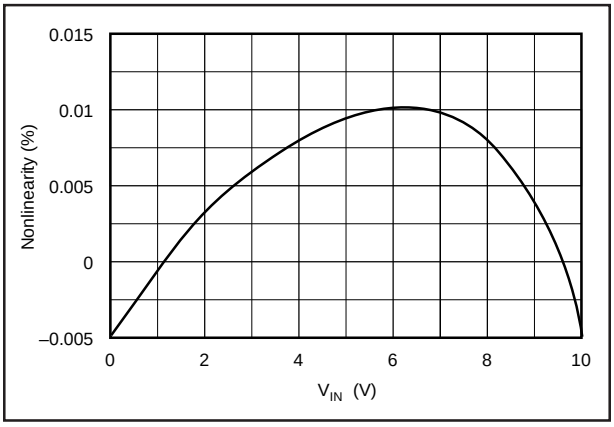


FIGURE 11. Typical Nonlinearity vs V_{IN}. (f_{FS} = 0.1MHz)

at higher operating frequency. The VFC100's gain drift remains excellent at higher operating frequency, typically remaining within specifications at f_{FS} = 1MHz.

Drift of the external clock frequency directly affects the output frequency, but by using a common clock for the VFC and counting circuitry, this drift can be cancelled (see "Counting the Output").

POWER SUPPLIES AND GROUNDING

Separate analog and digital grounds are provided on the VFC100 and it is important to separate these grounds to attain greatest accuracy. Logic sink current flowing in the f_{OUT} pin is returned to the digital ground. If this "noisy" current were allowed to flow in analog ground, errors could be created. Although analog and digital grounds may eventually be connected together at a common point in the circuitry, separate circuit connections to this common point can reduce the error voltages created by varying currents flowing through the ground return impedance. The +5V V_{REF} pin is referenced to analog ground.

The power supplies should be well bypassed using capacitors with low impedance at high frequency. A value of 0.1µF is adequate for most circuit layouts.

The VFC100 is specified for a nominal supply voltage of ±15V. Supply voltages ranging from ±7.5V to ±18V may be used. Either supply can be up to 28V as long as the total of both does not exceed 36V. Steps must be taken, however, to assure that the integrator output does not exceed its linear range. Although the integrator output is capable of 12V output swing with 15V power supplies, with 7.5V supplies, output swing will be limited to approximately 4.5V. In this case, the comparator input cannot be offset by directly connecting to the 5V reference output pin. The comparator input must be connected to a lower voltage point (approximately 2V). This allows the integrator output to operate around a lower voltage point, assuring linear operation. This threshold voltage does not affect the accuracy or drift of the VFC as long as it is not noisy. It should not be made too

small, however, or the negative output limitation of the integrator (–0.2V) may cause saturation. Additionally, a large integrator capacitor may be used to limit the required integrator waveform swing to approximately 100mV (see "Integrator Capacitor").

Figure 12 shows a circuit for operating from the minimum power supplies, avoiding saturation of the integrator amplifier and loss of accuracy. C_{INT} is chosen for a +100mV to –75mV integrator voltage swing (referred to the noninverting comparator input). The offset voltage applied to the comparator's noninverting input is derived from a resistive voltage divider from V_{REF}.

The relationship of the allowable operating voltage ranges on important pins is show in Figure 13. Note that the integrator amplifier output cannot swing more than 0.2V below ground. Although this is not "normal" for an operational amplifier, a special internal design of this type optimizes high frequency performance. It is this characteristic which necessitates the offsetting of the noninverting comparator input in voltage-to-frequency mode to avoid negative output swing.

COUNTING THE OUTPUT

In evaluation and use of the VFC100, you may want to measure the output frequency with a frequency counter. Since synchronization of the VFC100 causes it to await a clock edge for any given output pulse, the output frequency is essentially quantized. The quantized steps are equal to one clock period of the counting gate period. The quantizing error can be made arbitrarily small by counting with long gate times. For instance, a one-second counter gate period with a 100kHz full-scale frequency has a resolution of one part in 100,000. Many of the more sophisticated laboratory frequency counters, however, use period measurement schemes to count the input frequency quickly. These instruments work equally well, but the gate period must be set appropriately to achieve the desired count resolution. Short gate periods will produce many digits of "accuracy" in the display, but the results may be very inaccurate.

Figure 14 is a typical system application showing a basic counting technique. A 0 to 10V input is converted to a 0 to 100kHz frequency output. The VFC's clock is divided by M = 4000 to produce a gate period for the counter circuit. The resulting VFC count, N, is insensitive to variations in the actual clock frequency. The input voltage represented by the resulting count is V_{IN} = (N/M) 20V.

Resolution is related to the number of counts at full scale, or half the number of clock pulses in the gate period.

The integrating nature of the VFC is important in achieving accurate conversions. The integrating period is equal to the counting period. This can be used to great advantage to reject unwanted signals of a known frequency. Figure 15 shows that response nulls occur at the inverse of the integration period and its multiples. If 60Hz is to be rejected, for instance, the counting period should be made equal to, or a multiple of, 1/60 of a second.

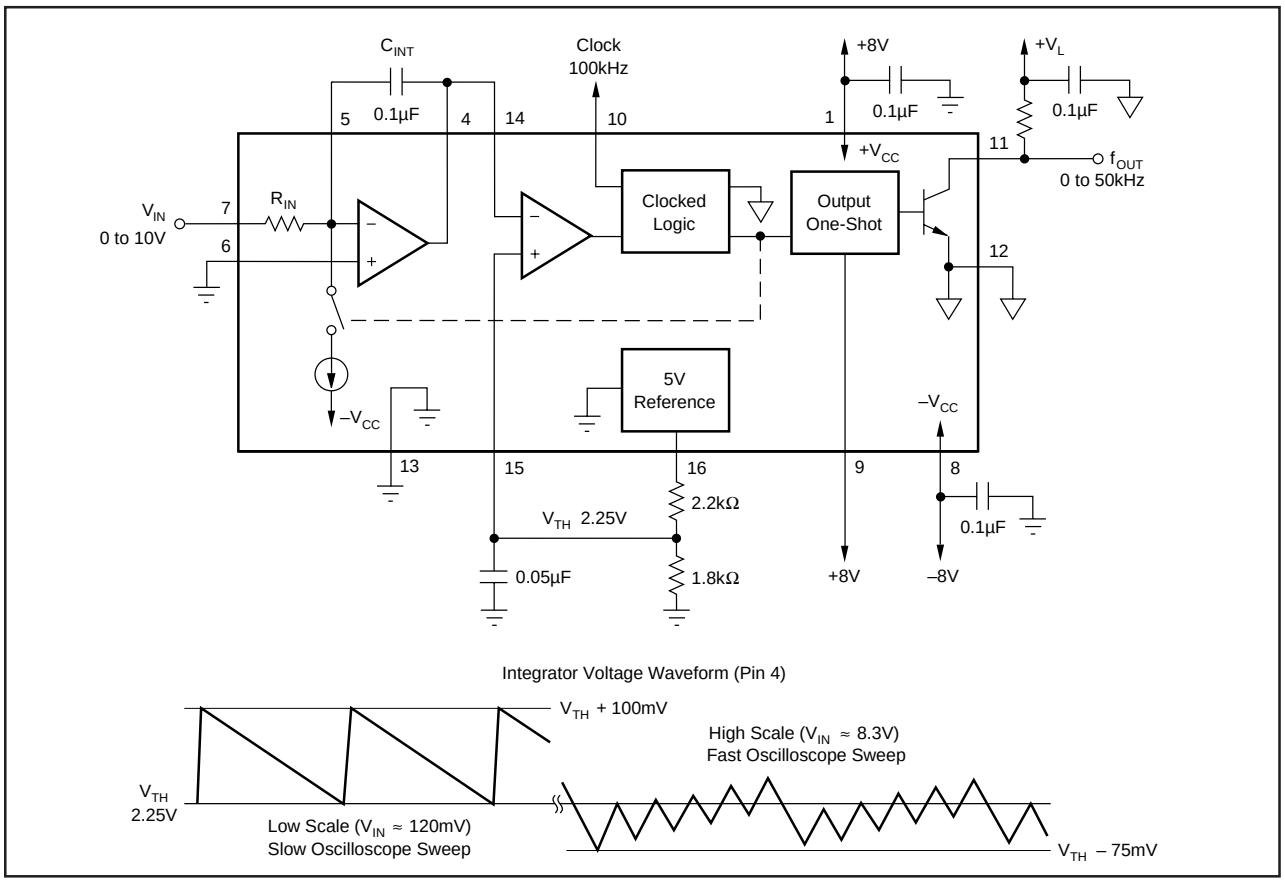


FIGURE 12. Circuit Diagram and Integrator Voltage Waveform Power Supply Voltage Operation.

FREQUENCY-TO-VOLTAGE MODE

The VFC100 can also function as a frequency-to-voltage converter by supplying an input frequency to the comparator input as shown in Figure 16. The input resistor, R_{IN}, is connected as a feedback resistor. The voltage at the integrator amp output is proportional to the ratio of the input frequency to the clock frequency. The transfer function is $V_{OUT} = (F_{IN}/f_{CLOCK})\ 20V$.

This transfer function is complementary to the voltage-to-frequency mode transfer function, making voltage-to-frequency-to-voltage conversions simple and accurate.

Direct coupling of the input frequency to the comparator is easily accomplished by driving both comparators with complementary frequency input signals. Alternatively, one of the comparator inputs can be biased at half the logic voltage (using V_{REF} and a voltage divider) and the other input driven directly.

The proper timing of the input frequency waveform is shown in Figure 16. The input pulse should go low for one clock cycle, centered around a falling edge of the clock. The minimum acceptable input pulse width must fall no later than 200ns before a negative clock edge and rise no sooner

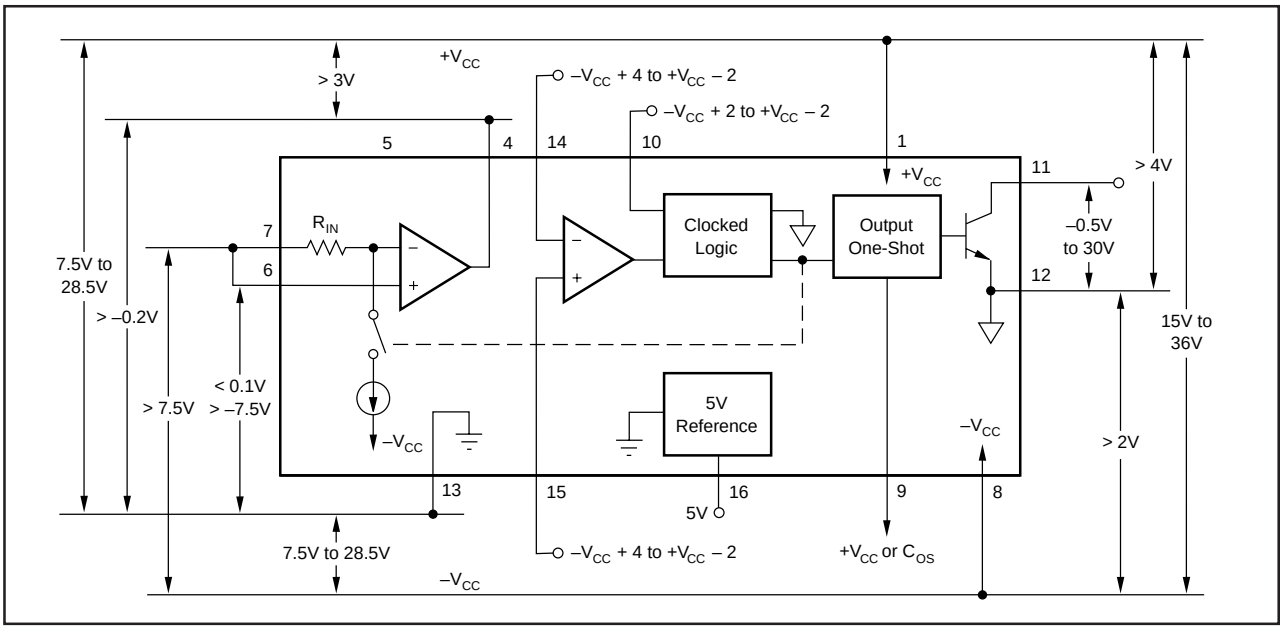


FIGURE 13. Relationships of Allowable Voltages.

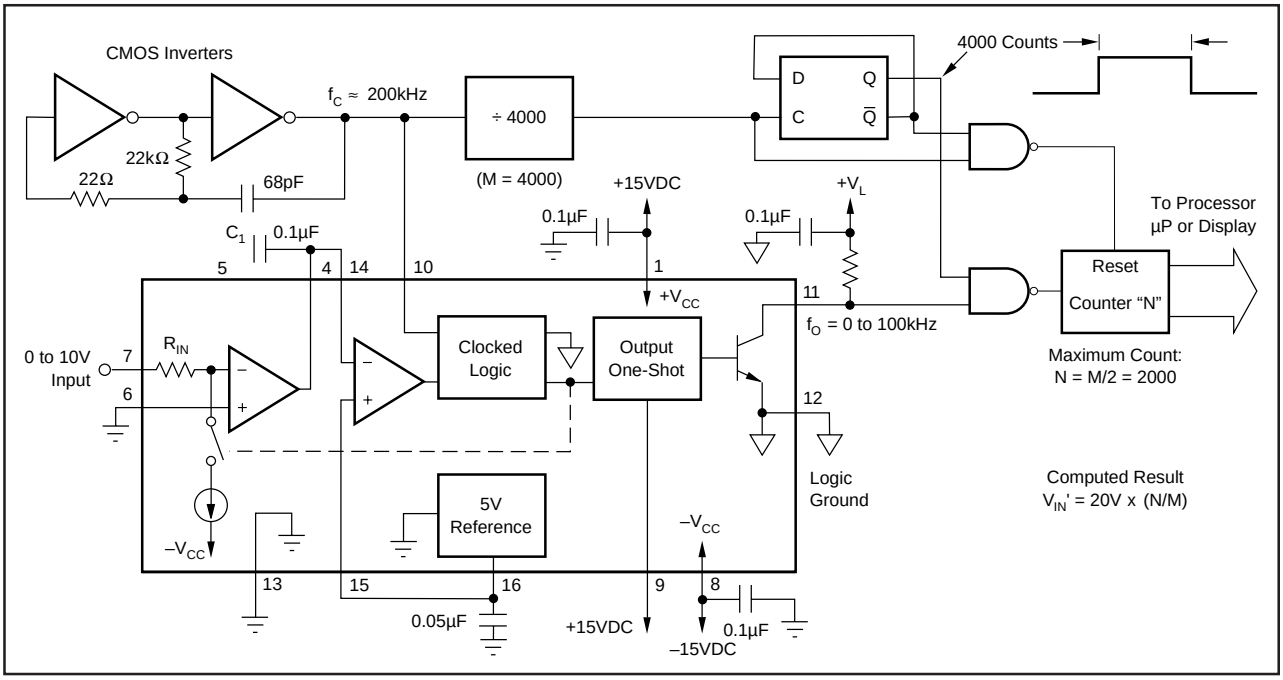


FIGURE 14. Diagram of a Voltage-to-Frequency Converter and Counter System.

than 200ns after the falling clock edge. An input pulse which remains low for more than one falling edge of the clock will produce incorrect output voltages. Positive (active high) input pulses can be accepted by reversing the connections to pins 14 and 15. Figure 17 shows a digital conditioning circuit which will accept any input duty cycle and provide the proper pulse width to the comparator. Each rising edge at this circuit's input generates the required negative pulse at the inverting comparator input. The noninverting comparator is driven by a complementary signal.

The integrator amplifier output is designed to drive up to 10,000pF and 5kΩ loads in frequency-to-voltage mode. This allows driving long lines in a large system.

Ripple voltage in the voltage output is unavoidable and is inversely proportional to the value of the integrator capacitor. Figure 18 shows the output ripple and settling time as a function of the C_{INT} value.

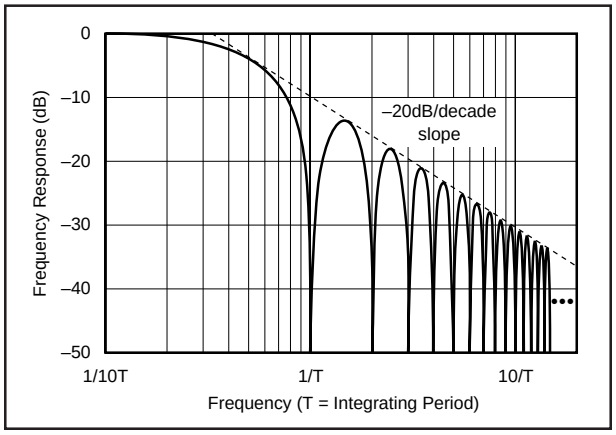


FIGURE 15. Frequency Response of an Integrating Analog-to-Digital Converter.

The ripple frequency is equal to the input frequency. Its magnitude can be reduced by using a large integrator capacitor value, but at the sacrifice of slow settling time at the voltage output in response to an input frequency change. The settling time constant is equal to $R_{IN} \times C_{INT}$. A better compromise between output ripple and settling time can be achieved by using a moderately low integrator capacitor value and adding a low-pass filter on the analog output. The cutoff frequency of the filter should be made below the lowest expected input frequency to the frequency-to-voltage converter.

The system in Figure 20 makes use of both voltage-to-frequency and frequency-to-voltage modes to send a signal across an optically isolated barrier. This technique is useful not only for providing safety in the presence of high voltages, but also for creating high noise rejection in electrically noisy environments. The use of a common clock frequency causes the two devices to have complementary transfer functions, which minimizes errors.

Optical coupling is facilitated by use of the output one-shot feature. The output pulse is shortened (see "Shortened Output Pulses") to allow for the relatively slow turn-off time of the LED. The timing diagram in Figure 19 shows how the accumulated delay of both optical couplers could produce too long an input pulse for the frequency-to-voltage converter, VFC_2, of Figure 20.

An output filter is used to reduce the ripple in the output of VFC_2. In order to most effectively filter the output, both input and output VFCs are offset. By connecting R_1 to V_{REF},

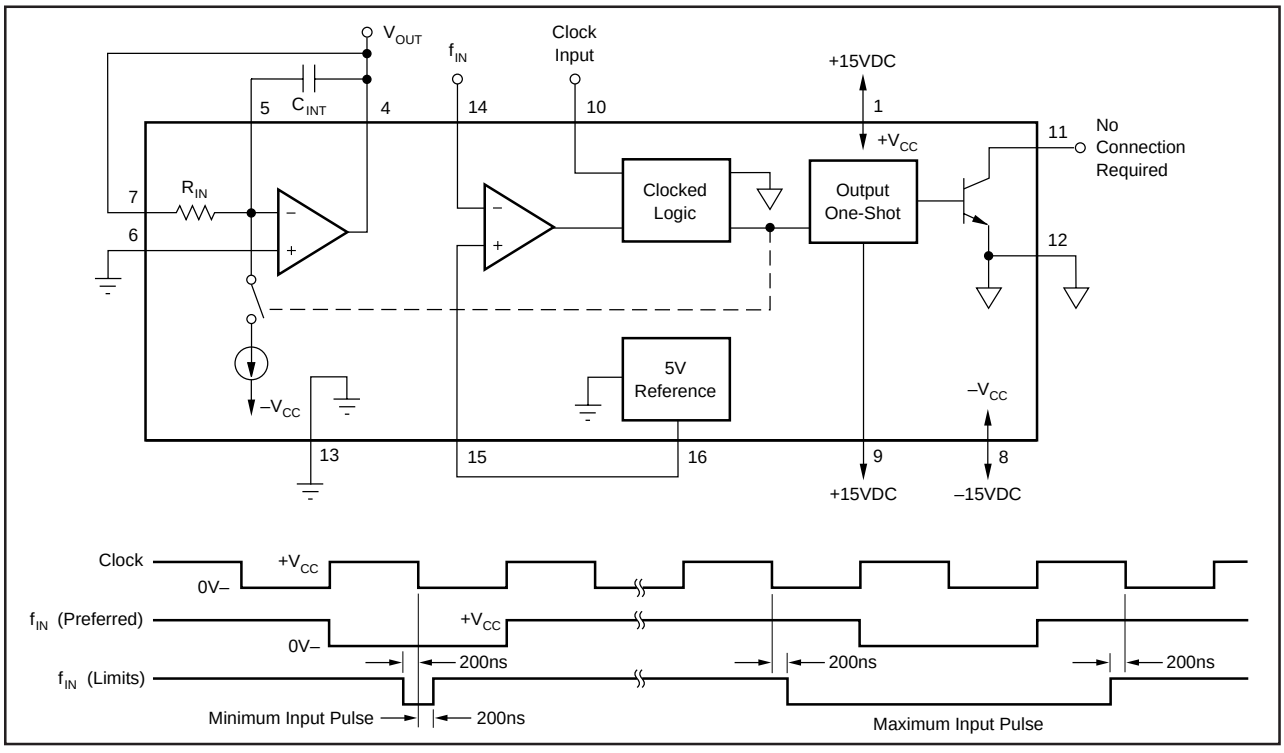


FIGURE 16. Circuit and Timing Diagram of a Frequency-to-Voltage Converter.

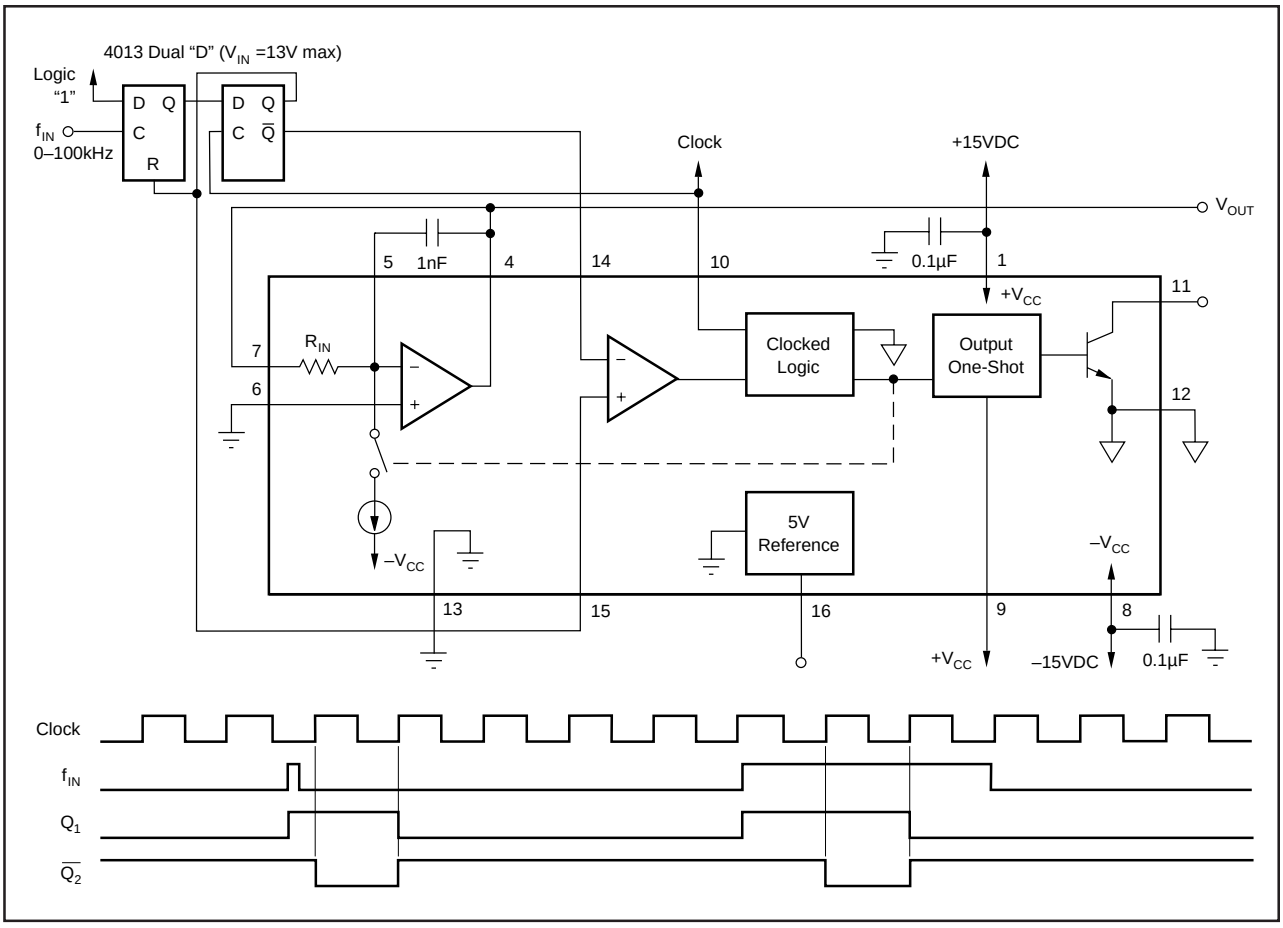


FIGURE 17. Digital Timing Input Conditioning Circuit for Frequency-to-Voltage Operation.

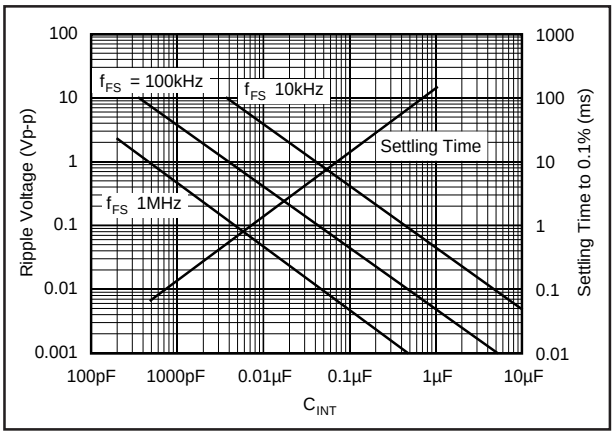


FIGURE 18. Frequency-to-Voltage Mode Output Ripple and Settling Time vs Integrator Capacitance.

an accurate offset is created in the voltage-to-frequency function. Zero volts input now creates a 10kHz output. This offset is subtracted in the frequency-to-voltage conversion on the output side, by V_{REF} and R_5.

MORE PULSE POSITION RESOLUTION

Since output pulses must always align with clock edges, the instantaneous output frequency is quantized and appears to have phase jitter. This effect can be greatly reduced by using a high speed clock so that available clock edges come more frequently. This would also create a high full-scale frequency, but the technique shown in Figure 21 offers an alternative. A high speed clock is used to produce high resolution of the output pulse position, but a low full-scale frequency can be programmed.

When an output pulse is generated, the next rising edge of the high frequency clock is delayed for a programmable number of clock counts. Since the integrator reset period (which sets the full-scale range) is determined by the time from rising edge to rising edge at the VFC's clock input once the comparator is tripped, the effective clock frequency is $f_{CLOCK}/16$. The circuit shown can be programmed for an N from 2 to 16. Since an output pulse must propagate through the VFC before the next rising edge of the clock arrives, maximum clock frequency is limited by the delay time shown in the timing diagram.

With output pulses now able to align with greater resolution, the output has lower phase jitter. Using this technique, the output is suitable for ratiometric (period measurement) type counting. This counting technique achieves the maximum possible resolution for short gate periods (see Burr-Brown Application Note AN-130).

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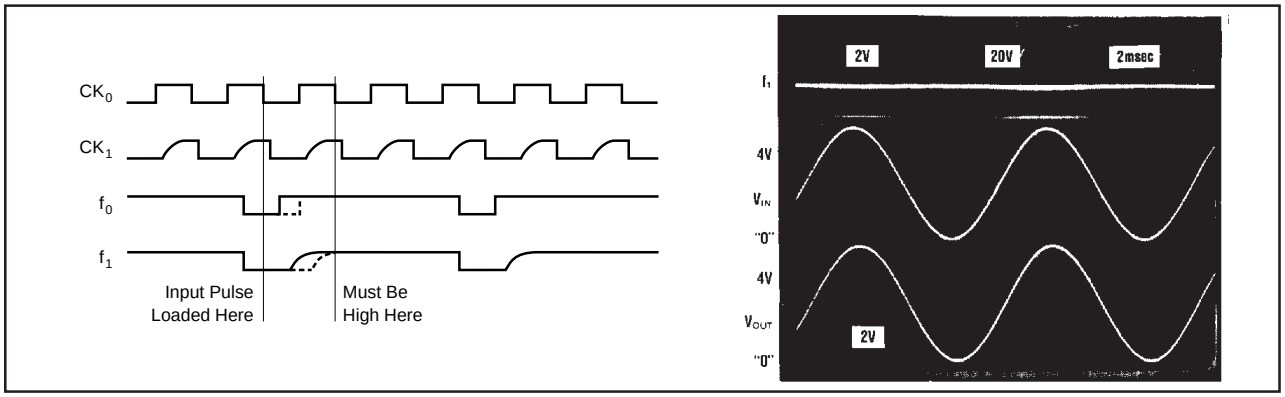

FIGURE 19. Timing Diagram and Oscilloscope Trace of Isolated Voltage-to-Frequency/Frequency-to-Voltage System.

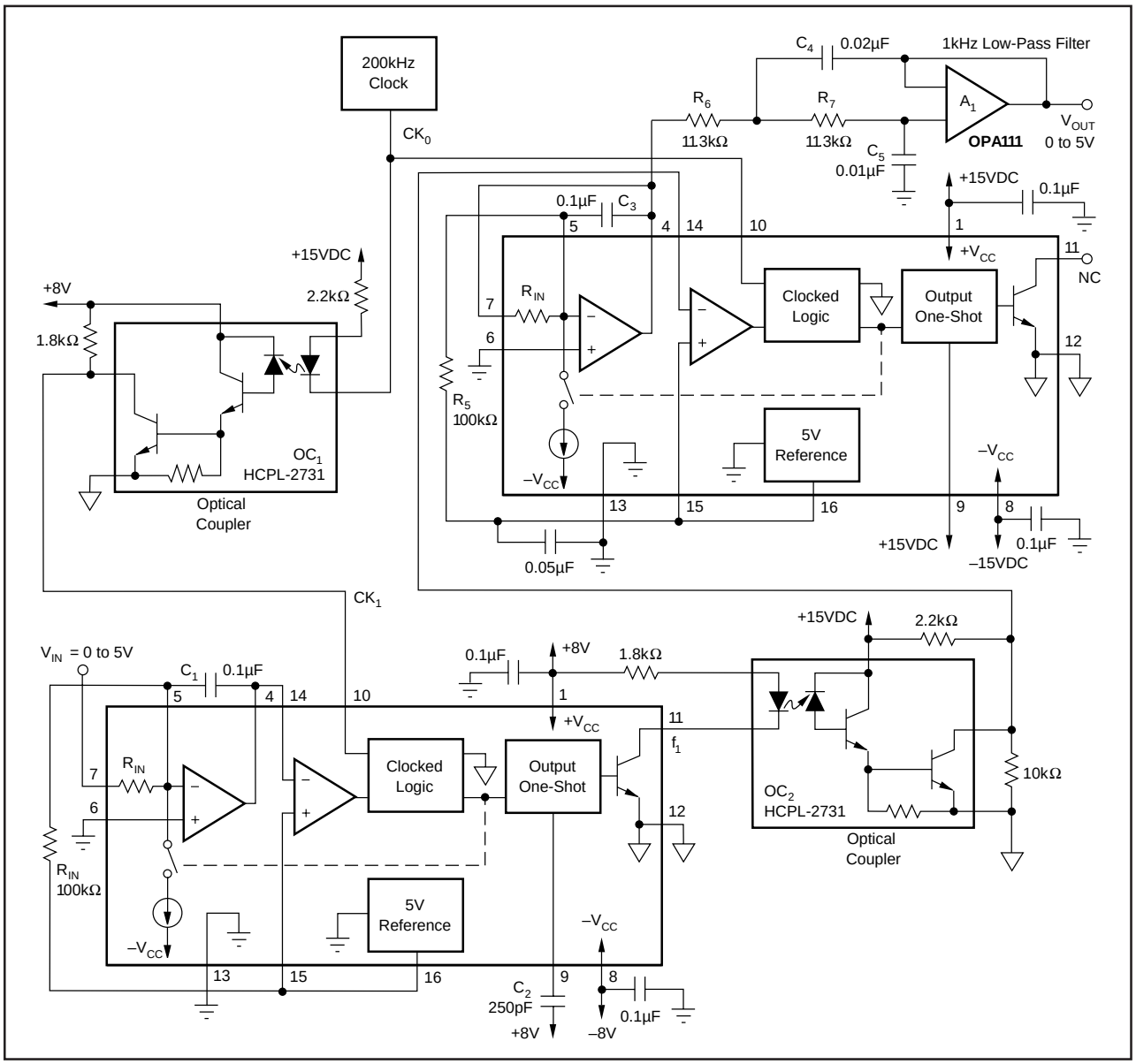

FIGURE 20. Circuit Diagram of Isolated Voltage-to-Frequency/Frequency-to-Voltage System.

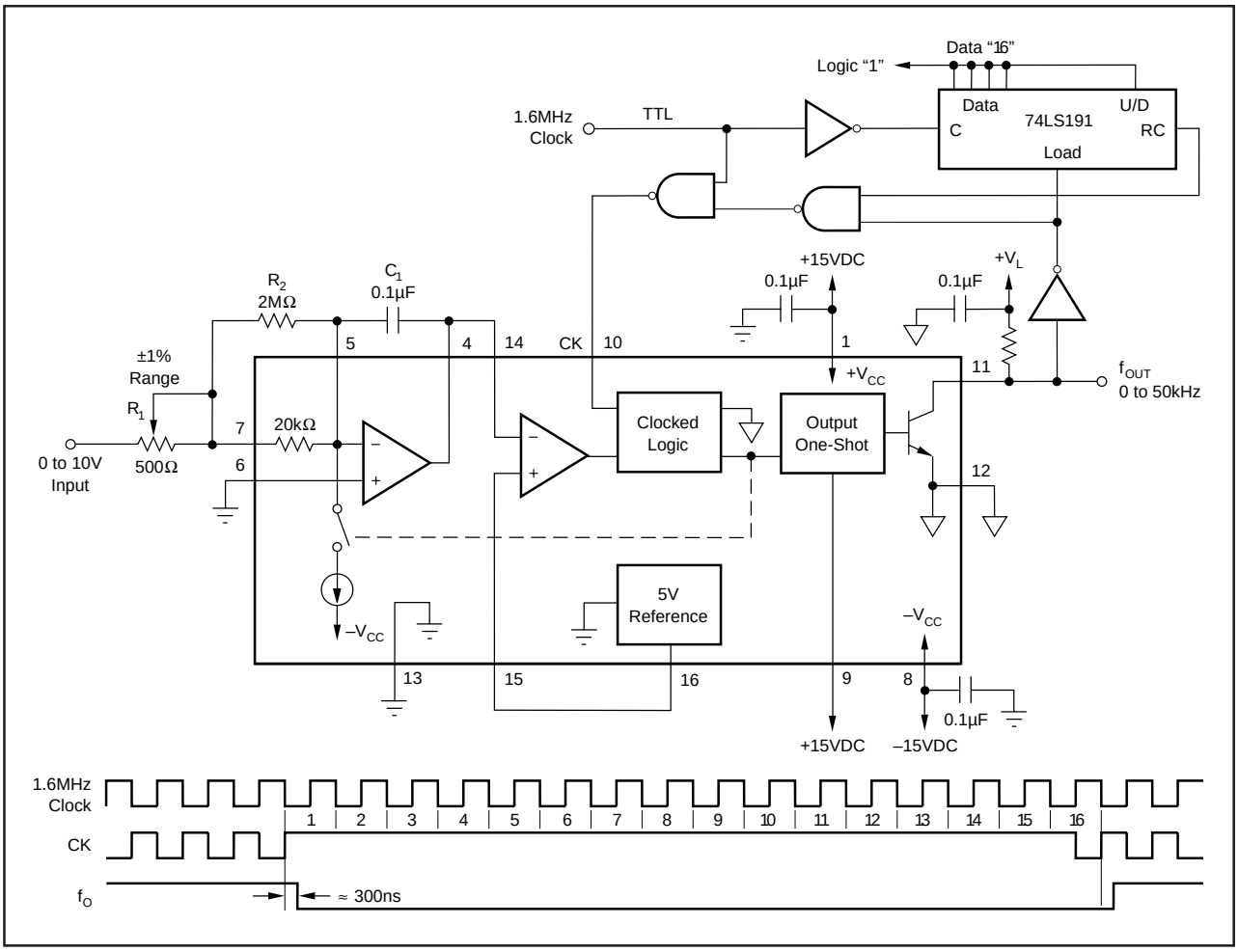

FIGURE 21. Circuit Diagram for Increased Pulse Position Resolution.

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