Ordering number : EN5477A

Wideband Output Module (Video Pack)

VP453

CRT Display Video Output Amplifier

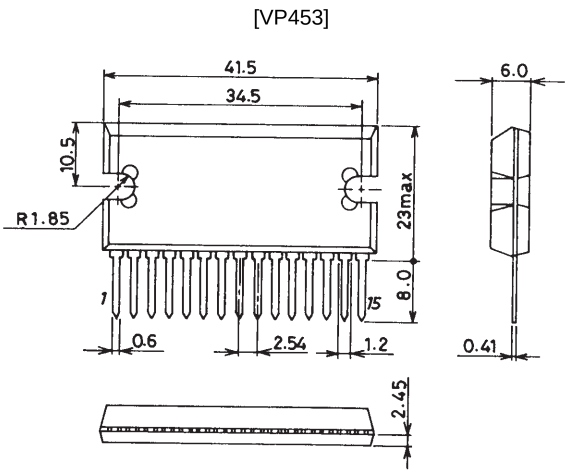
Features

- Active load circuits
- Wide bandwidth and high output voltage. Optimal for use in f_H (horizontal deflection frequency) = 90 kHz class ultrahigh precision monitors.
- Single 15-pin SIP molded package houses three channels.

Package Dimensions

unit: mm

2127A



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		90	V
Allowable power dissipation	Pd max	With an ideal heat sink at Ta = 25°C	25	W
Maximum junction temperature	Tj max		150	°C
Maximum case temperature	Tc max		100	°C
Storage temperature	Tstg		–20 to +110	°C

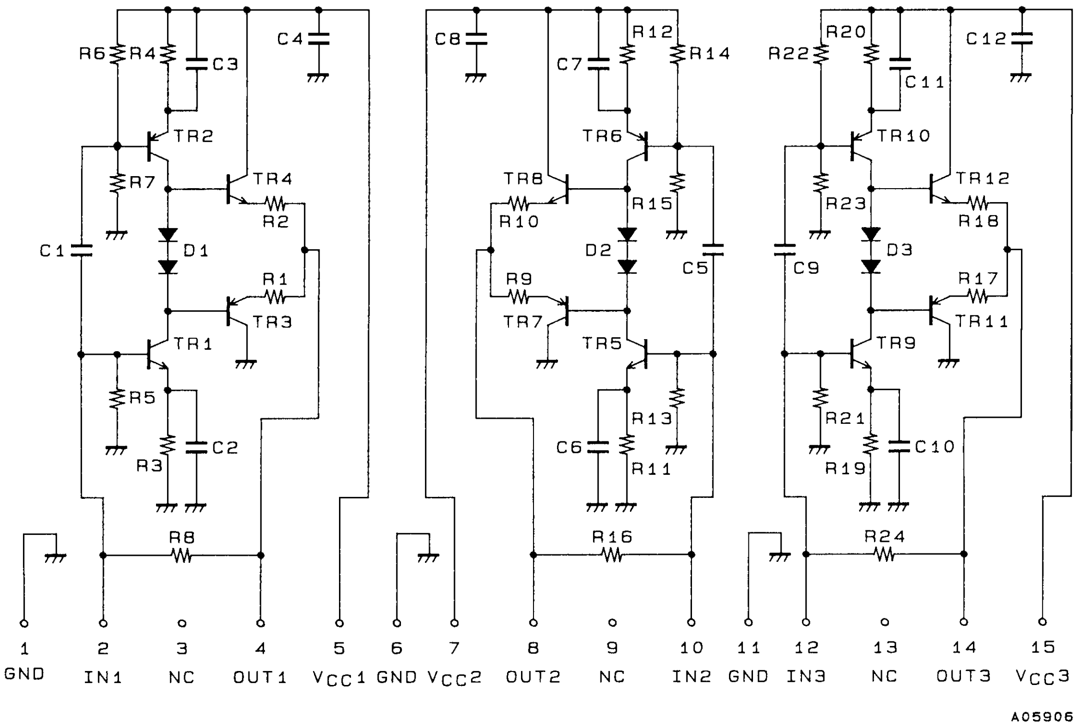
Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		80	V

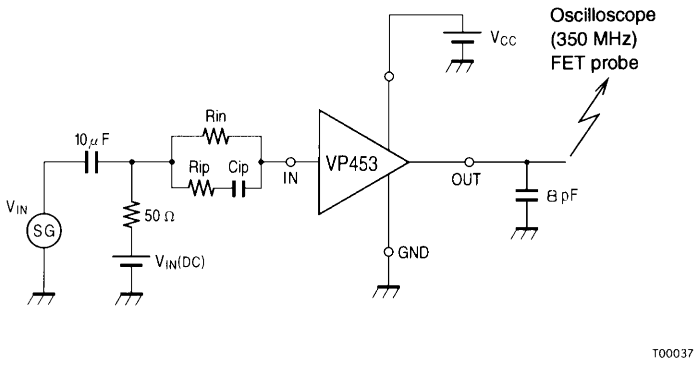
Electrical Characteristics at Ta = 25°C (For a single channel, with Rin = 560 Ω, Rip = 22 Ω, Cip = 47 pF)

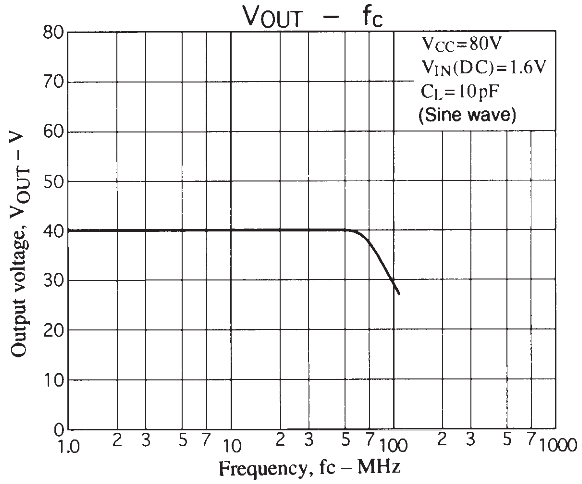
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Clock frequency bandwidth (–3 dB)	f (clock)	V_{CC} = 80 V, C_L = 10 pF V_{IN} (DC) = 1.6 V, V_{OUT} (p-p) = 40 V		190		MHz
Frequency bandwidth (–3 dB)	f_c			90		MHz
Pulse response	t_r	V_{CC} = 80 V, C_L = 10 pF V_{IN} (DC) = 1.6 V, V_{OUT} (p-p) = 40 V		4.0		ns
	t_f			3.6		ns
Voltage gain	VG (DC)		11	13	15	Double
Current drain	$I_{CC}(1)$	V_{CC} = 80 V, V_{IN} (DC) = 1.6 V, f = 10 MHz clock, C_L = 10 pF, V_{OUT} (p-p) = 40 V		35		mA
	$I_{CC}(2)$	V_{CC} = 80 V, V_{IN} (DC) = 1.6 V, f = 100 MHz clock, C_L = 10 pF, V_{OUT} (p-p) = 40 V		77		mA

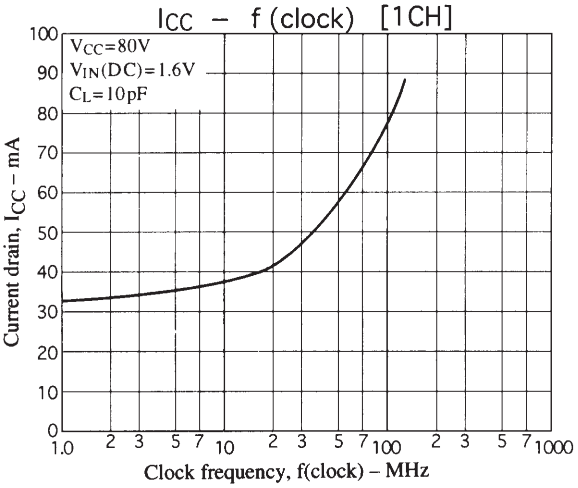
Internal Equivalent Circuit

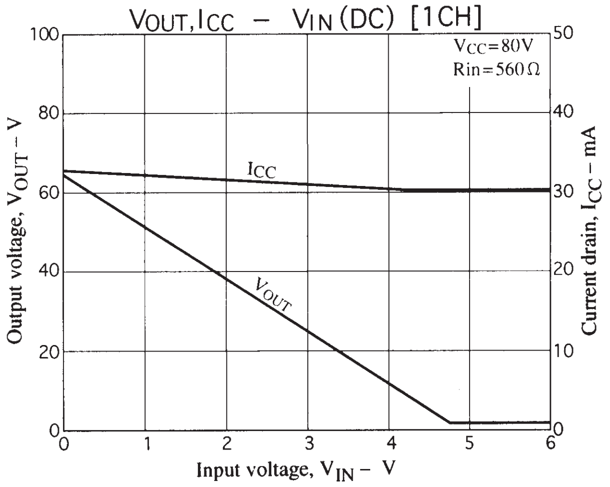


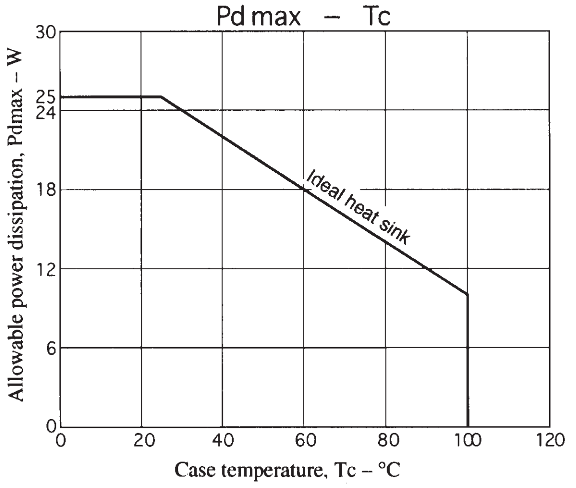
Test Circuit (for a single channel)











Thermal Design

Thermal design requires that the two conditions Tj (max) ≤ 150°C and Tc ≤ 100°C be met.

(a) Concerning Tj (max), the chip temperature Tj for each transistor is given by equation (1).

$Tj = (Tri) = \theta j\text{–}c\ (Tri) \times P_C\ (Tri) + \Delta Tc + Ta\ (°C)$ ....(1)

θj–c (Tri): The thermal resistance of each transistor chip itself

P_C (Tri): The collector loss for each transistor

ΔTc: Increase in the case temperature

Ta: Ambient temperature

θj–c (Tri) for each chip will be:

θj–c (Tr1) to (Tr4) = 35°C/W ....(2)

The loss in transistors in a video pack varies with frequency. The loss increases with the frequency.

For example, if the maximum frequency will be 120 MHz (clock), then the transistors with the largest losses will be transistors 3 and 4 in the emitter-follower (EF) stage. From the Pd – f (clock) figure, we see that that loss will be 25% of the total for a single channel. That is:

$P_C\ (EF\ stage)_{f = 120\ MHz} = Pd\ (1ch)_{f = 120\ MHz} \times 0.25\ [W]$ ....(3)

The thermal design must assure that Tj does not exceed 150°C at this time.

(b) Concerning Tc(max), the relationship between θh and ΔTc is:

$\Delta Tc = Pd\ (total) \times \theta h$ ....(4)

Taking the increase due to Ta into account, the condition the thermal design must meet becomes Tc = ΔTc + Ta < 100°C.

Next we design thermal conditions for the VP453 that meet the conditions in sections (a) and (b) above.

Sample Thermal Design for the VP453

Conditions: For an f_H = 95 kHz class monitor, f_V = 120 MHz (clock).

V_{CC} = 80 V, V_{OUT} = 40 Vp-p (C_L = 10 pF)

Here we consider the case where such a monitor is to be operated at ambient temperatures up to Ta = 60°C and at a maximum frequency of f = 100 MHz (clock).

As mentioned previously, the chips with the maximum loss will be transistors 3 and 4 in the emitter-follower stage. Equation (5) follows from deriving that value from the figure below and equation (3).

P_C (Tr3, 4)$_{f\,=\,120\text{ MHz}}$ = 6.9 × 0.25 ≈ 1.72 [W] ....(5)

However, the actual usage conditions include a blanking period. If we calculate the power during this period approximately at a 1-MHz power ratio, from Pd – f(clock) and P_C (Tri)Ratio – f (clock) figures, we see that P_C (BLK) for transistors 3 and 4 will be:

P_C BLK (Tr3, 4) = 2.6 × 0.08 = 0.21 [W].. (6)

If the blanking period is 20% of the total, from the data of equation (5) and formula (6) we see that the loss in transistors 3 and 4 will be:

P_C (Tr3, 4) = P_C (Tr3, 4) $_{f\,=\,120\text{ MHz}}$ × 0.8 + P_CBLK (Tr3, 4) × 0.2 ≈ 1.42 [W] ...(7)

Next, applying the value of θj–c to equation (7), shows ΔTj to be:

$\Delta Tj = 1.42 \times 35 \approx 50$ [°C]

Since ΔTj ≤ 50°C, it suffices to only consider the Tc ≤ 100°C condition in the thermal design. That is, in the thermal design we design θh so that Tc will be under 100°C when Pd (total) = Pd (1ch) × 3 for the time when all three channels are operating at their maximum levels.

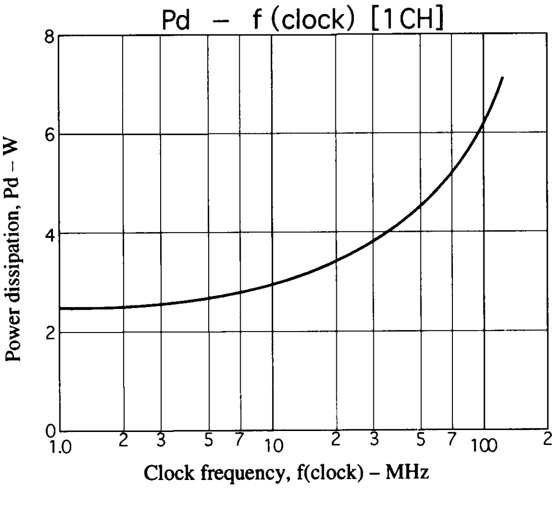
ΔTc will be: ΔTc = 100 – 60 = 40°C

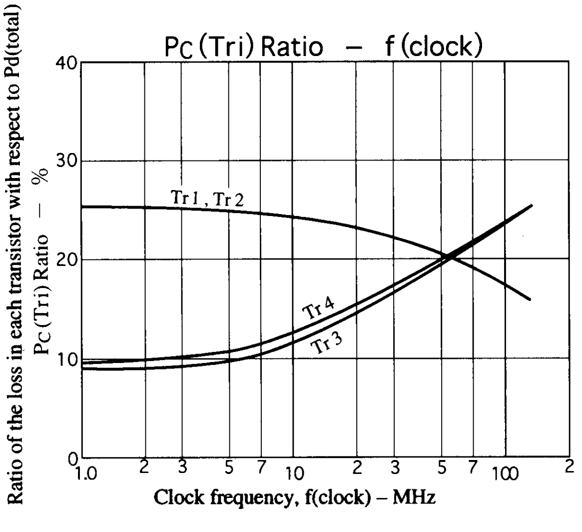
θh = ΔTc ÷ Pd (total) = 40 ÷ {(6.9 × 0.8 + 3.5 × 0.2) × 3} = 2.1

Thus:

θh = 2.1°C/W

In actual use, due to the actual ambient temperature, the operating conditions, and other factors, it will be possible to use a heat sink smaller than the one required by the above design. Users should design an optimal heat sink using the data presented above and their actual conditions.





V_{CC} (V)	V_{OUT} (V)	V_O (center)
80	40	40

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