

CA В

6X **b**

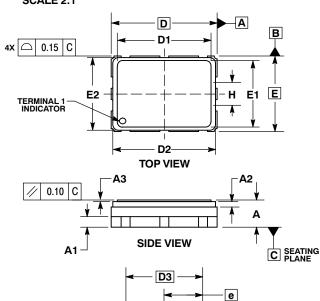
С 0.05

0.10

6 PIN CLCC, 7x5, 2.54P CASE 848AB-01 ISSUE C

DATE 17 DEC 2007

SCALE 2:1

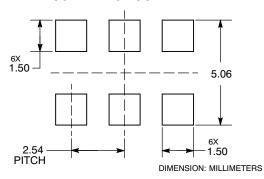


SOLDERING FOOTPRINT*

BOTTOM VIEW

E3

6X L



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

- NOTES:
 1. DIMENSIONING AND TOLERANCING PER
- ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
Α	1.70	1.80	1.90
A1	0.70 REF		
A2	0.36 REF		
A3	0.08	0.10	0.12
b	1.30	1.40	1.50
D	7.00 BSC		
D1	6.17	6.20	6.23
D2	6.66	6.81	6.96
D3	5.08 BSC		
E	5.00 BSC		
E1	4.37	4.40	4.43
E2	4.65	4.80	4.95
E3	3.49 BSC		
е	2.54 BSC		
Н	1.80 REF		
L	1.17	1.27	1.37
R	0.70 REF		

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code = Assembly Location

= Wafer Lot WL ΥY = Year WW = Work Week = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present.

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STATUS:	ON SEMICONDUCTOR STANDARD
NEW STANDARD:	
DESCRIPTION:	6 PIN CLCC, 7X5, 2.54P

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ISSUE	REVISION	DATE
0	RELEASED FOR PRODUCTION. REQ. BY C. REBELLO.	20 OCT 2006
Α	CORRECTED DEVICE MARKING. REQ. BY C. REBELLO.	13 MAR 2007
В	REVISED DEVICE MARKING. REQ. BY C. REBELLO.	05 SEP 2007
С	ADDED BEVELS TO SIDES OF PACKAGE ON TOP AND BOTTOM VIEWS. ADDED H DIMENSION. REQ. BY P. CELAYA.	17 DEC 2007

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