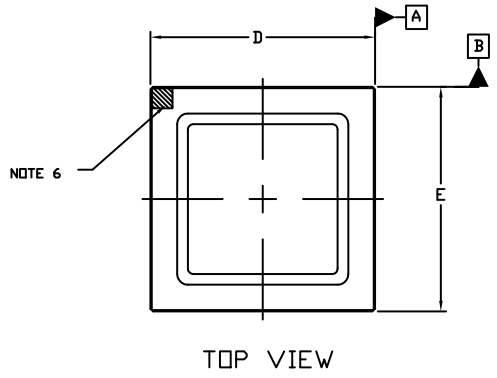
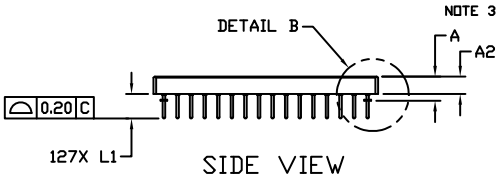
CPGA127, 42.00x42.00
CASE 107CW−01
ISSUE O

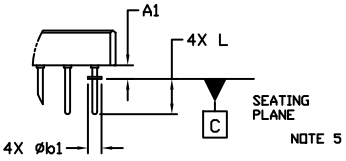
DATE 06 JUL 2011



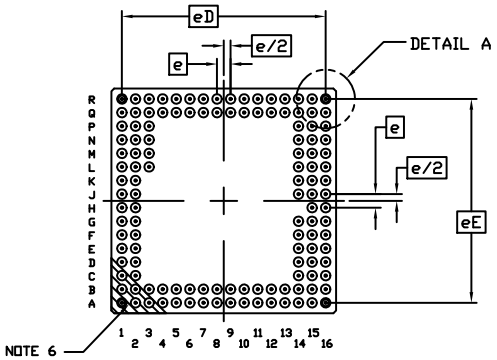
TOP VIEW



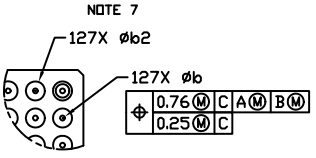
SIDE VIEW



DETAIL B
2X SCALE



BOTTOM VIEW



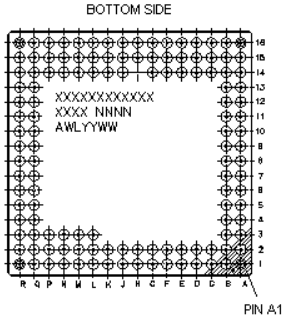
DETAIL A
2X SCALE

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION A INCLUDES THE PACKAGE BODY AND LID BUT DOES NOT INCLUDE HEATSINKS OR OTHER ATTACHED FEATURES.
4. DIMENSIONS D AND E DO NOT INCLUDE PROTRUSIONS. SUCH PROTRUSIONS SHALL NOT EXTEND MORE THAN 0.08 ON ANY SIDE. CORNERS AND EDGES OF THE PACKAGE MAY HAVE CHAMFERS.
5. THE SEATING PLANE IS DEFINED BY THE OUTER STAND-OFF SURFACE . STAND-OFFS ARE LOCATED ON THE PIN MATRIX DIAGONALS.
6. PIN A1 IDENTIFICATION WILL BE IN THESE AREAS. ID TYPE MAY CONSIST OF NOTCHES, METALLIZED MARKINGS, OR OTHER FEATURES.
7. THIS DIMENSION DEFINES THE MAXIMUM SIZE FOR THE PIN BRAZE PADS.

	MILLIMETERS	
DIM	MIN.	MAX.
A	4.06	4.98
A1	1.14	1.40
A2	3.25 REF	
b	0.43	0.50
b1	1.14	1.40
b2	---	2.03
D	41.58	42.42
E	41.58	42.42
e	2.54 BSC	
eD	38.10 BSC	
eE	38.10 BSC	
L	3.17	3.43
L1	4.44	4.70

GENERIC MARKING DIAGRAM



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
NNNN = Serial Number

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STATUS:	**ON SEMICONDUCTOR STANDARD**		
REFERENCE:			
DESCRIPTION:	**CPGA127, 42.00 X 42.00**		**PAGE 1 OF 2**

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION FROM CYPRESS DRAWING #001−07580 TO ON SEMICONDUCTOR. REQ. BY K. BERKMAN.	06 JUL 2011