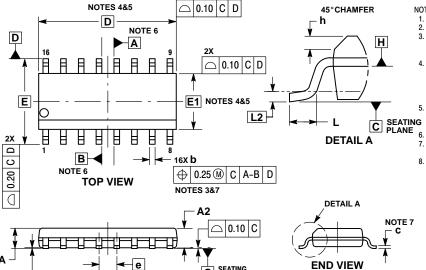


Α1

NOTE 8

## SOIC-16 CASE 751BA **ISSUE A**

**DATE 18 MAY 2015** 



SEATING PLANE

- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

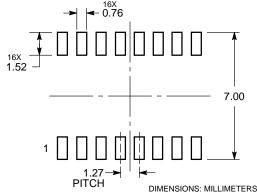
  2. CONTROLLING DIMENSION: MILLIMETERS.

  3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006 mm PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM H.
- DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN  $0.10\ TO\ 0.25\ FROM\ THE LEAD\ TIP.$
- A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

|     | MILLIMETERS |      |
|-----|-------------|------|
| DIM | MIN         | MAX  |
| Α   |             | 1.75 |
| A1  | 0.10        | 0.25 |
| A2  | 1.25        |      |
| b   | 0.31        | 0.51 |
| C   | 0.10        | 0.25 |
| D   | 9.90 BSC    |      |
| Е   | 6.00 BSC    |      |
| E1  | 3.90 BSC    |      |
| е   | 1.27 BSC    |      |
| h   | 0.25        | 0.41 |
| L   | 0.40        | 1.27 |
| L2  | 0.25 BSC    |      |

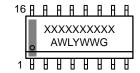
## **RECOMMENDED SOLDERING FOOTPRINT\***

**SIDE VIEW** 



<sup>\*</sup>For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## **GENERIC MARKING DIAGRAM\***



XXXXX = Specific Device Code

= Assembly Location

WI = Wafer Lot Υ = Year WW = Work Week G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

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|--------|--|-------------|--|--|
| ISSUE  | REVISION   | DATE        |  |  |
| 0      | RELEASED FOR PRODUCTION FROM POD #6000209 TO ON SEMICONDUCTOR. REQ. BY B. BERGMAN. | 19 SEP 2008 |  |  |
| Α      | REDREW DRAWING TO JEDEC STANDARDS AND ADDED SOLDER FOOTPRINT. REQ. BY F. KOLANKO.  | 18 MAY 2015 |  |  |
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