SOIC20 NB LESS PINS 2, 4 & 19

CASE 751BS-01 **ISSUE 0**

DATE 28 APR 2011

NOTES:

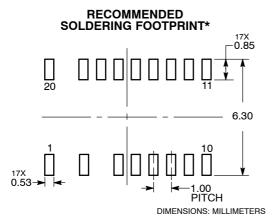
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994. CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 TOTAL IN EXCESS OF THE 6 DIMENSION. DIMENSION 6 APPLIES TO THE FLAT PORTION OF THE LEAD AND SHALL BE MEASURED BETWEEN 0.13 AND 0.25 FROM THE TIP.
 DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH.
- PROTRUSIONS, OR GATE BURRS BUT DO INCLUDE MOLD MISMATCH. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
- DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
- A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEAT-ING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
- CHAMFER FEATURE IS OPTIONAL. IF NOT PRESENT, THEN A PIN ONE IDENTIFIER MUST BE LOCATED IN THIS AREA.

	MILLIMETERS		
DIM	MIN	MAX	
Α		1.70	
A1	0.00	0.20	
b	0.31	0.51	
С	0.10	0.25	
D	9.90 BSC		
Е	6.00 BSC		
E1	3.90 BSC		
е	1.00 BSC		
h	0.25	0.50	
L	0.40	0.85	
L2	0.25 BSC		
M	0°	8°	

SCALE 1:1 □ 0.10 | C | A-B NOTE 4 D D NOTE 5 A NOTE 4 E1 Ε C SEATING **DETAIL A** Н \triangle 0.10 C A-B 0.20 е 17X b NOTE 5 B ⊕ 0.25 M C A-B D

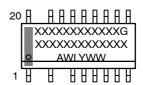
NOTE 3





*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code = Assembly Location Α

WL = Wafer Lot = Year WW = Work Week G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present.

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STATUS:	ON SEMICONDUCTOR STANDARD	acces versio
NEW STANDARD:		"CON
DESCRIPTION:	SOIC20 NB LESS PINS 2, 4 & 19	

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