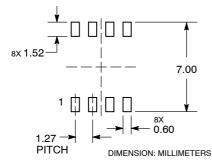


## **RECOMMENDED SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## **VSOIC8 NB** CASE 753AA

**DATE 16 OCT 2012** 

- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSION & DOES NOT INCLUDE DAMBAR
  PROTRUSION. ALLOWABLE PROTRUSION SHALL
  BE 0.10mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
- 4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
- DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
- A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS		
DIM	MIN	MAX	
Α	0.65	0.85	
A1	0.05		
b	0.31	0.51	
С	0.17	0.25	
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
е	1.27 BSC		
L	0.40	1.27	
L2	0.25 BSC		

## **GENERIC MARKING DIAGRAM\***



XXXXX = Specific Device Code

= Assembly Location Α

= Wafer Lot L

Υ

W = Work Week

= Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

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