New Jersey Semi-Conductor Products, Inc.

MAC15 Series

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Triacs

Silicon Bidirectional Thyristors

Designed primarily for full-wave ac control applications, such as solid–state relays, motor controls, heating controls and power supplies; or wherever full–wave silicon gate controlled solid–state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied main terminal voltage with positive or negative gate triggering.

Features

- Blocking Voltage to 800 V
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Three Modes (MAC15 Series) or Four Modes (MAC15A Series)
- These Devices are Pb–Free and are RoHS Compliant*

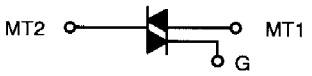
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off–State Voltage Note 1 (T_J = –40 to +125°C, Sine Wave 50 to 60 Hz, Gate Open) MAC15A6G MAC15–8G, MAC15A8G MAC15–10G, MAC15A10G	V_{DRM}, V_{RRM}	 400 600 800	V
Peak Gate Voltage (Pulse Width ≤ 1.0 μsec; T_C = 90°C)	V_{GM}	10	V
On–State Current RMS; Full Cycle Sine Wave 50 to 60 Hz (T_C = +90°C)	$I_{T(RMS)}$	15	A
Circuit Fusing Consideration (t = 8.3 ms)	I^2t	93	A^2s
Peak Non–Repetitive Surge Current (One Full Cycle Sine Wave, 60 Hz, T_C = +80°C) Preceded and Followed by Rated Current	I_{TSM}	150	A
Peak Gate Power (T_C = +80°C, Pulse Width = 1.0 μs)	P_{GM}	20	W
Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	W
Peak Gate Current (Pulse Width ≤ 1.0 μsec; T_C = 90°C)	I_{GM}	2.0	A
Operating Junction Temperature Range	T_J	–40 to +125	°C
Storage Temperature Range	T_{stg}	–40 to +150	°C

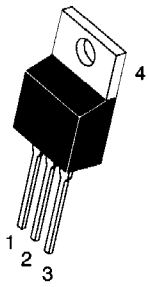
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

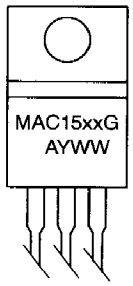
TRIACS
15 AMPERES RMS
400 thru 800 VOLTS



MARKING DIAGRAM



TO–220AB



MAC15xx = Specific Device Code
xx = See Table on Page 2
A = Assembly Location (Optional)*
Y = Year
WW = Work Week

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	2.0	°C/W
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 10 Seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted; Electricals apply in both directions)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Peak Blocking Current (V_D = Rated V_{DRM}, V_{RRM}; Gate Open)	T_J = 25°C T_J = 125°C	I_{DRM}, I_{RRM}	– –	– –	10 2.0	μA mA
ON CHARACTERISTICS						
Peak On–State Voltage Note 2 (I_{TM} = ±21 A Peak)		V_{TM}	–	1.3	1.6	V
Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, R_L = 100 Ω) MT2(+), G(+) MT2(+), G(–) MT2(–), G(–) MT2(–), G(+) "A" SUFFIX ONLY		I_{GT}	 – – – –	 – – – –	 50 50 50 75	mA
Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc, R_L = 100 Ω) MT2(+), G(+) MT2(+), G(–) MT2(–), G(–) MT2(–), G(+) "A" SUFFIX ONLY		V_{GT}	 – – – –	 0.9 0.9 1.1 1.4	 2 2 2 2.5	V
Gate Non–Trigger Voltage (V_D = 12 V, R_L = 100 Ω) T_J = 110°C) MT2(+), G(+); MT2(–), G(–); MT2(+), G(–) MT2(–), G(+) "A" SUFFIX ONLY		V_{GD}	 0.2 0.2	 – –	 – –	V
Holding Current (V_D = 12 Vdc, Gate Open, Initiating Current = ±200 mA)		I_H	–	6.0	40	mA
Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 17 A) (I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2 μs)		t_{gt}	–	1.5	–	μs
DYNAMIC CHARACTERISTICS						
Critical Rate of Rise of Commutation Voltage (V_D = Rated V_{DRM}, I_{TM} = 21 A, Commutating di/dt = 7.6 A/ms, Gate Unenergized, T_C = 80°C)		dv/dt(c)	–	5.0	–	V/μs

2. Pulse Test: Pulse Width ≤ 2.0 ms, Duty Cycle ≤ 2%.