

2N1792, 2N1805, 2N1909, 2N2023 SERIES 110 Amp RMS SCRs

Major Ratings and Characteristics

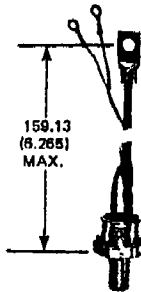
	2N1792 thru 2N1804	2N1805 thru 2N1807	2N1909 thru 2N1916	2N2023 thru 2N2030	Units
I_T (RMS)	110	110	110	110	A
I_T (AV)	70*	70*	70*	70*	A
θ_{TC}	86*	62*	86*	86*	$^{\circ}C$
I_{TSM} @ 50 Hz	955	955	955	955	A
@ 60 Hz	1,000*	1,000*	1,000*	1,000*	A
I_{2t} @ 50 Hz	4,550	4,550	4,550	4,550	A^2s
@ 60 Hz	4,150	4,150	4,150	4,150	A^2s
I_{GT}	70	70	70	70	mA
dv/dt	200	200	80	80	V/ μs
di/dt	100	100	100	100	A/ μs
T_J	-65* to 125*	-40* to 125*	-65* to 160*	-65* to 160*	$^{\circ}C$
V_{RRM}, V_{DRM} range	50* to 1,200*	25* to 840*	25* to 400*	25* to 400*	V

*JEDEC registered values

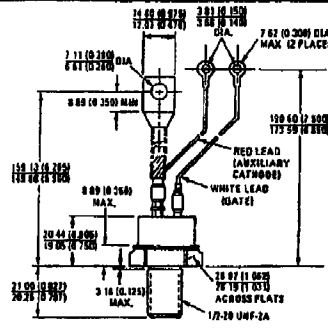
Description/Features

- For general purpose phase control applications
- Forward and reverse voltage ratings up to 1200V
- High temperature series
- High surge rating
- Standard 1/2" — 20 stud

CASE STYLE AND DIMENSIONS



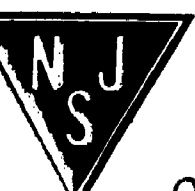
Case style (ceramic) A-11 furnished when part is rated 1000V or higher. A-13 (glass) for parts below 1000V.



Refer to Page A-34 for flag terminal Case Style

All Dimensions in Millimeters and (Inches)

IR Case Style A-13
Conforms to JEDEC Outline YO-208AC (YO-84)



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VOLTAGE RATINGS (Applied gate voltage zero or negative)

Part Numbers			V_{RRM} - Max. Repetitive Peak Reverse Voltage (V)	V_{DRM} - Max. Repetitive Peak Off-State Voltage (V) (1)	V_{RSM} - Max. Non-Repetitive Peak Reverse Voltage $t_p < 5$ ms (V)
TO-208AD Case	TO-209AC Case	TO-209AC Case	$T_J = -40^\circ\text{C to } 125^\circ\text{C}$	$T_J = -40^\circ\text{C to } 125^\circ\text{C}$	$T_J = 25^\circ\text{C to } 125^\circ\text{C}$
—	2N1809	2N2023	25*	25*	35*
2N1792	2N1910	2N2024	50*	50*	70*
2N1793	2N1911	2N2025	100*	100*	150*
2N1784	2N1912	2N2026	150*	150*	225*
2N1795	2N1913	2N2027	200*	200*	300*
2N1796	2N1914	2N2028	250*	250*	360*
2N1797	2N1915	2N2029	300*	300*	400*
2N1798	2N1916	2N2030	400*	400*	500*
2N1799	2N1805	—	600*	500*	625*
2N1800	2N1806	—	720*	600*	750*
2N1801	2N1807	—	840*	700*	880*
2N1802	—	—	960*	800*	1000*
2N1803	—	—	1080*	900*	1130*
2N1804	—	—	1200*	1000*	1250*

ELECTRICAL SPECIFICATIONS

	2N1792 to 2N1804	2N1805-16 2N1805-07	2N2023-30	Units	Conditions
ON-STATE					
$I_{T(RMS)}$ Max. RMS on-state current	110	110	110	A	
$I_{T(AV)}$ Max. average on-state current @ Max. T_C *	70*	70*	70*	A	180° half sine wave condition.
	65*	62*	65*	°C	
I_{TSM} Max. peak one cycle, non-repetitive surge current	955	955	955	A	50 Hz half cycle sine wave or 6 ms rectangular pulse Following any rated load condition, and with rated V_{RRM} applied following surge. BCR turned fully on.
	1000*	1000*	1000*	A	80 Hz half cycle sine wave or 5 ms rectangular pulse
	1150	1150	1150	A	50 Hz half cycle sine wave or 6 ms rectangular pulse Same conditions as above except with V_{RRM} applied following surge = 0.
	1200	1200	1200	A	80 Hz half cycle sine wave or 5 ms rectangular pulse
I^2t Max. I^2t capability, for fusing	4550	4550	4550	A ² s	$t = 10$ ms Rated V_{RRM} applied following surge, Initial $T_J = \text{max. rated}$
	4160	4160	4160	A ² s	$t = 8.3$ ms
I^2t Max. I^2t capability, for individual device fusing	6450	6450	6450	A ² s	$t = 10$ ms $V_{RRM} = 0$ following surge, Initial $T_J = \text{max. rated}$
	5900	5900	5900	A ² s	$t = 8.3$ ms
$I^2\sqrt{t}$ Max. $I^2\sqrt{t}$ capability, for individual device fusing (2)	64 500	64 500	64 500	A ² √s	$t = 0.1$ to 10 ms, V_{RRM} following surge = 0, Initial $T_J = \text{max. rated}$
V_{TM} Max. peak on-state voltage	1.85*	1.85*	1.8*	V	$T_J = 25^\circ\text{C}$, $I_{T(AV)} = 70\text{A}$ (220A peak)
	2.0*	—	—	V	$T_J = 25^\circ\text{C}$, $I_{T(AV)} = 70\text{A}$ (220A peak) 2N1803 & 2N1804 only
I_H Typical holding current.	20	20	20	mA	$T_C = 25^\circ\text{C}$, anode supply = 22V, initial $I_T = 2\text{A}$.

* JEDEC registered values.

(1) Units may be broken over non-repetitively without damage if di/dt does not exceed 20 A/μs.

(2) I^2t for time $t_x = I^2\sqrt{t} \sqrt{t_x}$.

ELECTRICAL SPECIFICATIONS (Continued)

		2N1792 to 2N1804	2N1806-16 2N1805-07	2N2023-30	Units	Conditions
BLOCKING						
dv/dt	Min. critical rate-of-rise of off-state voltage	200	200	50	V/ μ s	T _J = 125°C Exponential to 100% rated V _{DRM} . Gate open circuit. T _J = 150°C for 2N2023-30.
I _{R(AV)} & I _{D(AV)}	Max. average reverse and off-state current V _{RRM} & V _{DRM}					At rated V _{RRM} , V _{DRM} . T _J = max. rated, gate open circuited.
	- 25V to 150V	8.5*	8.5*	8.5*		
	- 200V	8.0*	8.5*	8.0*		
	- 250V	8.5*	8.5*	8.5*		
	- 300V	5.0*	8.0*	5.0*		
	- 400V	4.0*	4.0*	4.0*		
	- 500V to 600V	3.3* ^①	3.3* ^②	—		
	- 700V to 800V	3.0* ^③	3.0* ^④	—		
	- 900V to 1200V	2.7* ^⑤	—	—		
SWITCHING						
t _d	Typical delay time	1	1	1	μ s	T _C = 25°C, V _{DM} = rated V _{DRM} , I _{TM} = 80A dc resistive circuit. Gate pulse: 10V, 25 Ω source, t _p = 6 μ s, t _r = 0.1 μ s
t _r	Typical rise time	1.5	1.5	1.5		
t _f	Typical turn-off time	40	40	40 (70 @ 150°C)	μ s	T _C = 125°C, I _{TM} = 80A, commutating di/dt = -5 A/ μ s, min. V _R during turn-off interval = 50V, dv/dt = 20 V/ μ s linear to rated V _{DRM} .
dI/dt	Max. non-repetitive rate-of-rise of turned-on current V _{DRM}				A/ μ s	T _C = 125°C, V _{DM} = rated V _{DRM} I _{TM} = (2 x rated di/dt) A Gate pulse: 20V, 15 Ω , t _p > 6 μ s, t _r = 0.1 μ s Per JEDEC Standard BS-207, 5.2.2.8.
	- 25V to 600V	100	100	100		
	- 700V to 1200V	75	75	75		
TRIGGERING						
P _{GM}	Max. peak gate power	5*	5*	5*	W	t _p = 5 ms max.
P _{G(AV)}	Max. average gate power	0.5*	0.5*	0.5*	W	
+I _{GM}	Max. peak positive gate current	2*	2*	2*	A	
+V _{GM}	Max. peak positive gate voltage	10*	10*	10*	V	
-V _{GM}	Max. peak negative gate voltage	5*	5*	5*	V	
I _{GT}	Max. required DC gate current to trigger	130* ①	130*	150* @ -55°C	mA	T _C = -40°C. Max. required gate trigger current is the lowest value which will trigger all units with +6V anode-to-cathode. T _C = 25°C T _C = 125°C T _C = 150°C
		70* ②	70	70		
		40* ③	40	—		
		—	—	35		
	Typical DC gate current to trigger	35	35	35		T _C = 25°C +6V anode-to-cathode